A HAYDEN PUBLICATION

ElectronicDesign®

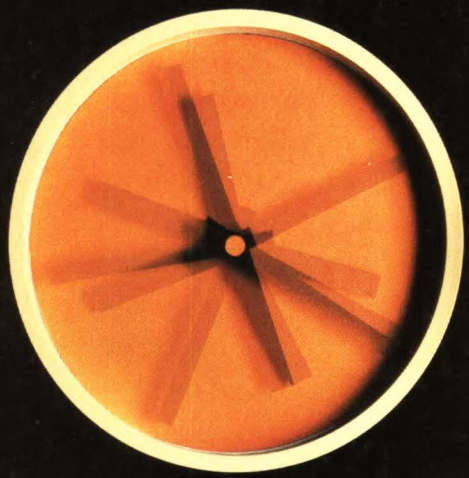
FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

DECEMBER 27, 1984

Designer's Reference: Software standards remain elusive for CAE, networks

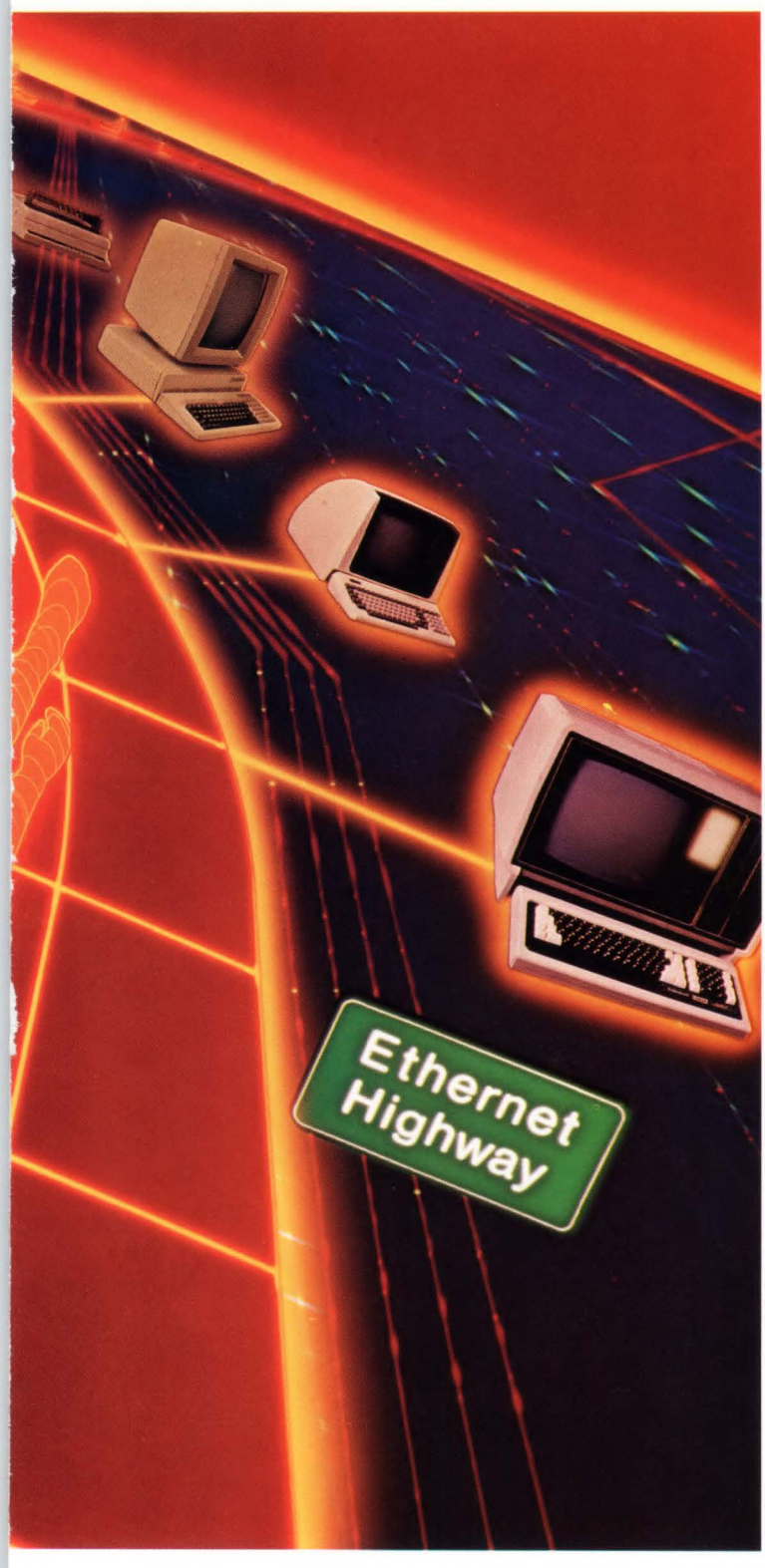
Personal Computer Survey: Users look for a wide variety of improvements

Graphics workstation sculpts 3D models with high resolution, brilliant color



GaAs RAM creates cache that cycles at half the speed of light

ETHERNET CHIP SET IS HERE



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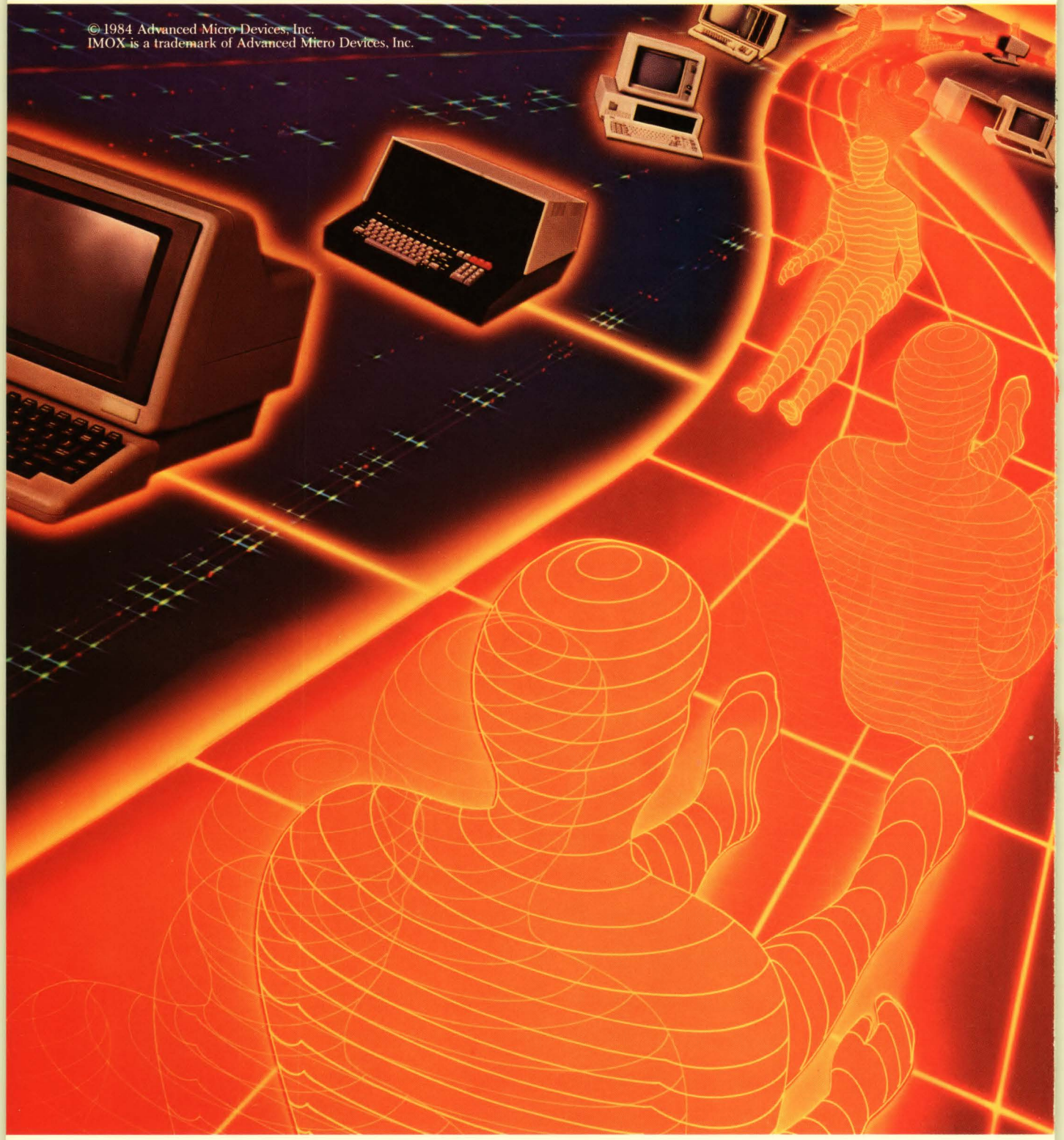
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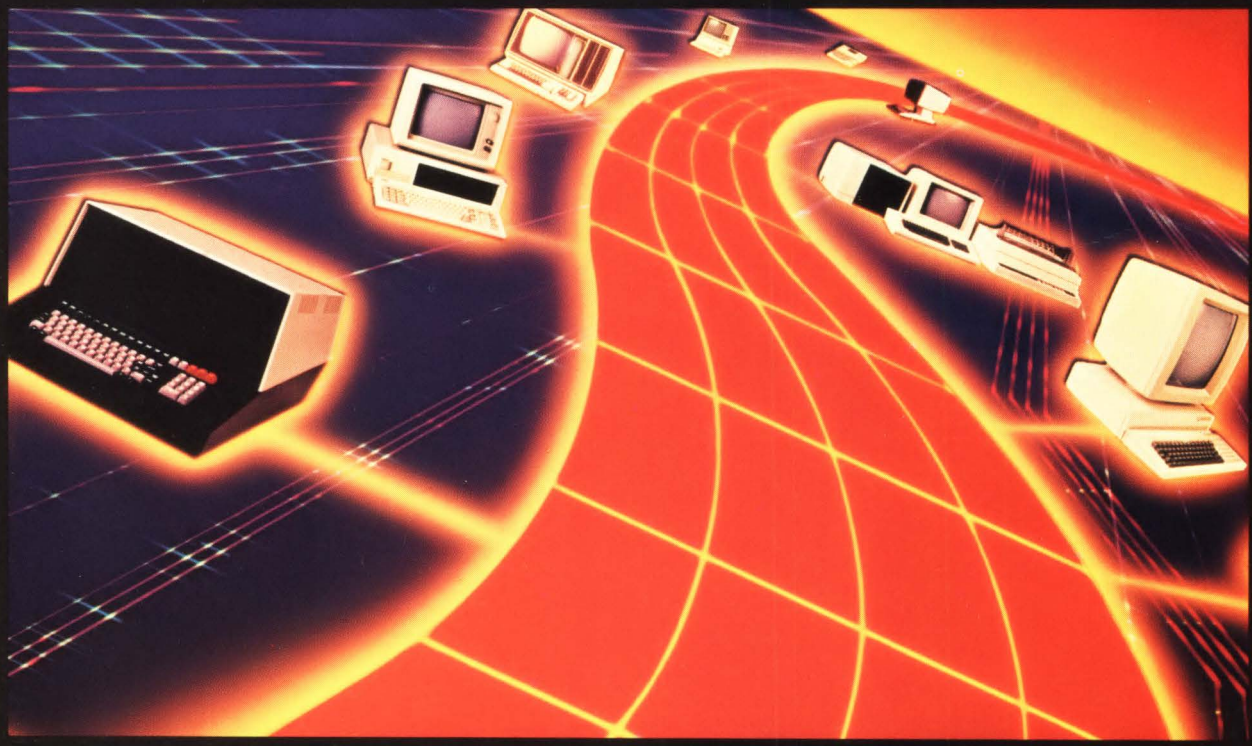

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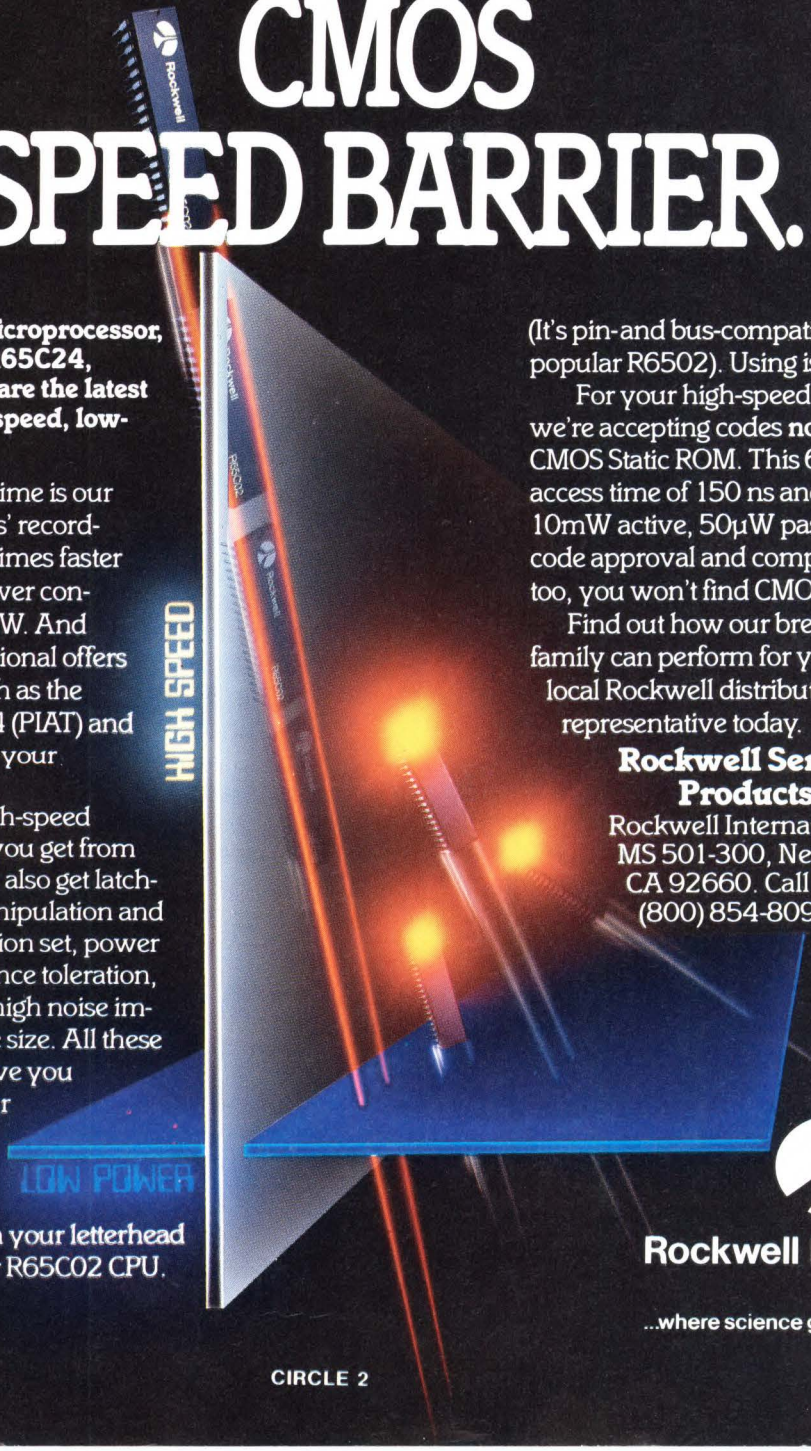

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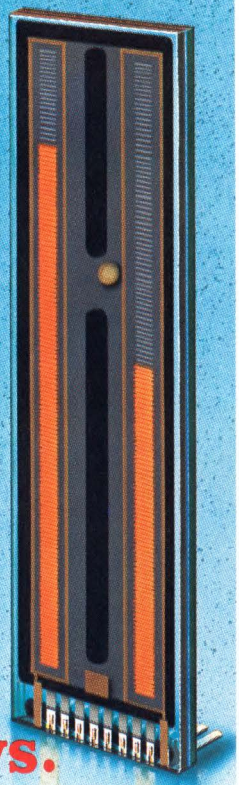

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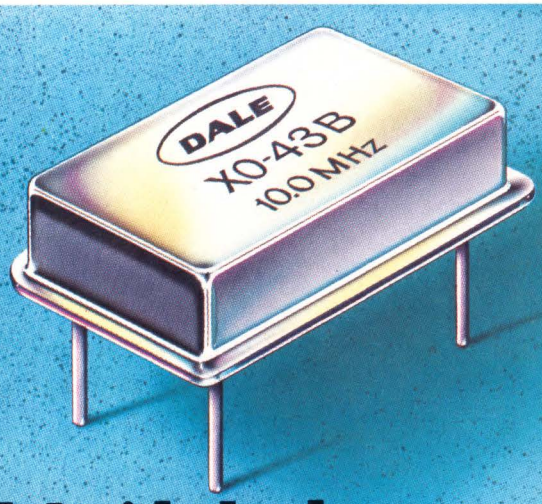

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BEHIND THE COVER

At the outset, their goal was lofty but conventional enough: mass-produce a 1-ns, 1-kbit gallium arsenide RAM by the start of 1985. Unexpectedly, they may also have invented what could become a classic memory architecture.

"In the new realm of speed, the traditional RAM design would not work," says Stewart Sando, strategic marketing director at GigaBit Logic and one author of this issue's cover story (p. 157). "Below a 5-ns cycle time, the rule book starts changing wildly," confirms coauthor and director of RAM development, Andy Graham.

Not that mass-producing any RAM with such speed is easy. To date, 1-ns cycle time has belonged in the laboratory. So starting in 1983, Graham led GigaBit's team of GaAs experts and commercial silicon designers in developing a manufacturable 1-ns RAM. By early this year they had seen "first GaAs" and verified their novel high-speed cell's operation.

Then for a month, equipped with timing diagrams, proposed pinouts, and block diagrams, Sando and Graham discussed the target specifications with potential customers—the makers of supercomputers, array processors, and signal processors. Observes Graham, "Each was running into different fundamental limits. Yet the more we talked, the more clearly a common denominator emerged."

Evidently at a 1-ns cycle time, no asynchrony among RAM inputs would be tolerated. Nor could inputs remain rock-steady till the output pulse was ready. Worst of all, a write pulse of 500 ps was essential yet extremely elusive.

A generic solution soon evolved. On-chip latches and an on-chip clock would synchronize inputs and regulate outputs, pipelining the two sets of signals would save time, and on-chip timing generation would expedite the write pulse. By the final few interviews with manufacturers, Sando recalls, he and Graham were simply marching in with their revised specifications and "getting instant concurrence."

The new RAM paves part of the way for the fifth generation of computers. "We can also see its architecture becoming the standard for sub-5-ns memory design," says Sando.

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December 27, 1984 • Vol. 32 No. 26

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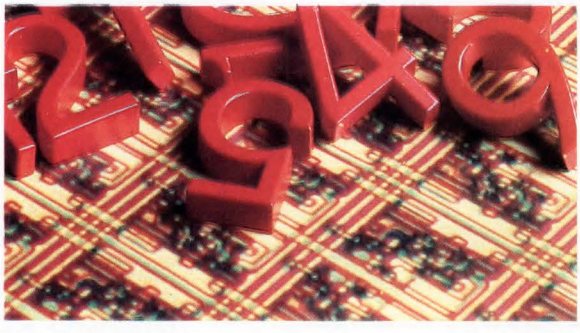

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Cover photograph by David Wagner

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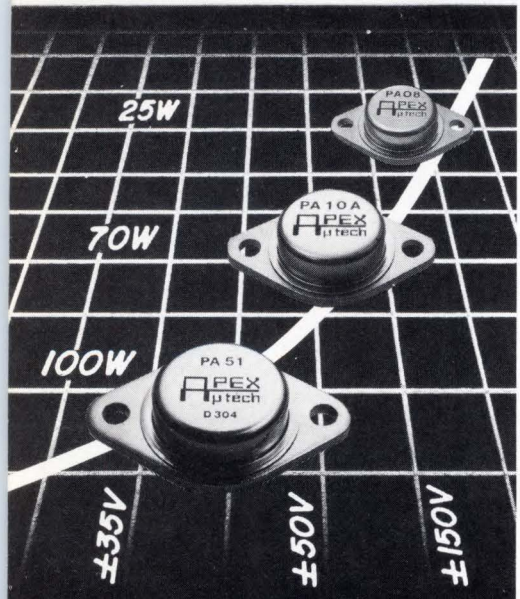

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Designer's Reference 85

If one word were needed to define the search for standards, that word would have to be "elusive." Nowhere is that truer than in the realm of software standards. The abstract and frequently changing nature of software dictates extremely adaptable standards. This year's Designer's Reference examines standards in three particularly difficult areas: networks (p. 87), computer-aided engineering (p. 99), and operating systems (p. 119). Though much is still left to the imagination, cooperation within the industry is producing some standard software protocols and practices that system designers can put their hands on.

Personal Computer Series 135

No matter how quickly the manufacturers of personal computers rush new ideas and architectures into production, the voracious appetites of users quickly push those plans into obsolescence. Besides the inevitable cry for power and memory, the second part of our reader survey pinpoints one area in dire need of improvement: the user interface. Though slightly more than half the respondents admit that their current systems are sufficient, their expectations for the next three to five years demand greater heights of computational speed, storage, and graphics.

Cover: 1-ns static RAM 157

The blazing speed of today's computers means that memories must keep pace. Quick as they are, today's silicon static RAMs will not be able to satisfy the performance needs of future computers, but a gallium arsenide static RAM, cycling in 1 ns and storing 1 kbit, is positioning itself as a successor. After all, every nanosecond saved in RAM access time typically means an equal saving in machine cycle time.

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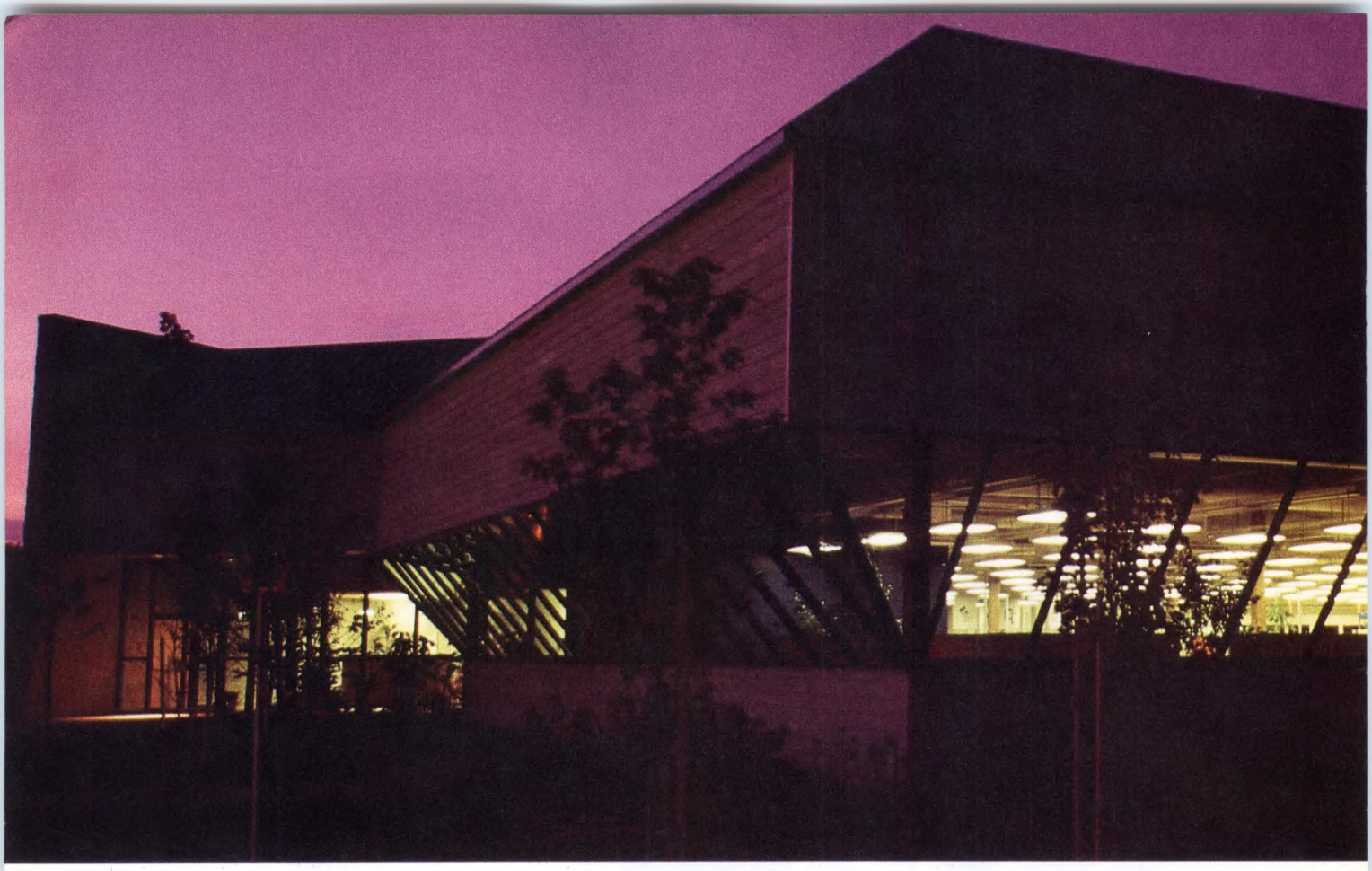

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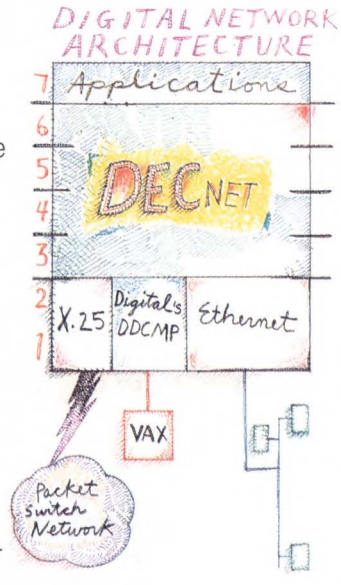

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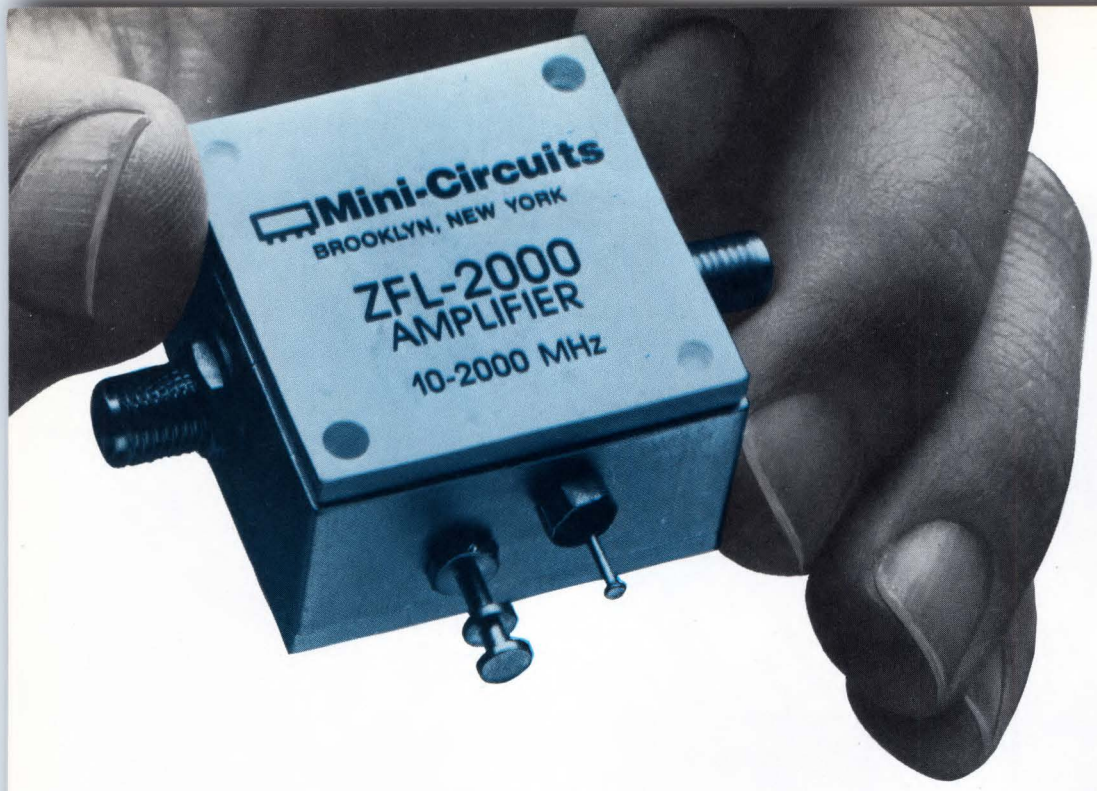

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- Creating multiple output ports for one signal generator when amplifying and then adding a Mini-Circuits power splitter or divider.

These unconditionally stable wideband amplifiers are available with SMA connectors and are housed with an internal heat sink in a rugged 1.25 in. sq. by 0.75 in. high RFI shielded case.

Meets MIL-STD 202, these units operate from −55°C to +100°C.

One week delivery and a one-year guarantee, of course.

For complete specifications and performance curves refer to the Goldbook, EEM, EBG, or Mini-Circuits catalog

ZFL-2000 SPECIFICATIONS

FREQUENCY	10-2000 MHz
GAIN	20 dB
GAIN FLATNESS	±1.5 dB
OUTPUT POWER (1 dB compression)	+17 dBm
NOISE FIGURE	7.0 dB
INTERCEPT POINT (3rd order)	25 dBm
VSWR, 50 OHMS	2:1
DC POWER volt, current	+15 V, 100 mA
HEAT SINK	Internal
OPERATING TEMP	−55°C to +100°C

CIRCLE 7

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C98 REV. A

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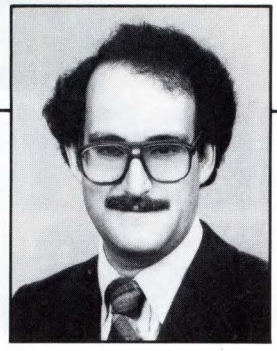


Already in short supply, the airwaves demand more careful allocation

For a society accustomed to an abundance of resources, it comes as quite a shock that certain commodities are in short supply. For communications, the electromagnetic spectrum has practical limits that are quickly being reached by its users—commercial, government, military, and civilian interests.

In a recent petition for rulemaking (RM-4829), the Land Mobile Communications Council (LMCC) asked the FCC to consider reallocating or sharing present uhf television channels to help relieve spectrum congestion. The industry group also asked for space now used by other interests, including the federal government, as well as the release of 32 MHz—now held in reserve for future mobile use.

As in business, where the bottom line is often boosted by limiting expenses as well as increasing sales, the spectrum problem may profit from a similar strategy—compressing signals into narrower bandwidths and searching for better ways to allocate space among users. Technically, impressive strides have been made in the past ten years. Digital communications especially has benefited from such spectrum-efficient techniques as packet radio, which allows several users to communicate concurrently on a single frequency. Encouraging advances are also being made in such frequency-conserving techniques as amplitude-compandored sideband and cellular radio.

But the land mobile industry is forecasting a need for considerably more frequencies than are currently allotted. Due to the practical limits of equipment design and propagation characteristics, some of those frequencies may have to come from users who cannot show a public good arising from the space they occupy or cannot demonstrate that they have been working toward reducing the bandwidth of their signals.

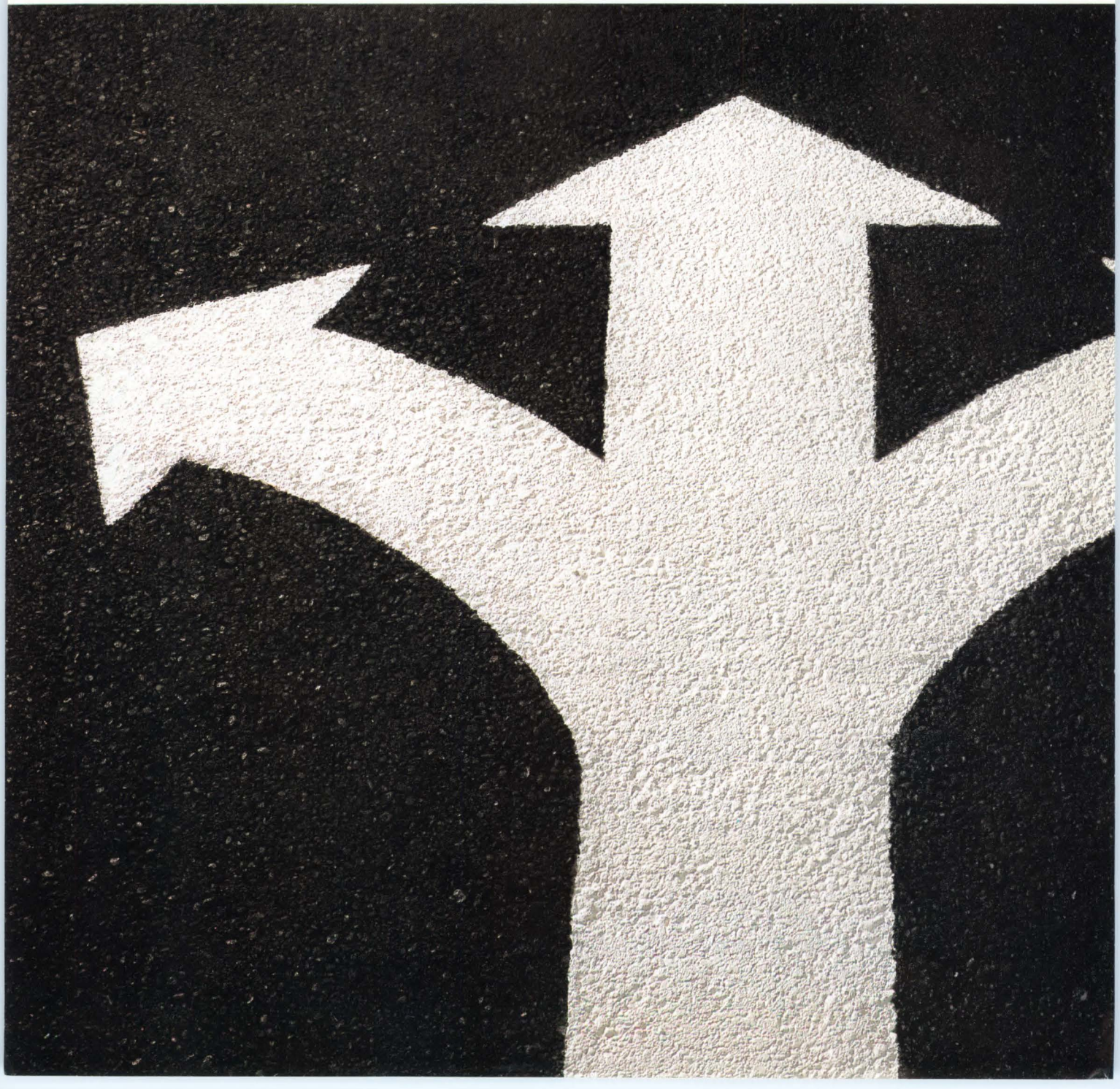
Television broadcasters are particularly vulnerable to a frequency attack, since they hold some 408 MHz of spectrum below 1 GHz, the only area that the LMCC considers appropriate for mobile communications. Indeed, TV broadcasting occupies 72 MHz—(about 27%) of the vhf range, which is ideal for mobile radio because of its good local coverage. Yet, while the vhf range is quickly eaten up, many uhf TV frequencies stay reserved but unused. Although new circuit designs have made uhf television receivers more sensitive and easier to use, broadcasters seem disinclined to vacate the vhf range for uhf assignments.

Condensing signals in both the time and frequency domains solves part of the dilemma, but the thorniest problem lies in reallocating frequencies fairly and equitably. Alas, the spectrum is not influenced by engineers alone but by governmental agencies, such as the FCC, and economic interests, such as the broadcasting industry. Thus the mood in Congress or such economic factors as the cost of new equipment could force decisions that run counter to sound technical advice for long-range spectrum use.

The issue may worsen as the land-mobile community sharpens lobbying skills and gains economic clout. Broadcasters should consider the consequences of a possible protracted confrontation with mobile-radio users versus an orderly move to uhf frequencies.

Harold Winard

HERE'S EXACTLY WHERE YOU CAN GO WITH THE 82586 LAN COPROCESSOR.



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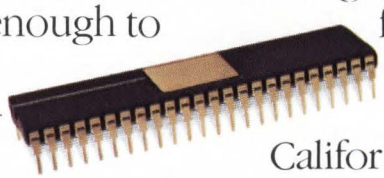
Networking needs are as diverse as city streets and eight-lane highways. So it's a turn for the better that office LAN standards are emerging: IEEE 802.3/Ethernet, Cheapernet and IBM* PC Network.

And even though all three networks are different, they have one thing in common:

Intel's 82586 LAN Coprocessor, the only programmable LAN chip.

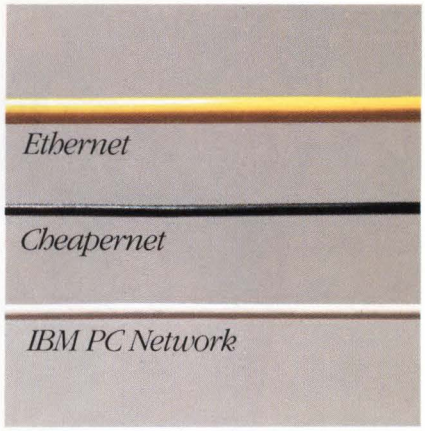
Because it's programmable, you have the flexibility to implement any of these office networks. With the 82586, you won't have to relearn a new chip every time the market takes a turn. You choose the office network and the 82586 is flexible enough to support it.



In addition to its unique programmable features, the 82586 eases your LAN design effort.

Its high level command interface performs datalink functions which means there's no low level software to write.

The 82586's diagnostic features such as loopback and self test,



make it easy to debug your system during development.

And the 82586 is designed to work with Intel's highly integrated microprocessors like the 8-bit 80188 and the 16-bit 80186. So you can keep your chip count down, which saves time and eases your design effort.

Find out more about the 82586 and how Intel can support your LAN design efforts. For our free brochure, call toll free: (800) 538-1876. In California, (800) 672-1833. Or write Intel Corporation, Lit. Dept. W-41, 3065 Bowers Ave., Santa Clara, CA 95051.

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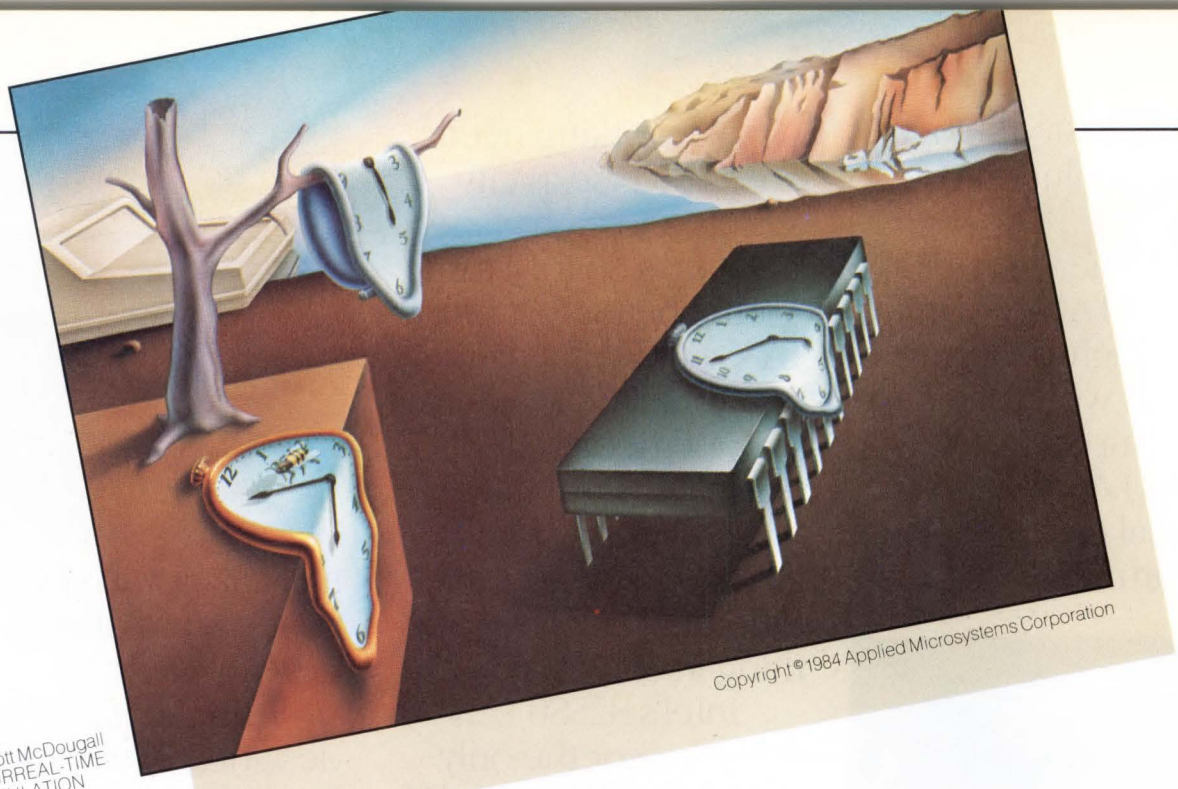

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Scott McDougall
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MYTH 2

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CIRCLE 8

READER FEEDBACK

Sputtering goes into volume production

I must take exception to a statement attributed to Cyberdisk in your News Analysis, "Sputtering, Plating Vie for High Bit Densities on Winchester Disks" [Nov. 15, p. 65]. The story states: "Cyberdisk and Domain agree that it may be years before the [sputtering] process is fine-tuned enough for volume production."

On the contrary, Cyberdisk believes that sputtering has arrived as a viable production process. In fact, next month we are beginning volume production of both 5¼- and 3½-in. sputtered media on aluminum and glass substrates. We will be using custom continuous in-line planar magnetron sputtering systems.

Virgle Hedgcoth
Vice President, Operations
Cyberdisk Inc.
Anaheim, Calif.

A choice of lengths, too

The article "Highest Capacity 8-In. Drive Presents Choice of Interfaces" in the Nov. 15 issue [p. 271] provides an interesting comparison of features between the SCSI and SMD interfaces, but I would like to clarify one point.

Mr. Czernek implies on p. 273 that the SCSI allows cable lengths of only 20 ft. As he states, the reason is that the drivers are typically designed with single-ended open-collector transistors. However, the proposed ANSI SCSI standard allows implementation of either single-ended or differential alternatives. The differential alternative permits cable lengths of up to 25 meters (82.5 ft).

It is true that the availability of drivers and receivers for the differential alternative is currently limited. This limitation is due primarily to the small demand in the marketplace for such devices and not because of the proposed SCSI standard or because of a lack of technology.

David A. Strawser
Methode Electronics Inc.
Datamate Division
Chicago, Ill.

A matter for mirth and concern

I note, with both mirth and concern, the contents of the Newsfront story entitled "Electron Microscope Takes a Peek at Logic Levels inside Working IC," which appeared on p. 50 of the Nov. 15 issue.

My mirth is caused by the statement that the voltage-contrast process was developed by scientists at Bell-Northern Research Ltd. In fact, this technique is at least 15 years old, having been used in the early days of scanning microscopes to investigate the function of early inte-

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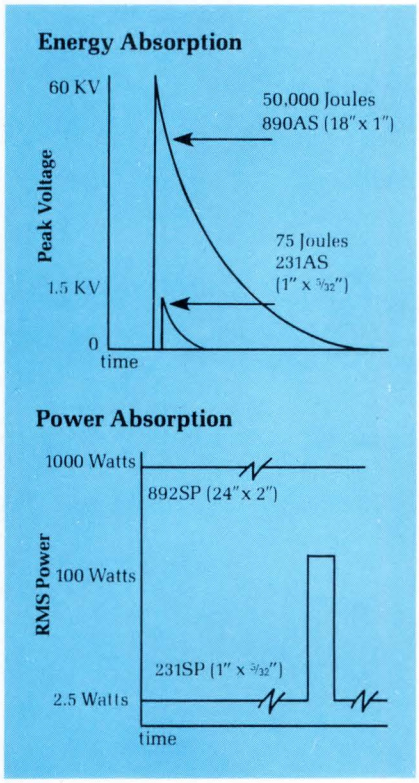

Regardless of the pulse shape, we have the resistor. Our Type SP handles large amounts of power from 60 cycles through VHF. Type AS can absorb huge amounts of energy in millisecond pulses. Type A solves high resistance problems in high voltage situations.

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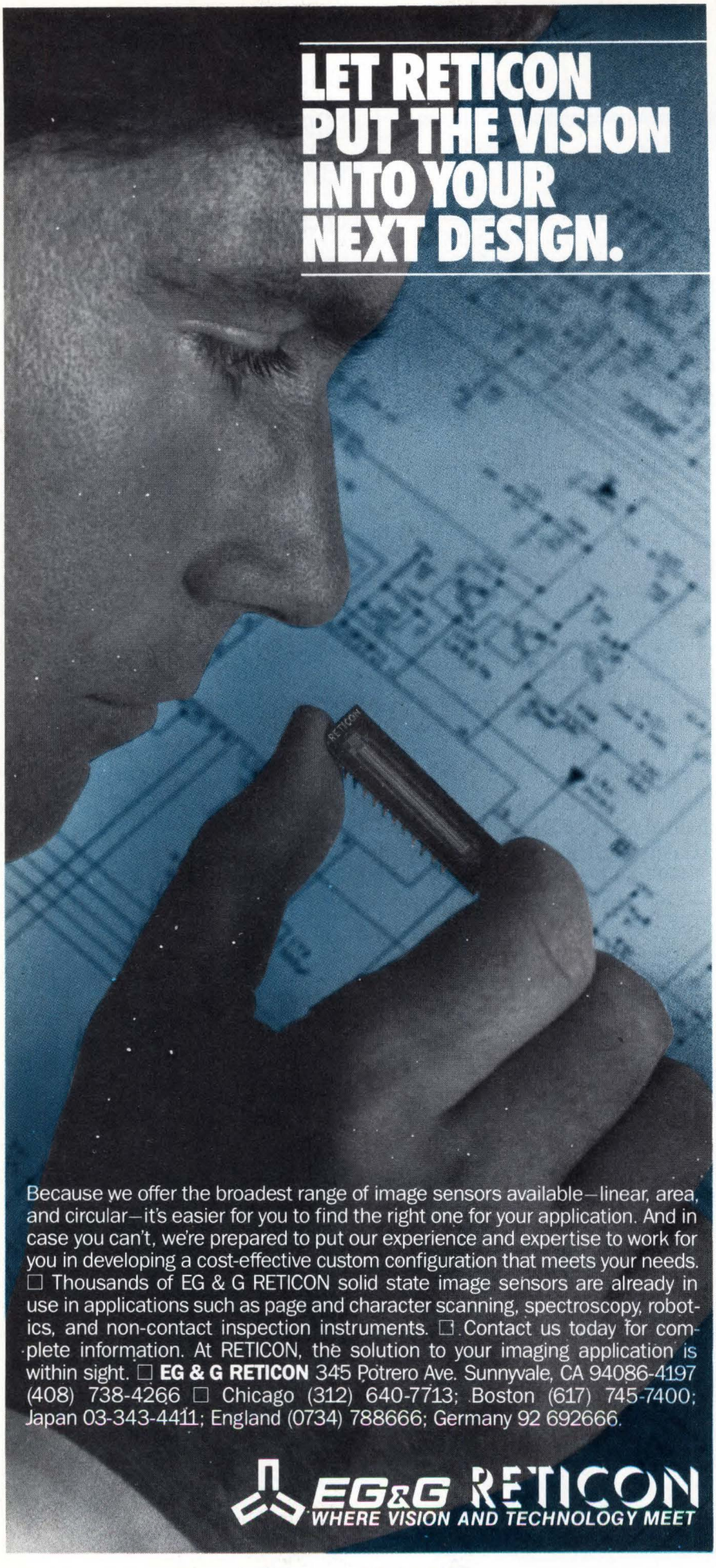
CIRCLE 9



CIRCLE 10

grated circuits (though not on a stroboscopic basis).

My concern arises because at least a score of others have already reported significant work in the use of sampling techniques in combination with voltage contrast to inspect and find faults in ICs. The name of some of these companies will be familiar to you: Hitachi, IBM, ITT, Siemens, Sony, ...

Furthermore, there are products that are designed to do what is described in this story, and they have been sold in the commercial marketplace for a number of years. I saw an early demonstration of one of these products about two years ago.

Arnold Frisch
Chief Electronic Engineer
Tektronix Inc.
Beaverton, Ore.

Correction

The switch manufacturing division of Eaton Corp., Aerospace & Commercial Controls, was omitted from the Directory of Manufacturers accompanying our Aug. 23 Product Report, "Focus on Subminiature Switches" (p. 301). The division produces a complete line of Cutler-Hammer subminiature switches, including pushbutton, rocker, paddle, toggle, and pc-mounted types.

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor, Electronic Design, 10 Mulholland Dr., Hasbrouck Heights, N.J. 07604. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

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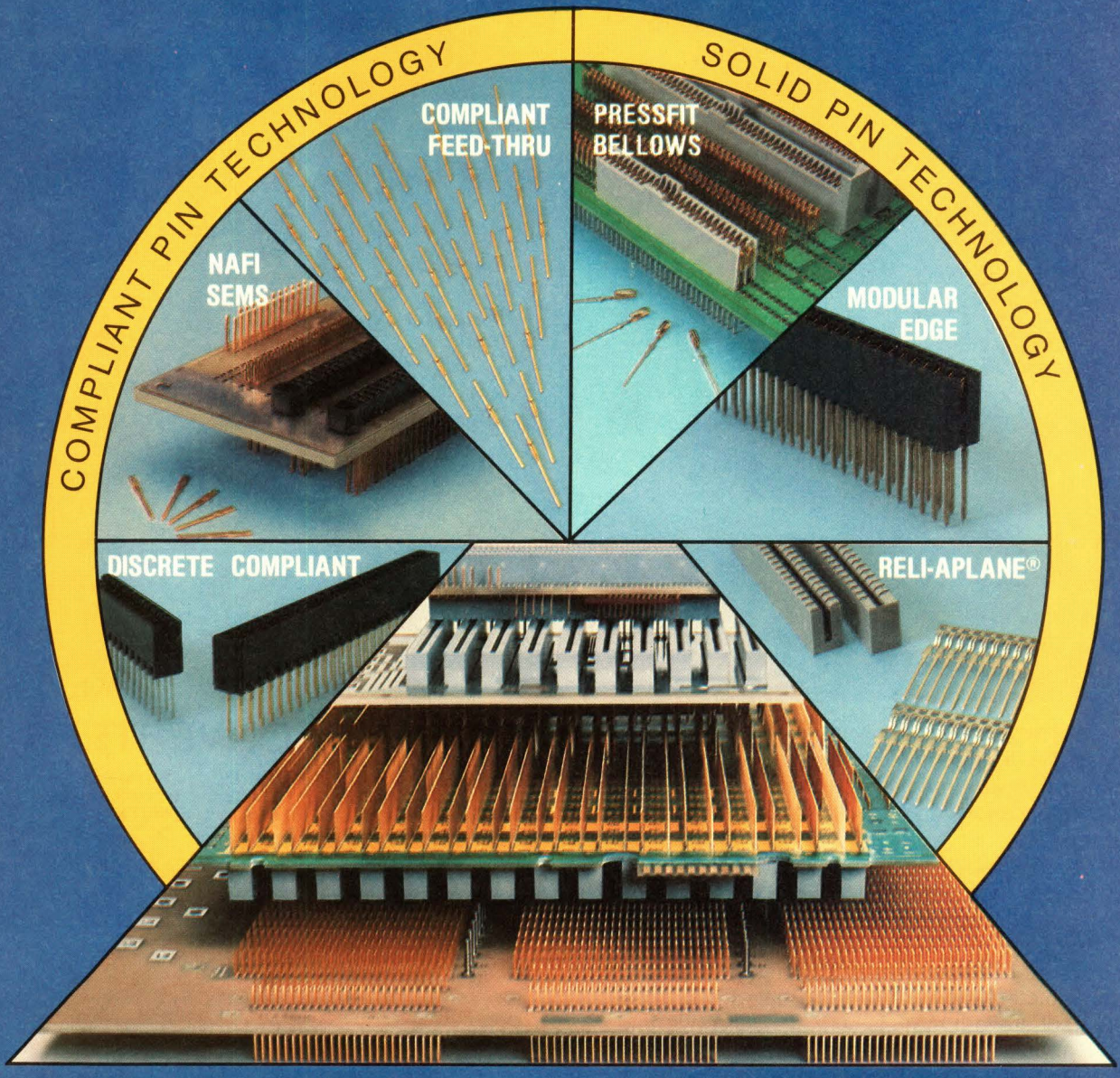

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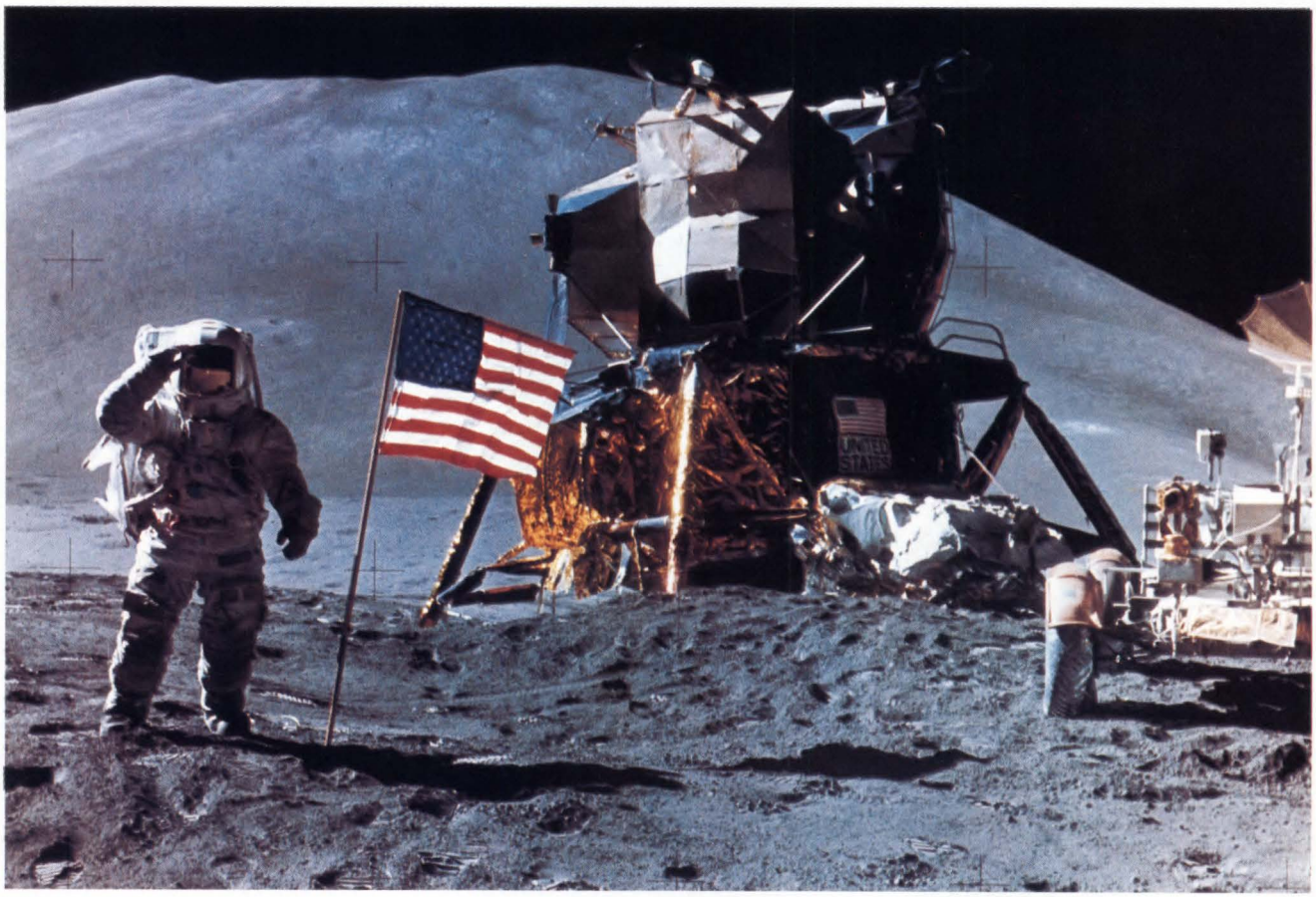

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MODEL	TYPICAL MTBF*	OUTPUT VOLTAGE RANGE	OUTPUT POWER RANGE (WATTS)
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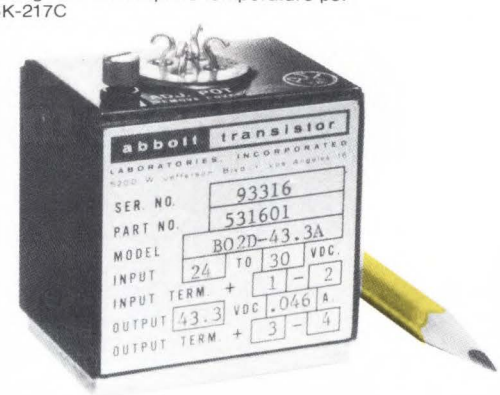
CC	176,000	±3-±30	3-20
B	626,000	5-500	2-170
BN	112,000	5-48	25-100

*Ground benign 50°C baseplate temperature per MIL-HDBK-217C



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CIRCLE 11

U.S. MEETINGS

1985 International Winter Consumer Electronics Show, Jan. 5–8. Las Vegas, Nev. Dennis Corcoran, CES, 2001 Eye St. NW, Washington, D.C. 20006; (202) 457-8700.

PC Fab Expo '85, Jan. 8–10. Sheraton Twin Towers Hotel, Orlando, Fla. Julia Wilson, PMS Industries, 1790 Hembree Road, Alpharetta, Ga. 30201; (404) 475-1818.

Automated Test Equipment West Conference (ATE), Jan. 14–17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (212) 340-9780.

Caldon West '85, Jan. 14–17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (800) 782-0009.

1985 Measurement Science Conference, Jan. 17–18. Marriott Hotel, Santa Clara, Calif. Darlene Diven, Lockheed Missiles and Space Co., PO Box 3504, Sunnyvale, Calif. 94088; (408) 756-0270.

Uniform, Jan. 21–25. Infomart, Dallas, Texas. Pemco, Inc., 2400 E. Devon Ave., Suite 205, Des Plaines, Ill. 60018; (800) 323-5155.

Rf Technology Expo '85, Jan. 23–25. Disneyland Hotel, Anaheim, Calif. K. Kriner, Cardiff Publishing, 6530 S. Yosemite St., Englewood, Colo. 80111; (303) 694-1552.

1985 Society for Computer Simulation (SCS) Multiconference, Jan. 24–26. Bahia Hotel, San Diego, Calif. SCS, PO Box 2228, La Jolla, Calif. 94038; (619) 459-3888.

Communication Networks Conference and Exposition, Jan. 28–31. Washington Convention Center, Washington, D.C. Louise Myerow, CW/Conference Management Group, 375 Cochituate Road, PO Box 880, Farmingham, Mass. 01701; (617) 879-0700 or (800) 225-4698.

Mini/Micro West, Feb. 5–7. Anaheim Hilton Exposition Center, Anaheim, Calif. Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

Conference on Optical Fiber Communication(OFC '85), Feb. 11–13. Town and Country Hotel, San Diego, Calif. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

IEEE International Solid-State Circuits Conference, Feb. 13–15. New York Hilton Hotel, New York, N.Y. Lewis Winner, ISSCC, 301 Almeria, Coral Gables, Fla. 33134; (305) 446-8393.

Integrated Machine Loading/Material Handling Systems Seminar, Feb. 19–21. Holiday Inn Livonia-West, Detroit, Mich. John R. McEachran, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, Ext. 382.

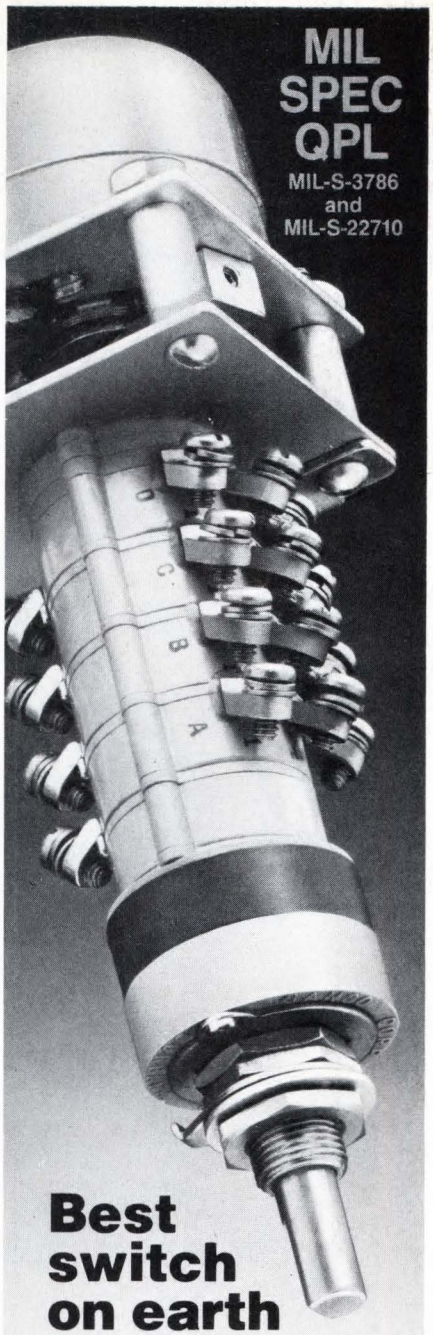
Automated Design and Engineering for Electronics Conference and Exhibition (ADEE), Feb 26–28. Anaheim Hilton and Towers, Anaheim, Calif. Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Ave., PO Box 5060, Des Plaines, Ill. 60018; (312) 299-9311.

Nepcon West '85, Feb. 26–28. Convention Center, Anaheim, Calif. Nepcon West '85, 1350 E Touhy Ave., Des Plaines, Ill. 60018; (312) 299-9311.

American Institute for Design and Drafting (AIDD) Exposition, March 3–8. Albert Thomas Convention Center, Houston, Texas. Philip Nowers, AIDD National Headquarters, 901 N. Washington St., Suite 509, Alexandria, Va. 22314; (703) 548-1263.

Interface '85, March 4–7. Georgia World Congress Center, Atlanta, Ga. The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

(continued on p. 21)



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CIRCLE 12

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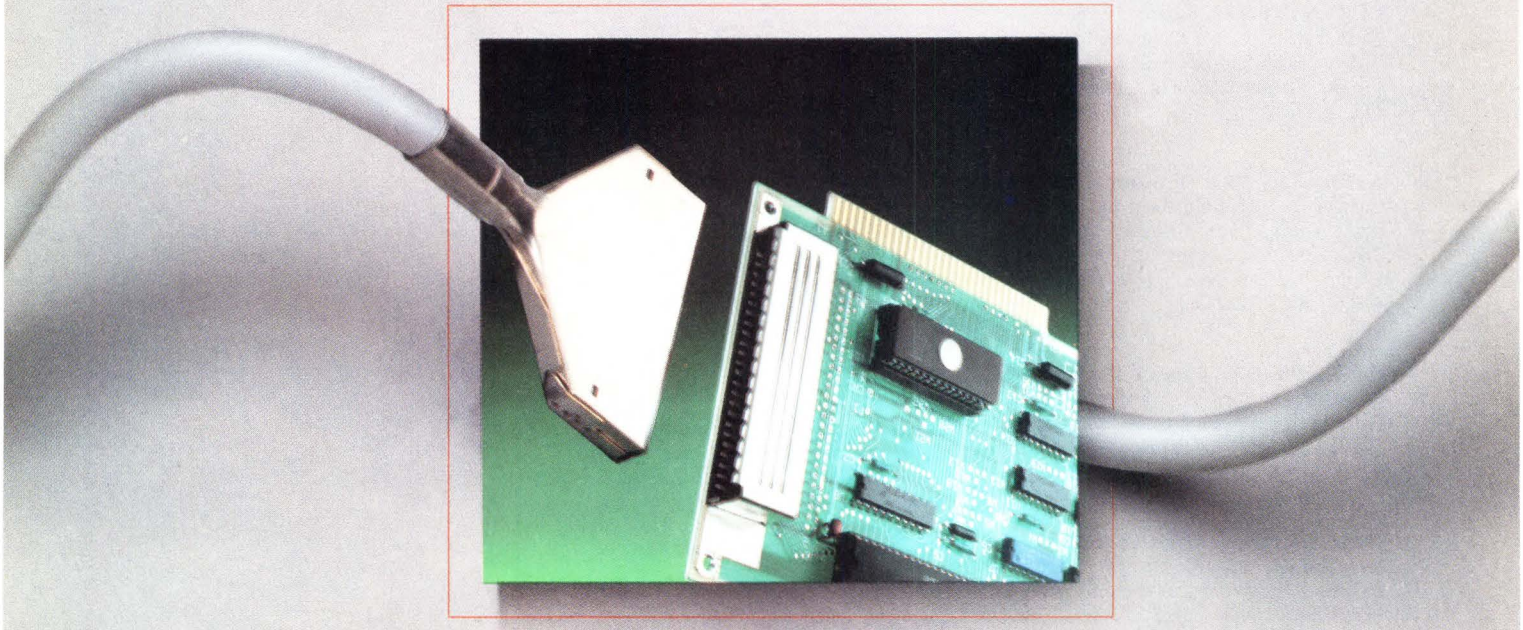

to any peripheral.

Presenting SCSI. Small Computer Systems Interface. An interface standard that lets you connect small computers with virtually any peripheral device — even those still on the drawing board. Without overhauling your hardware and software. So the best can go with the best, period — not the best of what's compatible.

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CIRCLE 13

U.S. MEETINGS

(continued from p. 19)

Southcon '85 and Mini/Micro Southeast, March 5–7. Georgia World Congress Center, Atlanta, Ga. Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

Integrated Services Digital Networks Exposition (ISDN '85), March 6–8. Bally's Park Place Casino Hotel, Atlantic City, N.J. Joan Barry, Information Gatekeepers Inc., 214 Harvard Ave., Boston, Mass. 02134; (617) 232-3111.

National Design Engineering Show & ASME Conference, March 11–14. McCormick Place, Chicago, Ill. National Design Engineering Show, 999 Summer St., Stamford, Conn. 06905; (203) 964-8287.

1985 ACM 13th Annual Computer Science Conference (CSC), March 12–14. New Orleans Marriott Hotel, New Orleans, La. Della T. Bonnette, Computing & Information Services, University of Southwestern Louisiana, Lafayette, La. 70504; (318) 231-6306.

Picosecond Electronics and Optoelectronics Meeting, March 13–15. Hyatt Lake Tahoe, Incline Village, Nev. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

International Computer and Telecommunications Conference (Comtel '85), March 18–20. Infomart, Dallas, Texas. Comtel '85, 5080 Spectrum Drive, Suite 707E, Box 17, Dallas, Texas 75248; (214) 631-6482.

Robotic End Effectors: Design and Applications Seminar, March 19–20. Holiday Inn Livonia-West, Livonia (Detroit), Mich. John McEachram, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, ext. 382.

Second Annual International Conference on Artificial Intelligence for Robotics, March 21–22. Stouffers Concourse, Crystal City, Arlington, Va. Dr. Diener, IIT Research Institute, 10 W. 35th St., Chicago, Ill. 60616; (312) 567-4376.

1985 Eastern Similation Conference (ESC), March 24–29. Williamsburg Hospitality House, Williamsburg, Va. Charles A. Pratt, SCS, PO Box 2228, La Jolla, Calif. 92038; (619) 459-3888.

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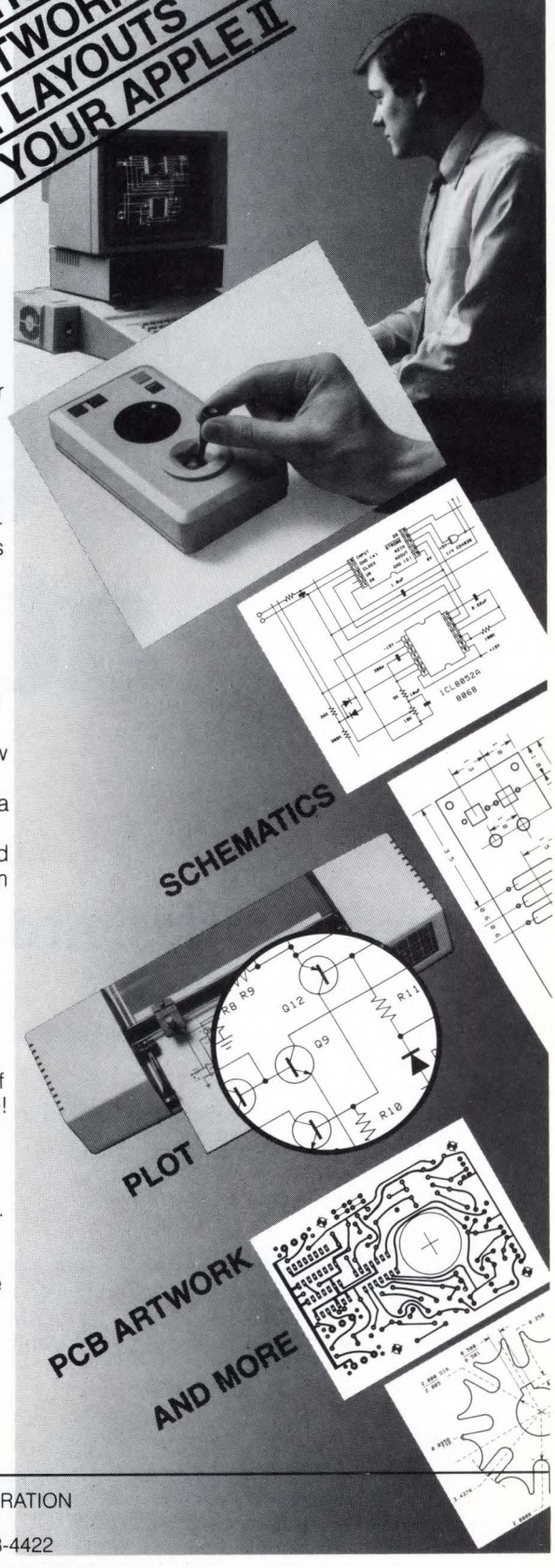

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*Freq. (MHz)	Atten. Tol. (Typ.)	Atten. Change, (Typ.) over Freq. Range		VSWR (Max.)	
		DC–1000	1000–1500	DC–1000 MHz	1000–1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

*DC–1000 MHz (all 75 ohm or 30 dB models) DC-500 MHz (all 40 dB models)

MODEL AVAILABILITY

Model no. = a series suffix and dash number of attenuation.
Example: CAT-3 is CAT series, 3 dB attenuation.
■ denotes 75 ohms; add –75 to model no.
● denotes 50 ohms

ATTEN	SAT (SMA)	CAT (BNC)	NAT (N)	TAT (TNC)
1	●	●	●	●
2	●			
3	●	●■	●	●
4	●			
5	●			
6	●	●■	●	●
7	●			
8	●			
9	●			
10	●	●■	●	●
12	●			
15	●			
20	●	●■	●	●
30	●	●	●	●
40	●	●	●	●

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CIRCLE 15

C 92 REV. A

PERSONALLY SPEAKING

Keep a watchful eye on single boards for IBM PC look-alikes

Let's face facts: the shakeout in personal computers has left the software and hardware for the IBM PC family in the enviable position of being nearly defacto standards. As a result, a number of design projects are under way with the express aim of creating compatible machines with a single board. These efforts, coming largely from start-up companies, mean more than just smaller machines; they promise smaller price tags as well.

By turning to highly integrated CMOS gate arrays, denser memories, and microprocessors and their peripherals, it's possible to trim the IBM PC's hardware from three boards down to one. In the process, a great deal of discrete TTL circuitry and several high-performance MOS chips can be left by the wayside. In fact, as few as three arrays—packed with several thousand gates each—can stand in for nearly 80 low-power Schottky TTL circuits, as well as the chips that make up the computer's parallel I/O, clock generator, and keyboard and printer ports.

There will be an even greater use of CMOS gate arrays in the board-level subsystems that are now on the drawing boards for the IBM PC XTs and PC ATs. Standard cells will also be putting in an appearance. Allowing more flexibility than gate arrays, the cell approach can potentially do away with most of the personal computer's discrete logic—shrinking a single-board computer even more. But the high-current buffer circuitry needed for bus drivers doesn't lend itself to such neat solutions. For the foreseeable future, the PC will continue to implement it in bipolar logic.

Also squeezed onto the same board will be the 256-kbit dynamic MOS RAMs that are now making the scene. These chips are coming just in nick of time. As more challenging jobs are assigned to personal computers, a minimum of 1 Mbyte of memory becomes a must and 2 to 8 Mbytes sound more realistic. On top of that, software in silicon, which incorporates an operating system in ROM or EPROM, is memory hungry.

Designers also are keeping a close watch on the world of 32-bit microprocessors. Any chip that includes memory management, for example, would be worth far more than its weight in gold.

Surface-mounting can further save board real estate. Hard-disk controllers and high-resolution graphics, to name only two functions that call for an additional card, are ideal candidates for surface mounting. That way, both the cards and their connections are eliminated.

PCs will move into now unfamiliar territory, like factory automation and integrated engineering workstations. Until now both have depended on supercomputers to takle the more difficult back-end design problems.

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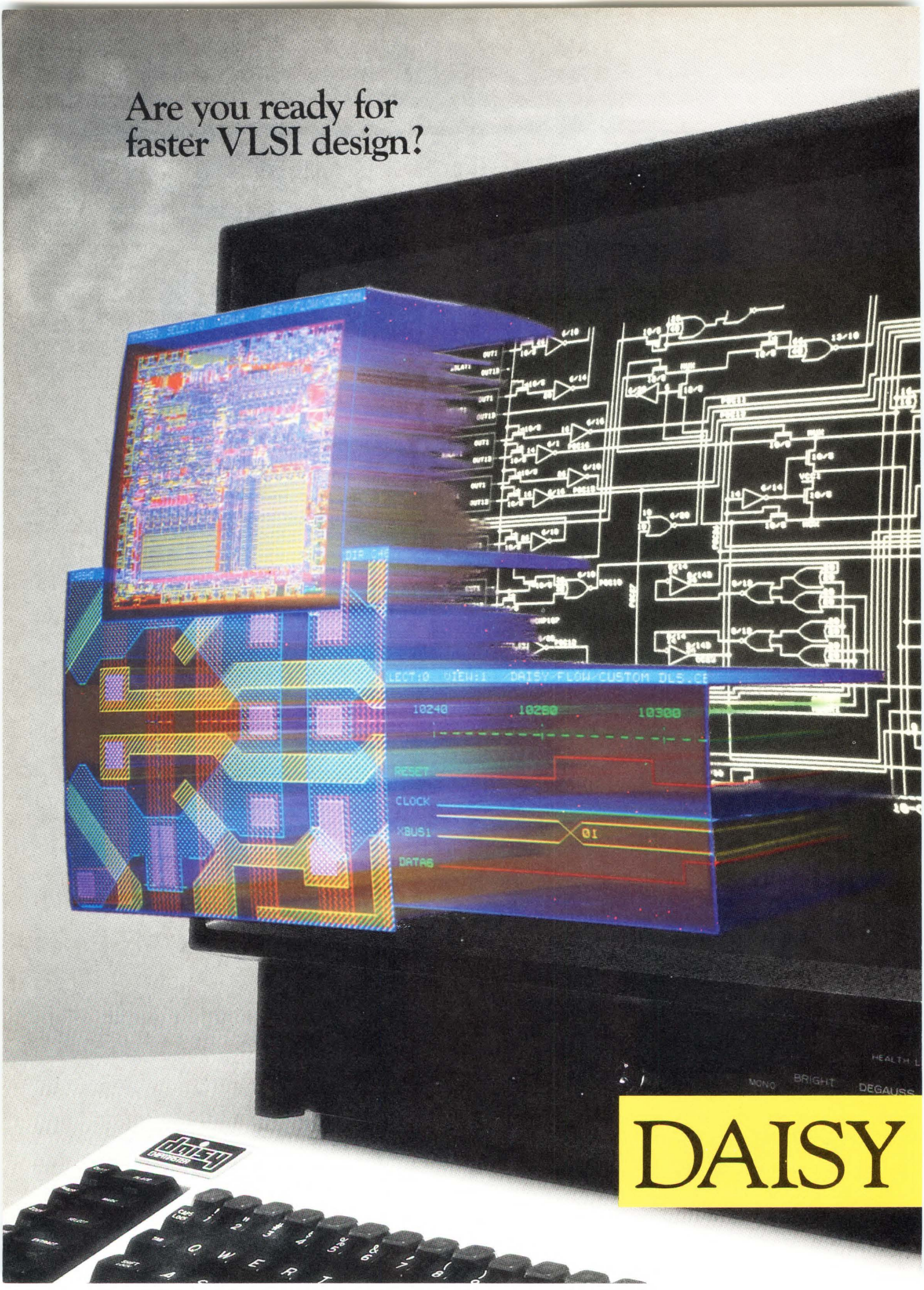

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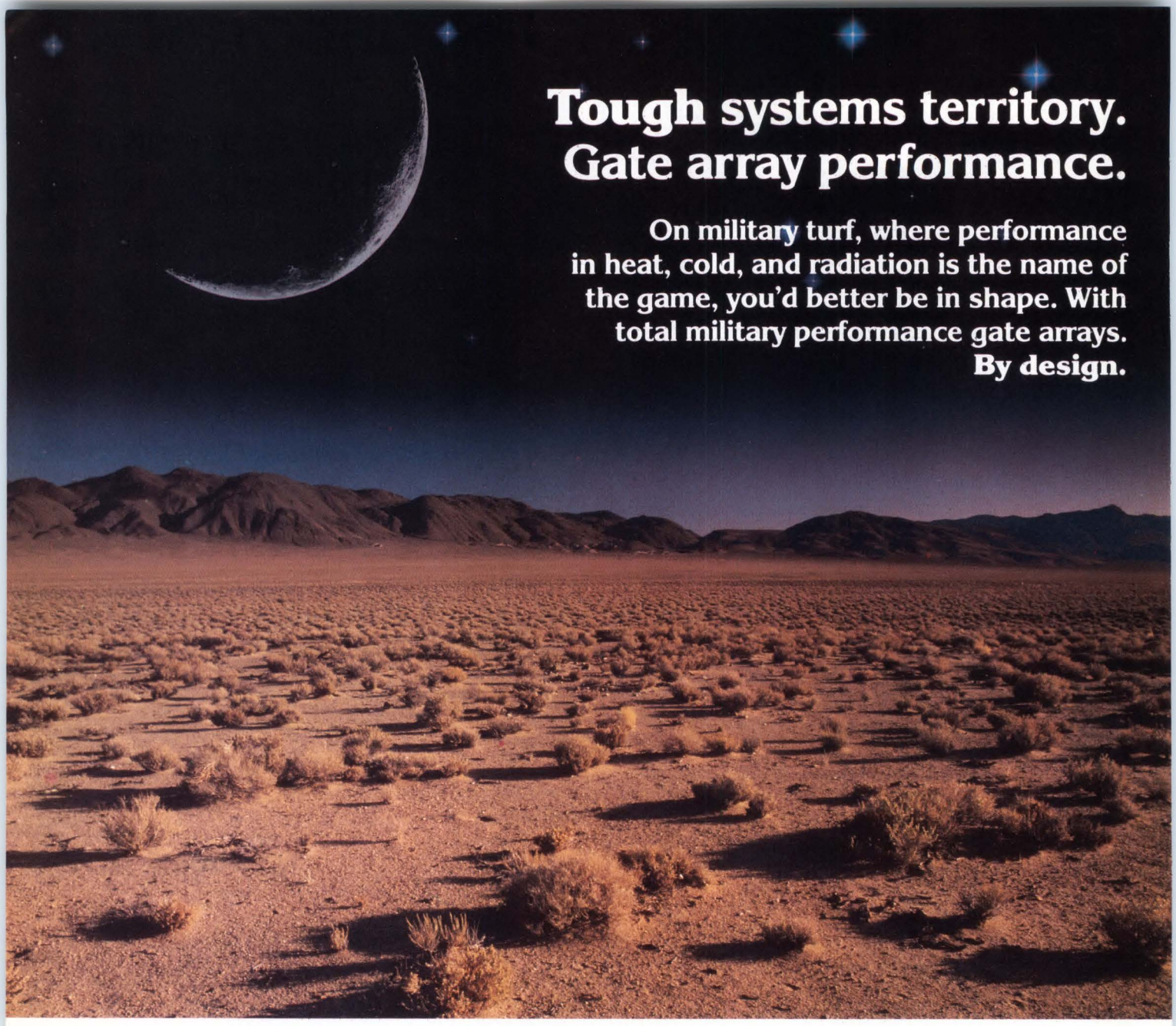

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CIRCLE 17

NEWSPULSE

Alloy puts erasable optical disks 'in the pink'

A thin-film alloy that changes color when heated may make erasable optical disks standard fare. The silver-zinc compound, developed by Hitachi Ltd. (Tokyo), turns pink when it is heated above 300°C; reheating it to between 100° and 300°C returns it to its original color. Using a semiconductor laser, data can be written without burning pits into the recording medium, and any portion of the disk can be erased simply by reversing its color. The company expects to use the alloy in video and file-memory systems.

PC XT handles the phones, screens callers

The first voice-store-and-forward application generator for the IBM PC XT gives the machine the power to record messages from telephone lines, verbally annotate local text files, and positively identify callers. SoundWare, from Digital Pathways Inc. (Palo Alto, Calif.), comprises a plug-in board and a series of software tools stored on a separate disk. The board carries a telephone line transformer and a combination analog-to-digital and digital-to-analog converter, which works with adaptive delta pulse-code modulation (ADPCM). The converter transforms speech into a digital stream that is passed through the PC to the hard disk, and vice versa. The software enables the computer to handle a number of voice and data-terminal tasks. Until now, such jobs could be tackled only by minicomputer-driven terminals.

Universities to get $25 million for materials research

Impelled by the need for new materials and a better understanding of existing ones at the atomic level, IBM Corp. (Armonk, N.Y.) will donate $25 million for research to a dozen universities across the country over five years. Graduate-level programs will focus on developing an extremely flat and smooth material—perhaps a new ceramic—which may well become a critical element in new computer components, particularly those involving high-speed switching. As for existing materials, the aim will be to gain a better understanding of how unlike substances interact. Of course, none of these things will be useful unless the project also explores new processing techniques, advanced instrumentation, and packaging and interconnection technologies. Information gathered from the research will be available to the public.

Each university will be awarded up to $1 million for expenses and another $1 million in IBM equipment and software. Interested universities should submit an initial short proposal to IBM Corp., Old Orchard Road, Armonk, N.Y. 10504, by April 2. Grants will be made early in 1986.

200-MHz video generator tackles CRT system development

Designers of high-speed, high-resolution monitors and terminals will get a big assist from a video signal generator that works at up to 200 MHz—nearly twice the bandwidth of current displays. The Opix box, from Quantum Data Inc. (Carol Stream, Ill.), proves a versatile development tool: It can fill screens with

NEWSPULSE

text, graphics, or both, emulating various pixel resolutions, scanning frequencies, and video bandwidths. Based on a 68000 microprocessor and some fast digital-to-analog converters, the generator stores the frames in a battery-backed RAM, so that terminal designers can compare them during development.

Infrared light builds cableless local network

With cable-based local networks currently the norm, one that shuns cables in favor of infrared light is sure to make a big hit. The unusual system bounces infrared light off walls and ceilings, thereby eliminating the need for direct transmission paths between sending and receiving nodes. The network, devised by Becos Industries Inc. (Campbell, Calif.), can handle as many as 99 channels, sending data at a rate of 400 kbits/s. The network might well find its primary application in open offices that use modular partitions to separate work areas.

EIA sets standards for voltage levels and packaging

The operating-voltage levels of the next generation of VLSI circuits and the pinout conversions between DIPs and leaded chip carriers have been spelled out by the Electronic Industries Association (Washington, DC). JEDEC Standard 8-1 defines a set of interface levels that allow 5-V TTL ICs and 3.3-V devices to be mixed without buffers or level shifters. JEDEC Standard 11 establishes criteria for going from DIPs to 20- or 28-pin leaded chip carriers for CMOS digital logic circuits.

Those interested should contact the Electronic Industries Association, 2001 Eye Street, Washington, DC 20006; (202) 457-4981.

Cosmic Cube matches the prowess of supercomputer

Though it has roughly one-tenth the power of the Cray-1, the so-called Cosmic Cube—a 64-node parallel processor—has proved the supercomputer's equal. Designed and built by researchers at the California Institute of Technology, the Cube showed its mettle by working out high-order physics problems that until now have only been solved using the supercomputer. Each of the parallel processor's nodes is fitted with a 16-bit 8086 and 8087 and 136 kbytes of RAM—approximately equal to that of an IBM PC personal computer. The system executes programs concurrently, using a network based on a six-dimensional cube, and comes in at about one-hundredth the cost of the Cray.

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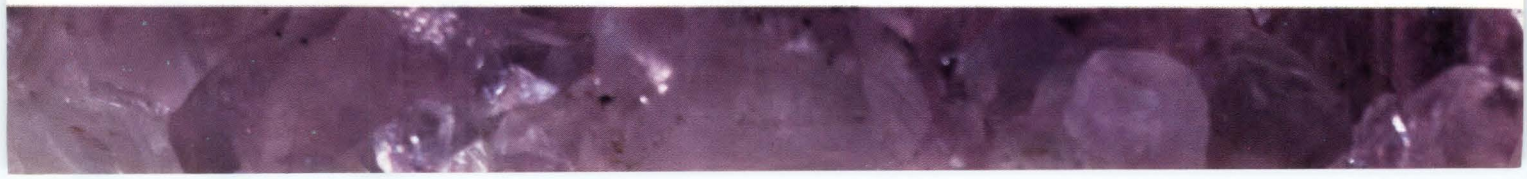

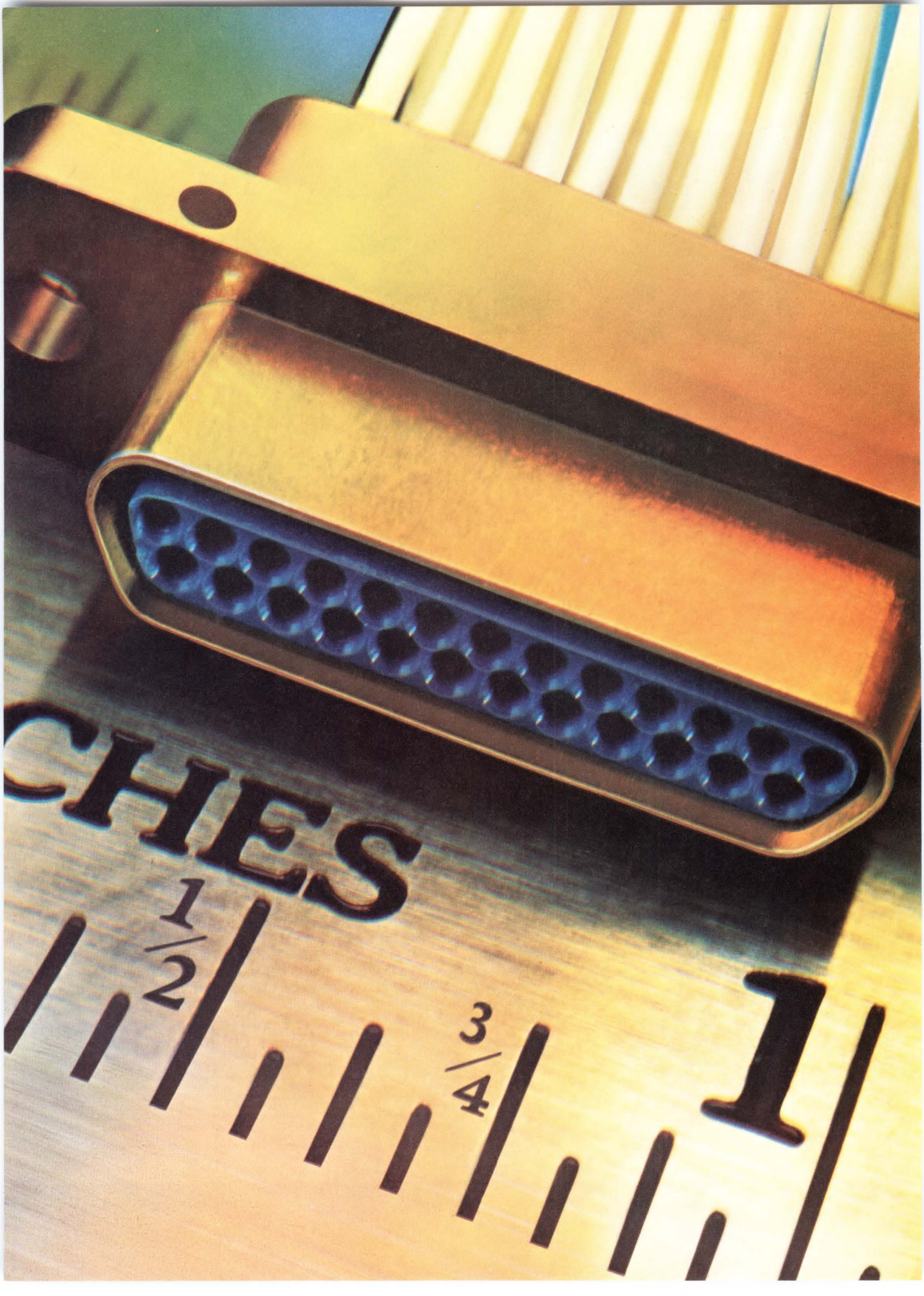
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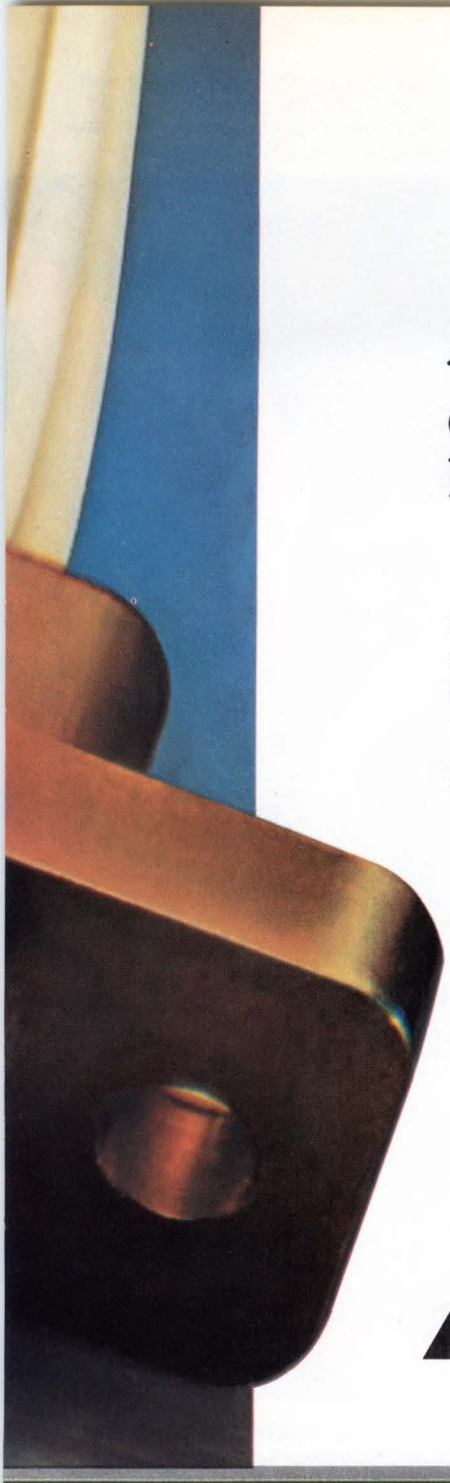

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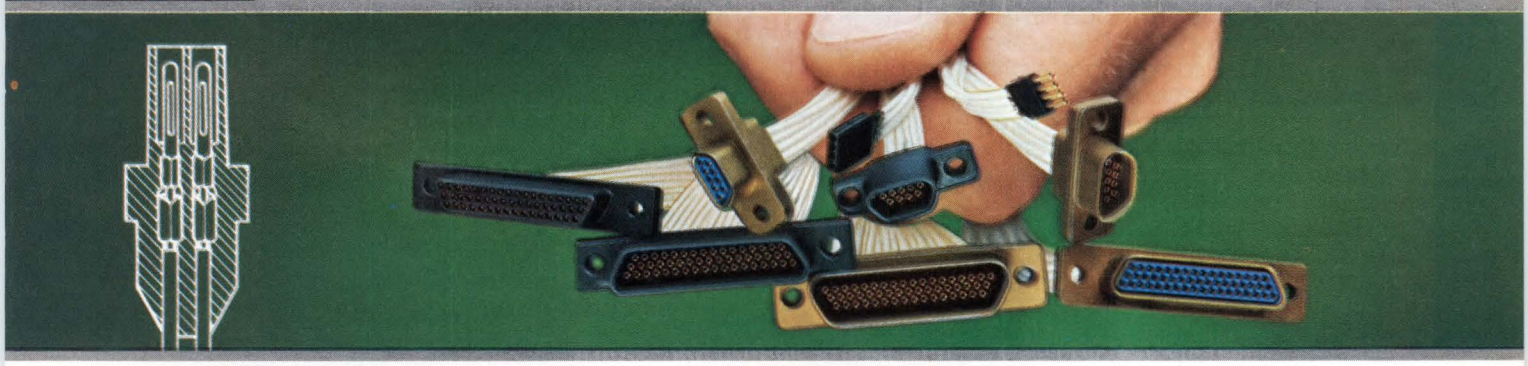

Available in both metal and plastic configurations, only AMP Micro Series 50 connectors have positive lead-in pin and socket contacts to avoid stubbing.

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SOLVING THE MYSTERY OF THE BLUE SKY PHENOMENON.

This is the 2nd in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.

In the microprocessor world, the "Blue Sky Phenomenon" refers to microprocessor development code crashes. The code simply and quite mysteriously disappears. The most common culprits are bugs. And the fact is, simple program bugs will crash most microcomputers.

The hosts for some of these bugs have famous names. What they all have in common is an absence of mechanism to protect against crashes. There is one exception.

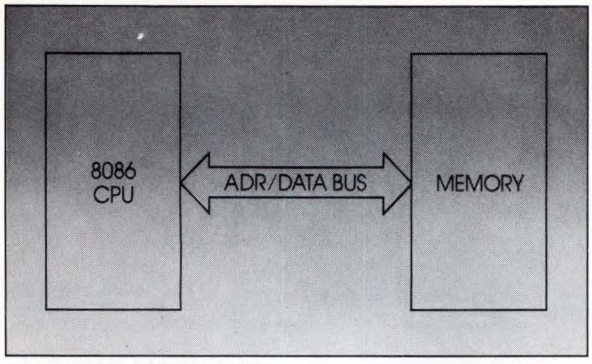
The Zilog Z8000® family provides comprehensive hardware protection to help create systems that are resistant to system crashes so common in primitive architectures. The Z8000 CPU is not only more reliable in this sense, but it's easier to learn how to use. Especially if you already know how to use the ubiquitous Z80® CPU.

LOST IN THE WILD BLUE YONDER.

There is a technological reason why some microprocessors are so prone to corruption. It stems from the direct connection of the memory to the processor. Without any checking hardware between the processor and memory, the processor can change any area in its memory at will—without regard to the consequences. Such a lack of restrictions allows illegal operations such as changing program memory stack underflow (running the stack into the data area), and even modifying the code of the operating system. This lack of appropriate technology has two glaring results:

- Illegal operations cannot be detected before damage has occurred.
- Any damage to the program and data cannot be undone.

There are far-reaching implications for a lack of memory protection. Systems designed without it do not support multiple users, nor even UNIX™ very well. The simplest bug will crash the system. There is no protection and no recovery mechanism against even minor problems of access violations. The ability to handle more than one user is usually not allowed, or is strongly discouraged.

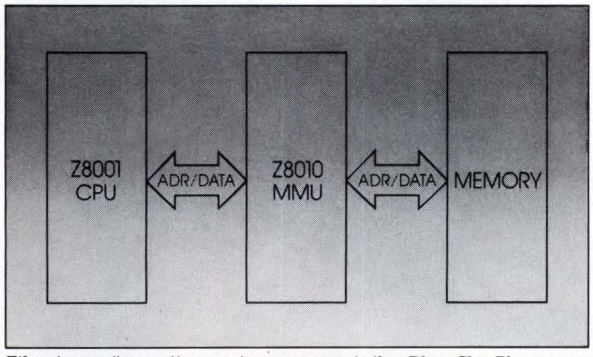


A typical Intel 8086-to-8088 configuration, the lack of memory checking hardware—the memory to the processor. The processor can change any area in its memory at will, without regard to the consequences. The result: illegal operations cannot be detected before damage has occurred; and any damage to the program and data cannot be undone.

THE Z8000 CPU—THE FULL-PROTECTION MICROPROCESSOR.

Zilog's Z8000 CPU solves these problems by inserting a chip called the Z8010 MMU (memory management unit; available in paged or segmented versions) between the processor and memory. This chip normally passes addresses from the processor to the memories—checking each memory access for its address and type of operation as it occurs. If the MMU chip detects an illegal operation, or the use of an unauthorized address, it suppresses the illegal operation and interrupts the program. It passes control to the operating system. Once the program is stopped, the operating system can inspect, correct, or abort the program that caused the error. All with no wait states.

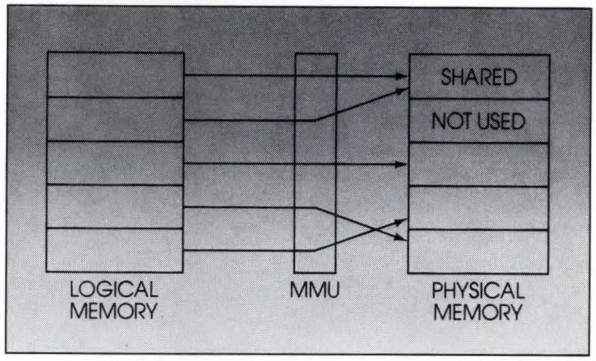
A system constructed with the Zilog MMU can allow many different programs to run without the fear that one program could entirely stop the rest or even corrupt the rest. But, the memory management hardware goes beyond providing protection. It also simplifies system implementation.



Zilog's configuration system prevents the Blue Sky Phenomenon by inserting a chip called the Z8010 Memory Management unit between the processor and memory.

HIGH LEVEL LANGUAGES REQUIRE MEMORY MANAGEMENT.

One of the strengths of 16-bit microprocessors—and the Z8000 CPU in particular—is that they support high level languages such as C, PASCAL and FORTH. A goal of most users is to allow more than one of these high-level language programs to execute in the processor at the same time (multi-user/multi-tasking)—gaining more effective utilization of the computer. The challenge is to provide an architecture that allows a language compiler to produce code targeted to run at one address, but allows the actual placement at a different physical address. This mapping is known as logical to physical translation—a feature of the Z8010 MMU.



Zilog satisfies the common requirement for systems to share information with our MMU. The logical-to-physical translation capability allows more than one logical area to access a common physical area.

SHARED MEMORY IN THE Z8000 CPU.

Another common requirement for systems is the need to share information. With Zilog's Z8010 MMU, the logical-to-physical translation capability allows more than one logical area to access a common physical area. When combined with the protection capabilities of the Zilog MMU, you can set up areas that can be common read-only while the same physical area could be read AND write when accessed under different conditions (operating system access).

For example, you could construct a process control system that posts status information into a common area. The central core of the system is allowed to read and write this common area. Application programs that need access to this information can read it through a totally different segment that is translated into the proper physical address—but with the provision that all access must be reads, not writes. If an application program were to run wild and attempt to corrupt the common area by writing into the read-only space, it would be intercepted before any write could occur.

The key benefit to using Zilog's MMU to implement shared memory is its flexibility to make multiple logical segments access a common physical area with all of the protection—or lack of protection—desired. All with no overhead per access. What's more, Zilog's MMU and other Z8000 devices are available from a host of reliable second sources.

Solving the problem of the "Blue Sky Phenomenon" is only one of the technological hallmarks of the Z8000 CPU. Others will be discussed in this continuing series of technical papers from Zilog, Pioneers of the Microworld. For details on the Z8000 CPU, call our Literature Hot Line at 800-272-6560.* Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.
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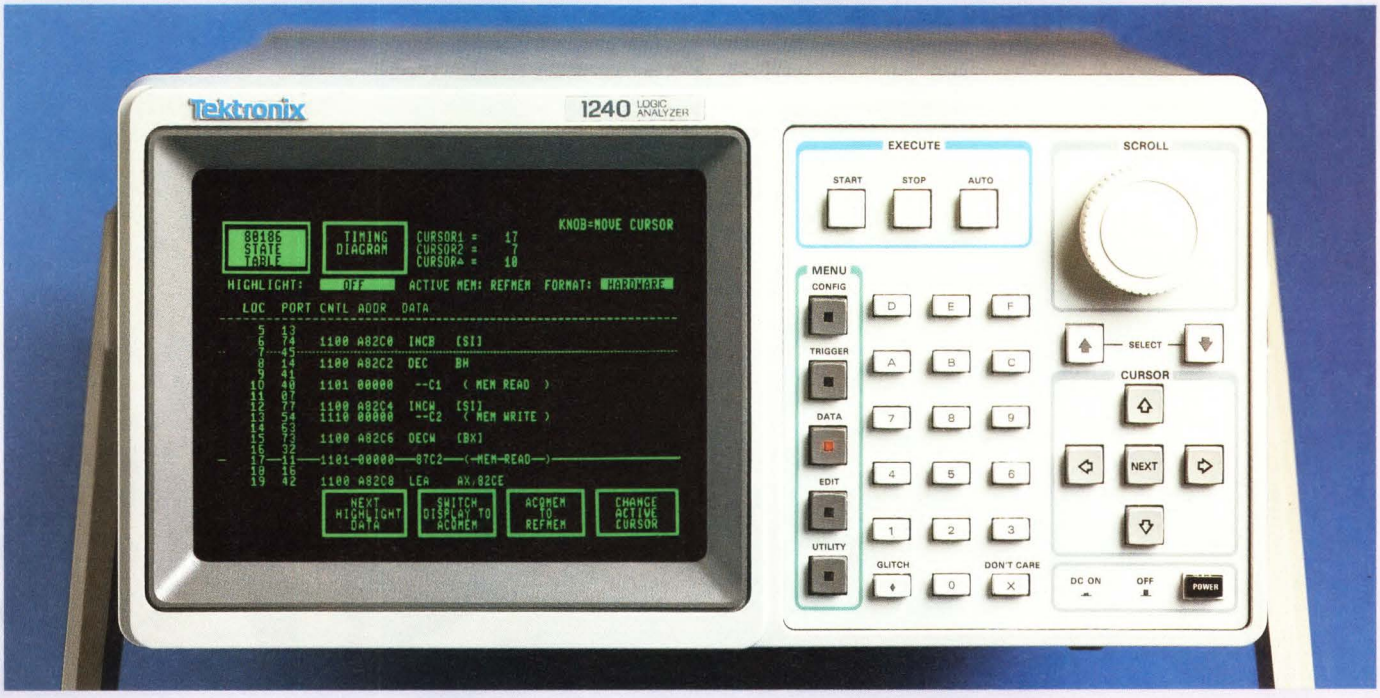

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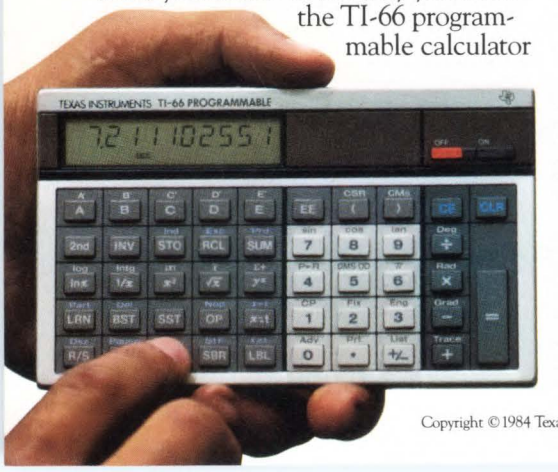

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NEWSFRONT

High-energy implanter cuts SOI processing time by a factor of 20

Long a sore point with silicon on insulator, processing time plummets with an oxygen implanter that also eliminates latch-up.

The prototype of a high energy oxygen implanter slashes the time needed to deposit an insulation layer within a silicon substrate from 20 hours to just 1. Although silicon-on-insulator schemes have long promised denser CMOS chips that are free from latch-up and unwanted capacitance, the technology's extensive processing time has—until now—relegated it to the laboratory.

Jointly developed by the Ion Implantation Division of Eaton Corp. (Beverly, Mass.) and Nippon Telegraph and Telephone Public Corp. (Tokyo), the implanter works with a technique called Simox (separation by implanted oxygen). It forms the buried silicon dioxide layer by forcing large amounts of oxygen (2×10^{18} ions/cm^2) into a semiconductor substrate.

The implanter develops an oxygen-ion current of 200 mA, compared with the 10 mA of previous machines. Since total dosage is linearly proportional to both current and time, its beam-current rating accounts for the twentyfold jump in speed.

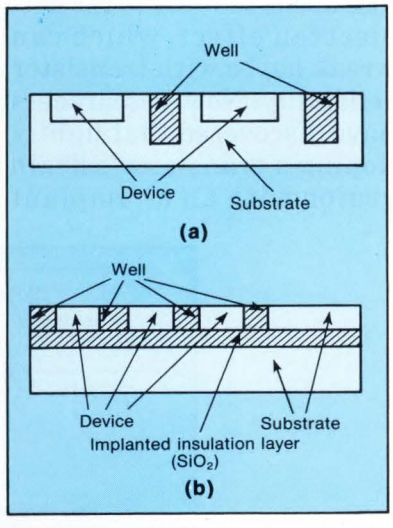
Bringing the silicon-on-insulator technique to the commercial arena will only spur the spread of CMOS chips. The insulation layer created beneath the substrate's surface is well suited to the insulation wells that are one of the hallmarks of CMOS. Additionally, the buried oxide completely isolates each circuit element, cutting down on parasitic capacitance and significantly reducing propagation delays.

Tighter packing

Further, since devices are isolated on their bottoms as well as on their sides, they can be squeezed more closely together. Leakage through the substrate is essentially nil (see the figure), and latch-up is completely eliminated because the substrate is no longer an element of the parasitic vertical device.

Insulating circuit elements not only from the substrate but from each other also makes it possible to place high-voltage components like thyristors alongside logic—a first that should yield some interesting combinations. Finally, silicon-on-insulator chips demonstrate a particularly high level of radiation resistance: Particles striking the device have virtually no effect because the insulating layer prevents any leakage from the active device's elements to the substrate.

The unit was built using some of the knowledge gained by scientists at the Chalk River Nuclear Laboratories (Chalk River, Ont.), who have been working on equipment for generating high-energy hydrogen ion beams. Many of



Transistors built in conventional wells supply some isolation (a); however, they must be well spaced to minimize leakage through the substrate. In comparison, the implanted silicon dioxide layer allows devices to be placed side by side, since the transistors are insulated from the substrate (b).

the problems they encountered turned out to be common for both gases. The corrosive effects of hydrogen and oxygen, for instance, called for exotic alloys and ceramics to be used for all parts that come in contact with the ion beam. What's more, lenses and magnets demanded exhaustive computer modeling to minimize the so-called space-charge effect, where ions with like charges tend to repel one another.

The development of the high-powered implanter heralds a brighter future for silicon-on-insulator chips, but there are still some bugs to be ironed out. The machine focuses 200 kV at 200 mA, resulting in 40 kW that must be dissipated from the target wafer. The solution, researchers believe, lies partly in spreading the energy out over a number of wafers—a's in batch processing—as well as in thermally coupling the wafer to some form of heat sink.

Gary Elinoff

Lightly doped n^- drains put the freeze on hot electrons

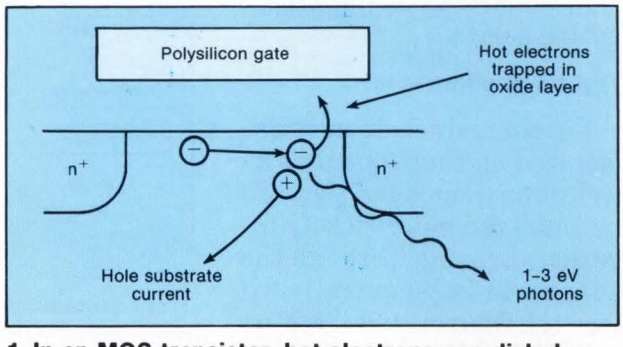
Scaling down MOS geometries cuts cost and increases speed, but it also opens the door to the hot-electron effect, which can wreak havoc with transistor reliability. Now, researchers have discovered that lightly doping a transistor's drain region with an n^- implant forms an effective voltage divider that reduces the potential of the high-speed electrons.

The approach, devised at Texas Instruments Inc. (Dallas), boosts a transistor's reliability by an order of magnitude at the expense of only a 10% to 20% reduction in performance. And it adds only minimally to manufacturing complexity. Until recently, many designers believed that the only way to sidestep the problem would be to lower supply voltages, in turn slowing down the electrons within a transistor.

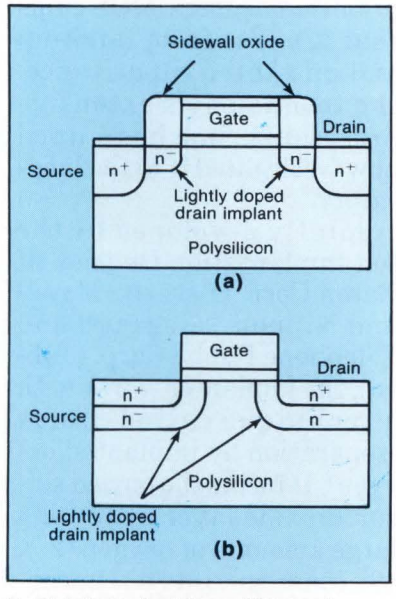
Electrons on the loose

Hot, or high-speed, electrons knock loose holes, as well as other electrons, and lead to three types of failures (Fig. 1). First, the unmoored holes tend to be attracted to a transistor's negative substrate, creating a current that ultimately leads to latch-up.

Second, the free electrons migrate toward and gather in the gate oxide layer, changing the operating characteristics of the transistor. Since the



1. In an MOS transistor, hot electrons can dislodge both electrons and holes, leading to three different failures. Holes migrating toward the substrate can create a substrate current that causes latch-up. Electrons trapped in the gate oxide can change device characteristics and ultimately lead to complete failure. Finally, photons may be generated that can force nearby transistors to change state.



2. TI fabricated two different structures for its lightly doped drain transistor. While one (a) is easier to manufacture and it results in some unwanted capacitance. The more complex structure (b) is harder to produce but yields superior performance.

DDC NEWS

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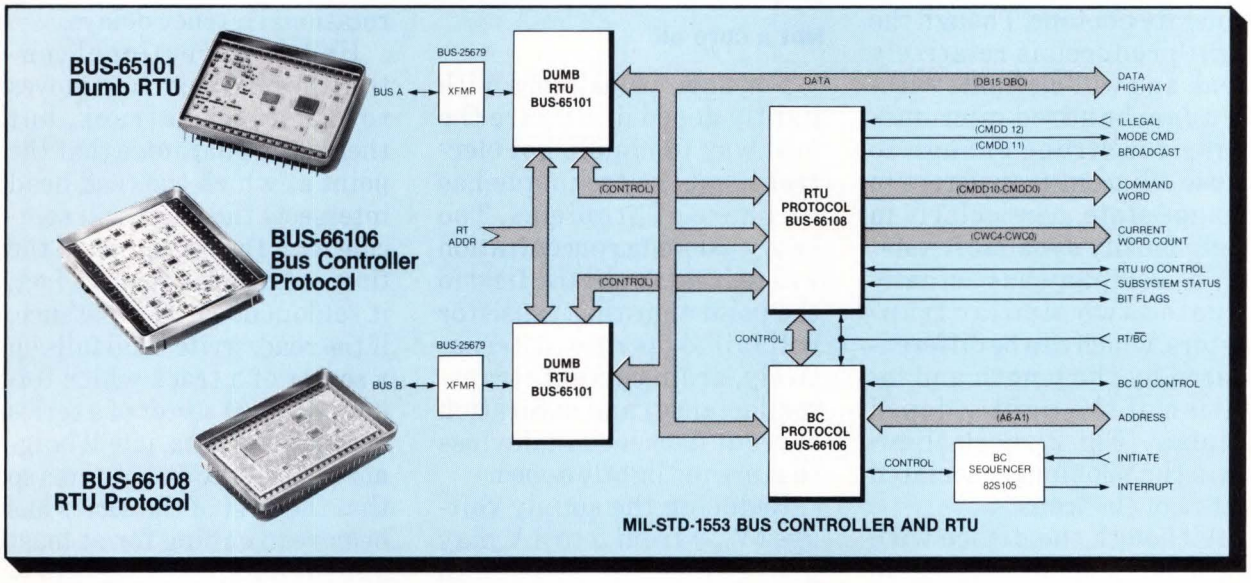
A 1553 BC AND RTU WITH JUST THREE HYBRID TYPES



MIL-STD-1553 BUS CONTROLLER AND RTU

DDC's flexible building block components allow implementation of most MIL-STD-1553 terminal configurations with just a few types of hybrids. As an example, a complete dual redundant Bus Controller (BC) and Remote Terminal Unit (RTU) can be achieved with a Dumb RTU hybrid (BUS-65101), an RTU Protocol hybrid (BUS-66108), and a BC Protocol hybrid (BUS-66106). As shown in the functional block diagram, these hybrids plus data bus transformers and state sequencer IC complete the design.

The RTU provides decoding and response to 13 mode codes with no subsystem intervention. Any combination of mode codes can be illegalized with the use of an external PROM. The subsystem interface is quite simple. Messages are transferred to and from the subsystem with a request-grant-acknowledge DMA type handshaking. Chip Select and Memory Write signals are provided for direct control of subsystem memory. Separate outputs are provided for Command Word and Current Word Count, so that subsystem memory addressing may be controlled by the RTU.

The Bus Controller supports all message formats. Status word and data word responses are validated by the BC Protocol hybrid with no subsystem intervention. The subsystem interface to the BC is similar to that of the RTU, Data ¶s transferred with DMA handshaking, and address and control line outputs are provided.

The Bus Controller sequence starts with the loading of a control word and a command word into the BUS-66106 storage registers. Since the control word contains message format and channel selection information, the BC Protocol hybrid completes the operation, on its own, after receiving a start command. Interrupt flags are provided to the host CPU for conditions of end of message, error, status bit set, and timeout.

The functional block diagram shown in the figure illustrates a combined Bus Controller and Remote Terminal Unit. Since the RTU Protocol and BC Protocol are contained in separate hybrids, the BC or RTU functions may be implemented individually by just omitting the appropriate protocol hybrid.

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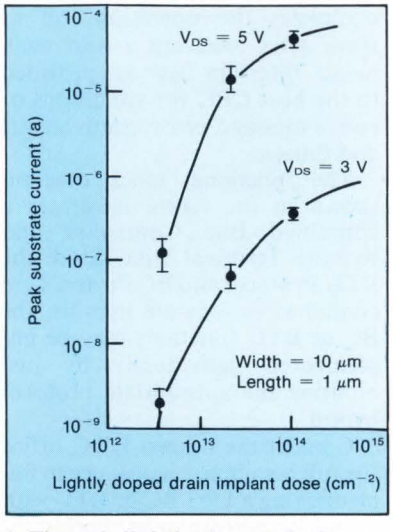
oxide layer is an insulator, the electrons have no place to go and if enough electrons collect, the transistor can fail completely. Third, the energy level of the electrons can become high enough to actually generate photons. Though the light produced is relatively weak and will dissipate within a few hundred micrometers, it is strong enough to cause adjacent transistors to change state, particularly in high-density dynamic RAMs.

The company has actually created two similar transistors, which can be differentiated by the length and location of the lightly doped implant (Fig. 2). Both eliminate the problem associated with hot electrons.

Although the device with the longer implant is easier to fabricate, it introduces some stray capacitance. It is being used in TI's family of 2-μm parts, but the company will go with the second design for devices made under the VHSIC program.



3. Though lightly doped drain structures reduce the peak substrate current, cutting supply voltage (V_{DS}) from 5 to 3 V has a far more dramatic effect on substrate currents.

Not a cure all

For now, transistors with lightly doped drains are the best way to handle hot electrons, but the technique has its share of problems. Too heavy a doping concentration will reduce the electric field to the point that the transistor will fail to operate. Alternatively, drain current (transconductance) and saturation current decrease in devices that are too lightly doped.

Reducing the supply voltage (V_{DS}) from 5 to 3 V may prove to be the answer to clamping a lid on the substrate currents associated with hot electrons (Fig. 3). But a change in supply voltage seems unlikely at present, since greater attention to noise immunity and tighter circuit control go hand in hand with lower voltages.

Heather Bryce

Read-ahead algorithm speeds disk access in Unix-based systems

A disk caching algorithm specifically optimized for Unix operating systems increases hard disk access speed 15% to 40%. The algorithm, a read-ahead routine incorporated in a disk controller, assumes that search requests made under Unix will repeatedly ask for data that is contiguous to the previously read sector. In addition, the head will begin reading data the moment it lands on the appropriate track—virtually eliminating rotational latency delays.

Under conventional control, the read head first moves to the selected track, but there is no guarantee that the point at which the read head intersects the track will coincide with the beginning of the first sector to be read. In fact, it seldom does. For instance, if the read/write head falls on a sector of a track which follows the first sector of a series of requested data, it will be ignored until the disk rotates so that the first of the series has been read calling for at least another half-revolution—adding a minimum of 8 ms to the data access time.

The peripheral controller, devised by Interphase Corp. (Dallas, Texas) for its Multibus controllers, overcomes this problem by reading the data sectors at the very point at which the read head intersects the track. If, for example, the user requests information located on sectors three, four, and five of a particular data track, and the head lands on sector four, the Interphase controller will actually begin by reading sector five (the beginning of the next contiguous sector). The contents of sector five, and all successive sectors on the track, will be automatically read and transferred to a buffer memory space on the controller. When sectors three, four, and five have been

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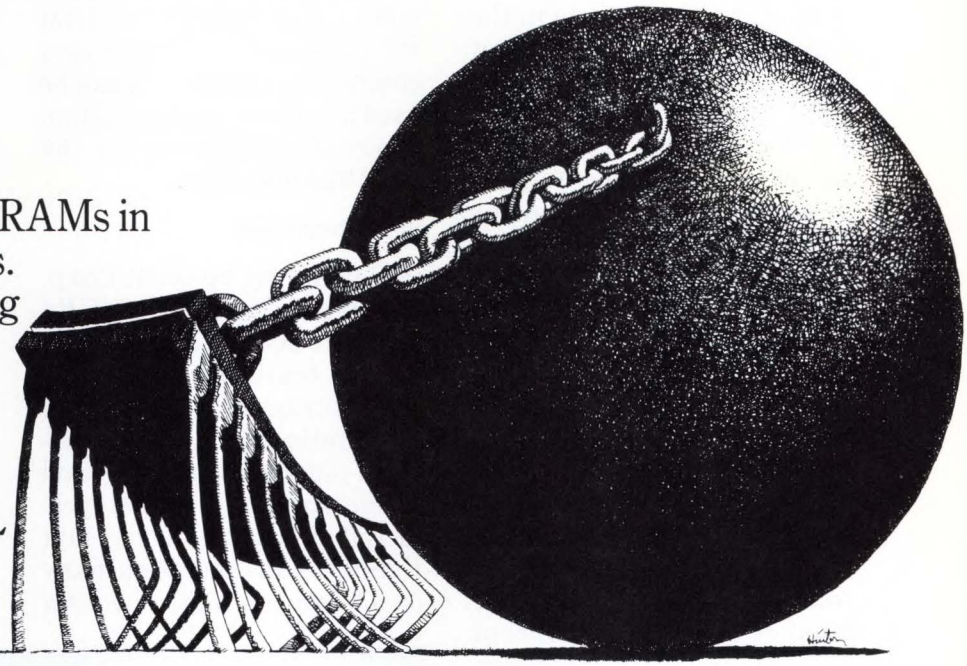

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read, the entire block will be transferred to the host. If the next request is for information on sectors six, seven, and eight, the time required to access it on disk is eliminated since that information already exists in RAM.

In many situations—especially where there are no other read/write requests in the disk queue—the contents of the entire data track will be read and transferred to a 16-kByte buffer. The buffer serves the data cache, and will be examined first when the controller receives the next read data request.

Interphase's disk cache scheme speeds disk access dramatically when data is located on contiguous sectors. But it does not have as great an effect with the scattering and gathering problem plaguing Unix systems—especially likely in a multitasking environment where the controller must respond to concurrent disk I/O requests. However, Interphase claims that a hardware memory management system can overcome that by building a scattering and gathering priority scheme into the controller. The head could then reach scattered files directly and in sequence without host intervention. *Stephan Ohr*

Multibus-based RISC brings 32-bit power to the board level

For the first time a 32-bit reduced-instruction-set computer (RISC) has been reduced to a single board for the Multibus I structure. The computer, installed on a NCR 3200-based development board, can either serve as a powerful add-on coprocessor in an existing system to provide 32-bit processing power in a Multibus I environment or emulate a computationally intensive processor. Moreover, when linked to an IBM PC personal computer or a compatible machine, it can be used as a development system to create programs for the NCR 3200 chip set.

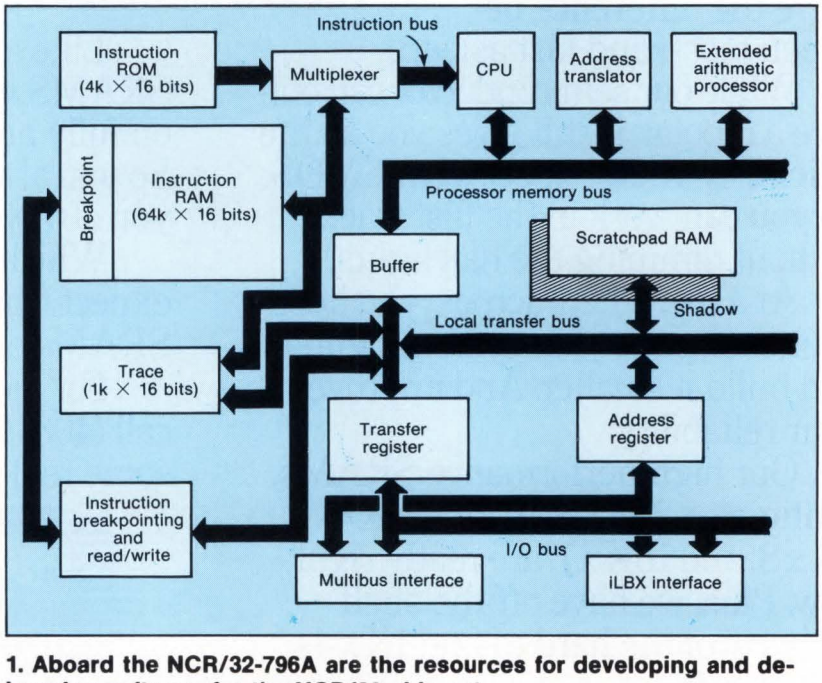
Risky business

Developed by NCR Corp. (Dayton, Ohio), the NCR/32-796A board draws on the salient features of RISC architectures, including simple instructions, a straightforward pipelined structure, and a high-speed instruction cycle of 150 ns. Based on that last figure, it can execute as many as 6.5 million instructions a second. In addition, it can move local data easily with only a few instructions.

As expected from its model number, the board carries the basic NCR 3200 chip set, including the CPU, the address translator, and the extended math chip (Fig. 1) along with local storage and I/O buffers. The translator works with a 4-Gbyte virtual and a 16-Mbyte physical addressing range, while the math chip tackles floating-point and other advanced arithmetic operations.

The board itself runs in two modes: direct and microprogram (or emulation). In the first it directly executes an external program comprising NCR 3200 instructions; in the second, it locally executes an external program, calling on microprogram subroutines and macros.

The Multibus card is designed to aid software devel-



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One octave from band edge		5.5	7.0
Total range		6.5	8.5
ISOLATION, dB		*TYP.*	*MAX.*
0.2-2 MHz	LO/RF	55	45
	LO/IF	50	40
2-250 MHz	LO/RF	50	35
	LO/IF	35	30
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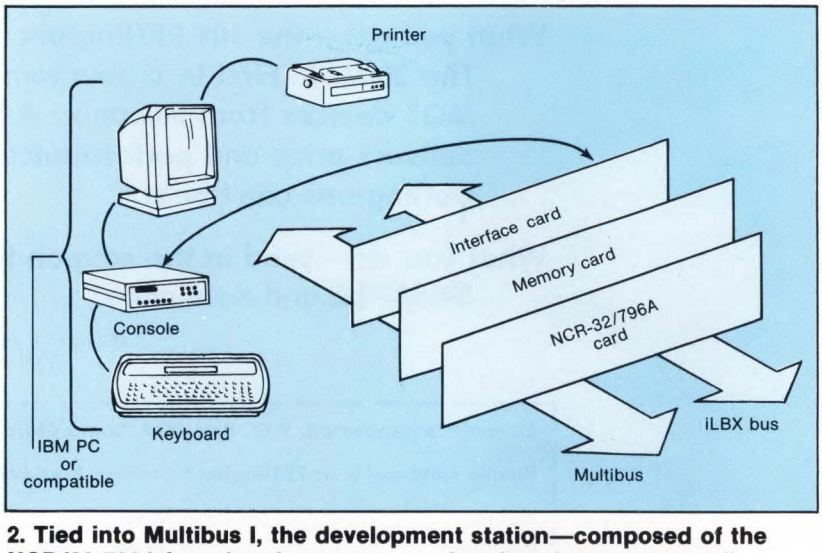
opment and debugging. The necessary diagnostic software is stored within part of the ROM of the instruction storage unit. For example, each microinstruction word in that memory carries a breakpoint bit that can be set during debugging. Furthermore, a special 128-word scratchpad memory is used for intermittent debugging, keeping that activity independent of the target program.

Microprogrammed

Initially, the board's instruction storage unit, which contains the microprogram and direct execution operations, will hold 16,000 words, each 16 bits wide. Eventually it may store as many as 64,000 words.

The CPU accesses local memory through either the Multibus itself and on-board memory through the faster iLBX bus, with the board acting as a primary master (Fig. 2). Interfacing the 32-bit processor with the 16-bit wide Multibus entails double buffering the input and the output data. The card uses the bus's full 24-bit address path, and its dynamic address translation unit maintains a set of 16 active pages, which can be 1, 2 or 4 kbytes deep. Naturally, versions of the card are in the works for 32-bit buses.

Ray Weiss



2. Tied into Multibus I, the development station—composed of the NCR/32-796A board and a memory and an interface card—easily hooks up with an IBM PC or similar machine.

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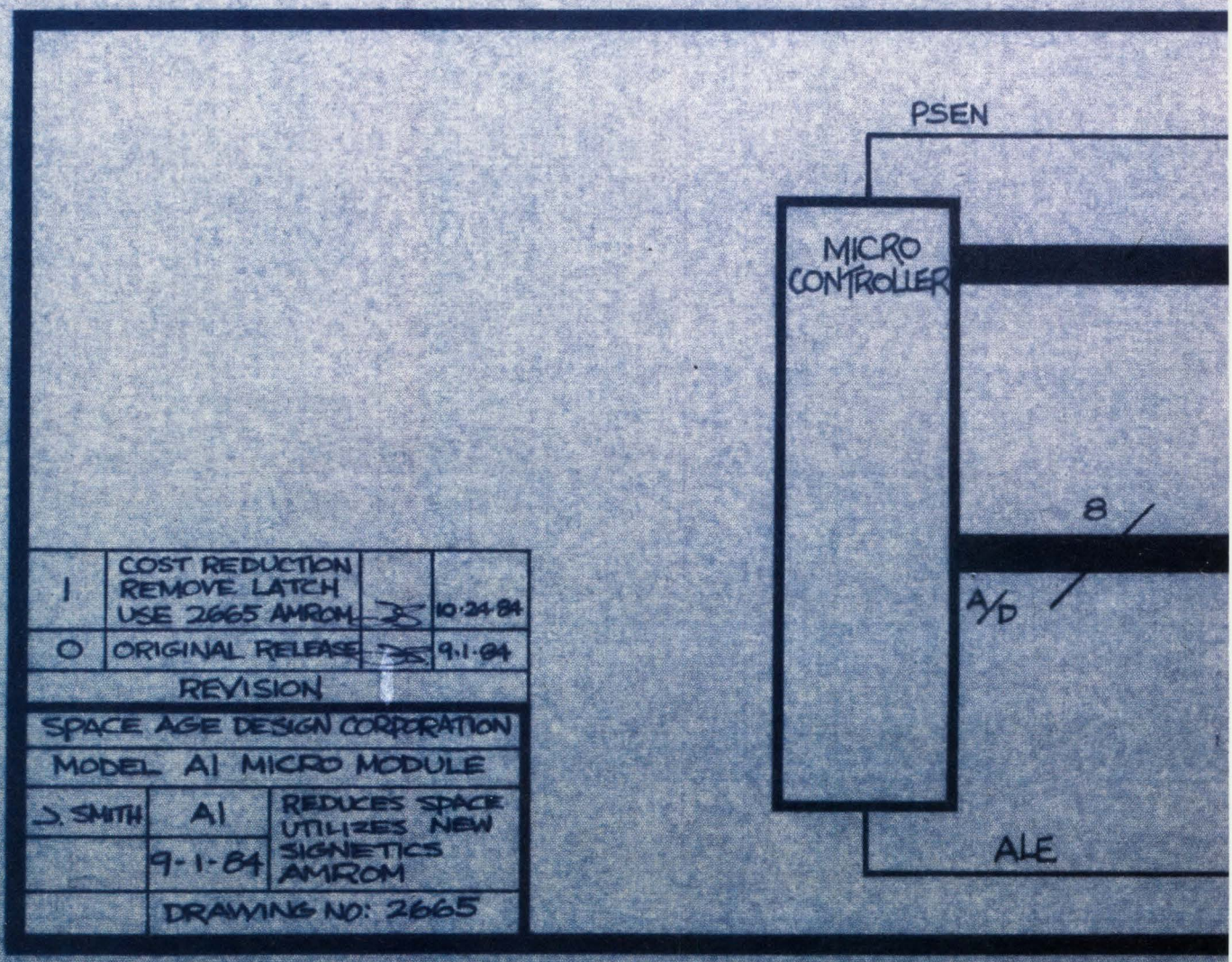

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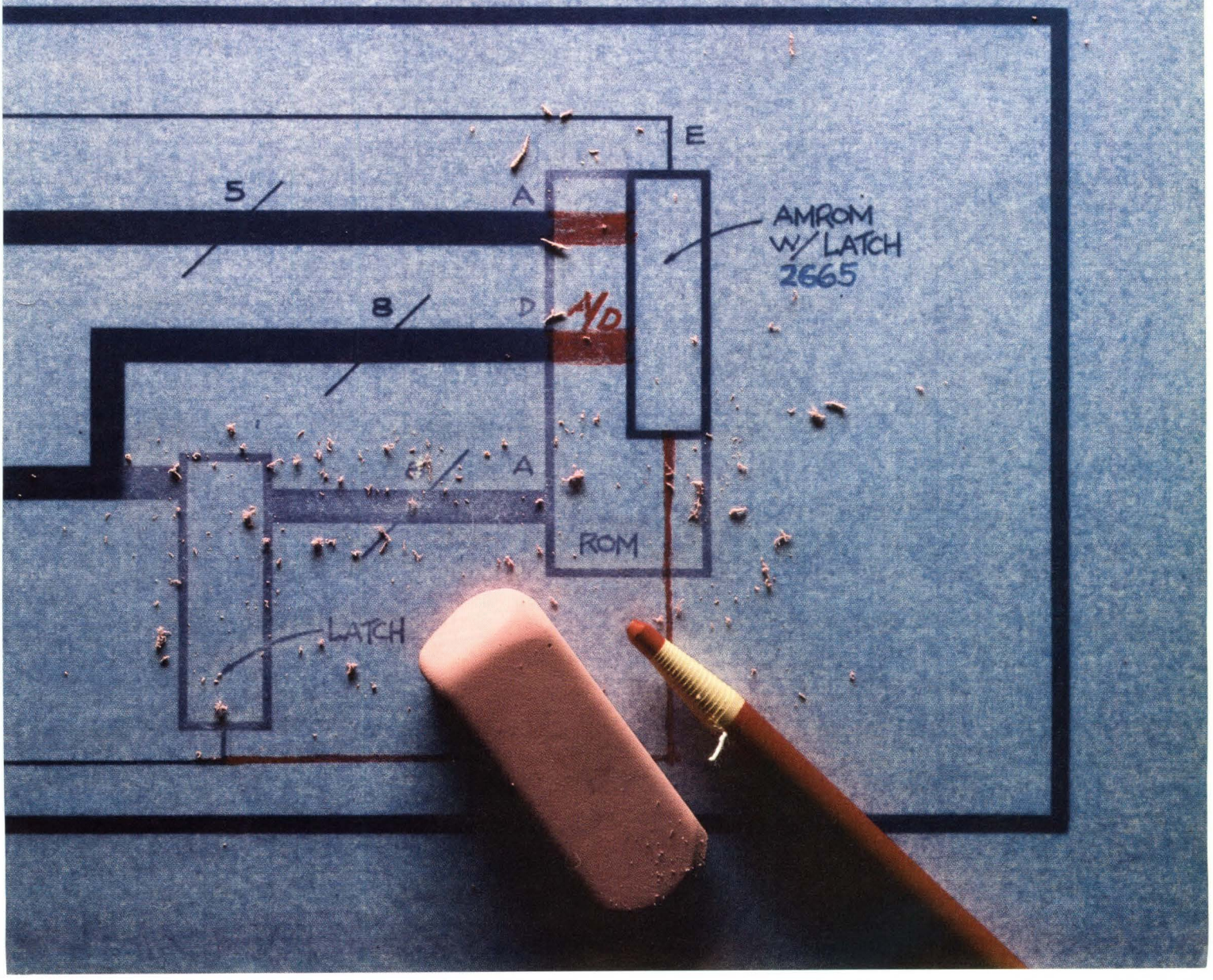

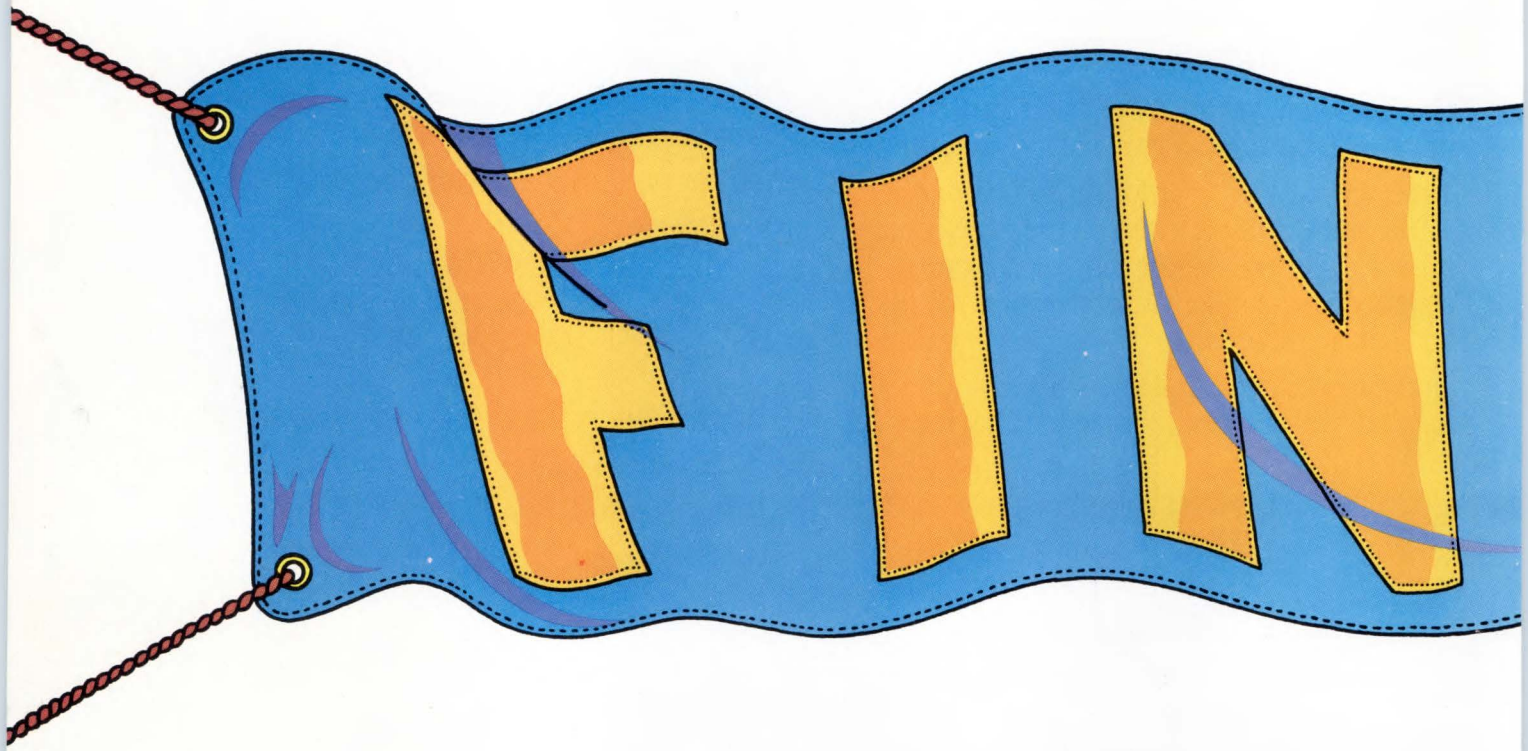
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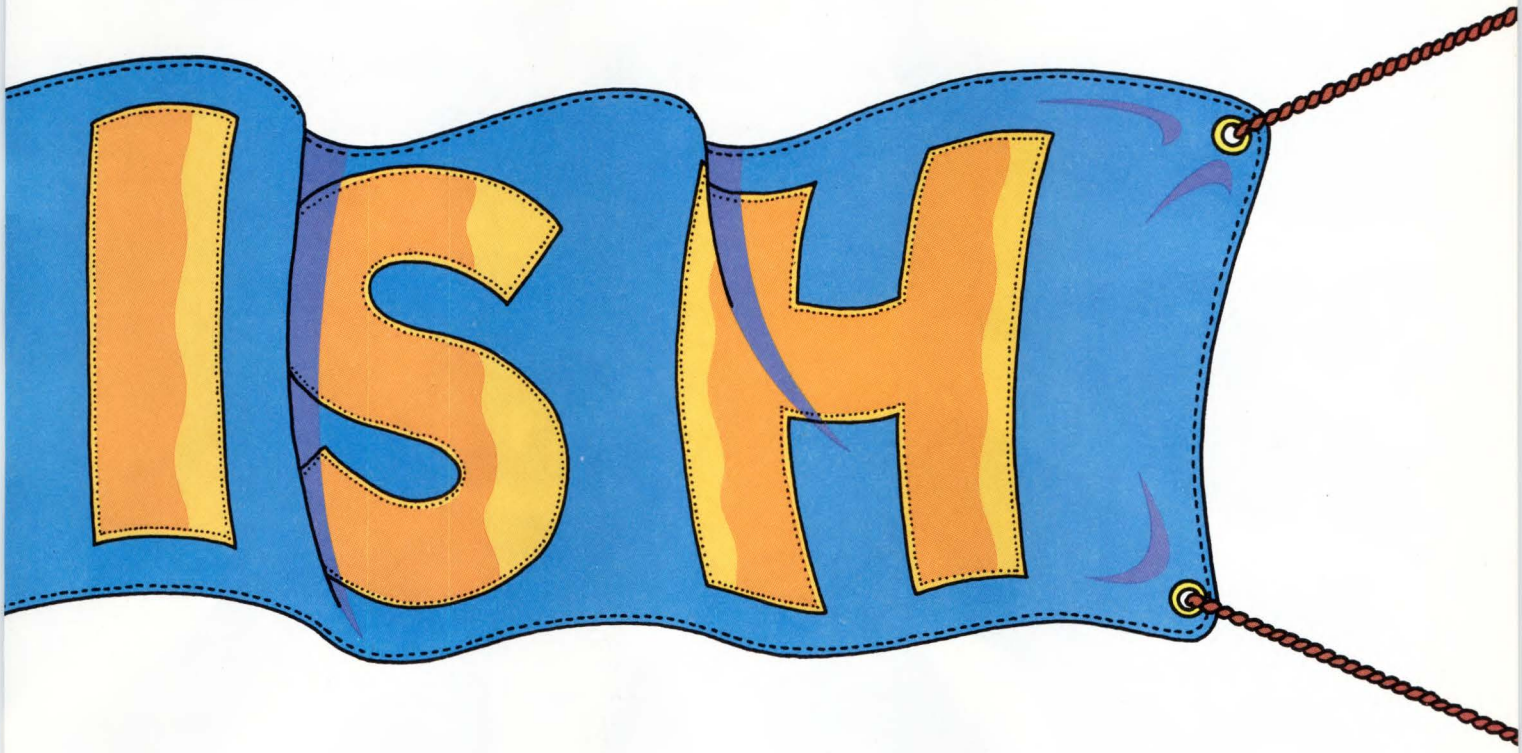

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NEWS ANALYSIS

Forth forsakes its image, moving from laboratory to software engineering

An adaptive language gets a second chance to show its strength—from numerical control to expert systems.

Forth, a computer language devised in the 1970s for real-time processing, is coming under increasing scrutiny as an alternative to its brethren for the coming generation of computers. Long ignored and relegated to the laboratory, Forth has been quietly building a hardware and software base. It is almost universally available, is portable, and boasts an interactive development environment.

New implementations of Forth seem to be popping up every day, ranging from dedicated microprocessors with Forth embedded in ROM to a microprogrammed version for a 32-bit chip set. And Forth is being increasingly turned to as the language of choice for applications that run the gamut from sophisticated data processing to control software. Even expert systems—normally the domain of languages like Lisp and Prolog—have appeared in Forth as well.

Ray Weiss

Forth is more than a high-level language; it also includes a software methodology, an interactive environment capable of incremental development, an assembler, and an operating system.

Forth and moving up

Forth has already been adapted for most popular minicomputers and micros, and is starting to surface for the newer computers as they arrive. One example, MacForth, from Creative Solutions Inc. (Rockville, Md.) is the first truly usable software development package for the Apple. The package takes full advantage of the Macintosh's hardware and software, and employs a 32-bit software architecture to mesh the language with the machine's operating system, user interface, file system, and toolbox.

Though compatible with the Forth-79 standard, MacForth has added some words and operators, so that it includes most of the Macintosh's commands. Rounding out the package is a 68000 assembler, which takes an indirect token approach to implementing threaded code. The package operates on top of the Macintosh operating system, and it is able to define and delimit memory space. MacForth occupies 25 kbytes of memory, partly because of its 32-bit addresses and partly because of the interfaces to the Macintosh core programs.

MacForth is a descendant of Multi-Forth, an adaptation for the 68000. Multi-Forth itself runs on the HP 200, the Motorola EXORmacs, and the VME 110, as well as on most single-board computers built around the 68000. Additionally, when wedded with Unix, the resultant Uniplus package can run on the Perkin-Elmer 7300 and gives users access to the Unix file system and shell commands.

For newer processors

Forth's proliferation into newer processors is typified by the polyForth II system now running on the 9300, from NCR Corp. (Dayton, Ohio), which is based on the company's recently released 32-bit 3200 chip set. The language was easily transported to the system because the computer was designed for microcode emulation. The software, a version of polyForth, from Forth Inc. (Hermosa Beach, Calif.), places the Forth primary definitions in the 16-bit-wide writable control store, with the secondary definitions in dynamic

memory. Only 8 kbytes of the available 128 kbyte control store contains the entire program.

Simple Forth instructions execute in 1.2 to 4 μs, because of the 9300's 150-ns clock cycle and pipelined architecture. Moreover, the call and return overhead for high-level Forth instructions is only 3.45 μs. The machine can compile a full Forth block (16 lines) in 50 to 100 ms, depending on the definitions involved. The system is presently hard at work in a hospital, running between 30 and 40 terminals in real time. It will soon be in charge of up to 250 terminals.

The powerful combination engendered by matching Forth and the 3200 chip set will not be restricted to the 9300. Board-level products are expected soon; initially designed for the Multibus, they will also feature polyForth as an option.

A world to win

As Forth is embedded in the ROM of single-chip microcomputers, its horizons are considerably broadened. One way in which it serves the need for fast, local processing in board-level systems can be found in the RSC-Forth of the 6500 family of single-chip microcomputers, from Rockwell International Corp. (Newport Beach, Calif.).

The R65F11 and R65F12 are 8-bit NMOS processors that carry the run-time portion of RSC-Forth, another modification of Forth-79. The run-time code occupies 3072 bytes and contains 133 Forth operators and words. The chips themselves can handle up to 8 kbytes of off-chip RAM for active program memory and contain 192 bytes of on-chip RAM.

For program development, a separate ROM chip, the R65FRx, retains the Forth development systems, comprising 153 development operators and an assembler. A simple development system can be configured using this chip, one of the processors, and the necessary RAM.

No experts need apply

An interesting variation on the embedded Forth scheme is seen in the MA2000 family, from National Semiconductor Corp. (Santa Clara, Calif.). The family is made up of a set of small, stackable plastic-encased modules that form a fully self-contained Forth-based computer system when assembled. A stand-alone entity rather than a board-level system, it can be used to tackle various control, testing, or monitoring tasks. Amazingly enough, setting up the system requires no engineering expertise.

Further, the MA2000 carries its own power-supply module and can be linked with a terminal and a printer. It also features its own CMOS RAM disk with battery back-up. Another of Forth-79's offspring, MVP-Forth, from Mountain View Press Inc. (Mountain View, Calif.), is embedded in its ROM.

But there is more on the Forth front than just systems: The language is being applied to new areas, such as artificial intelligence. Like Lisp, one of the more prominent AI languages, Forth is both a functional and an extensible language. Thus it can be easily tailored to build and functionally process rules for expert systems. Moreover, unlike Lisp, Forth is fast, needs little memory, and is available on most computers.

For instance, one simple implementation of Forth models the basics of expert systems. The expert system tool kit, distributed by Mountain View Press and Miller Microcomputing Services (Natick, Mass.), includes the Forth source code, a rule interpreter, a fact file, a knowledge base, and a user interface. Designed as an exploratory tool, the program can be easily altered.

On the right track

A far more complex and sophisticated undertaking is the diesel electric locomotive troubleshooting aid (Delta) expert system. Completed and now being evaluated by General Electric Corporate Research and Development (Schenectady, N.Y.), the system, as its name suggests, tackles the formidable job of troubleshooting and providing guidelines for repairing railroad locomotives.

Originally designed in Lisp, Delta's field prototype was written in Forth (to ensure portability) and run on a Digital Equipment PDP-11/23. It has been housed in a rugged unit that holds the computer, a 10-kbyte disk, a VT100, and a graphics board. It uses a color monitor and works in conjunction with a Sony laser-

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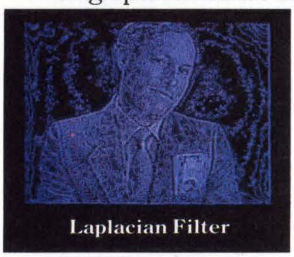

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Delta has a grand total of 530 rules: 330 for troubleshooting and 200 for help. As the system is tried and evaluated, the rule base is expected to grow to over 1200. Its rule processor consists of both a backward and a forward interpreter; that is, both backward and forward chaining are used.

Forward chaining is a search through the rule base that is initiated by some action (including adding a new fact) to determine what the results of the action will be.

The search itself may generate a new action through the success of an "if . . . then" rule. And the rules in the system are weighted, which means that they can carry different values based on the certainty of their assertions.

Don't look back

Alternatively, the system uses backward chaining to search the rule base in order to prove a hypothesis. A search can be initiated by the system while it is tracing a fault or by a user in response to a question. The search may generate new facts during the evaluation of "if . . . then" rules, which will in turn trigger a forward search.

Essentially, forward chaining is used to update the knowledge base, and backward chaining is used to prove or disprove each hypothesis and the system works toward a solution. Both searches may result in system actions and the creation of new facts.

Forth has proved to be a particularly suited medium to implement the expert system. Forth words were used to create the necessary high-level operators to build the system, which is easy to set up and can be used without any programming. Additionally, nine predicate functions—operators that assign truth values to the rule premises (the fronts of the rule)—were added to Forth's basic vocabulary. Also added were eight verbs, operators to specify actions for successful rules (send messages, make new facts, and the like). Finally, five utility functions were defined for the user interface and for graphics representation.

In the same class

Because of its full range of properties, Forth has been used as the base for a number of end-user data-base systems for machines in IBM's personal computer class. One such is Savvy, from Excalibur Technologies Corp. (Albuquerque, N.M.), a natural-language system for generating application programs.

Another is Simplex, an integrated data-base system with a pascal-like interpretive language, word processing, communications, Macintosh-like windows, and graphics. Simplex is based on Forth-32, a full 32-bit version of Forth, and has been developed by Quest Research Inc. (Huntsville, Ala.). A third example is Salvo, a fourth-generation data-base system from Software Automation Inc. (Dallas, Texas). Salvo is a relational data-base system that is coupled with an application generator and works with an English-like language.

Despite its bright future, there are a number of criticisms and weaknesses that will have to be addressed before Forth gains complete acceptance. For example, Forth code tends to be cryptic and hard to read because it uses keyboard symbols and abreviated mnemonics for Forth operators. Also, due to Forth's unique environment, individual programmers tend to tailor systems to their own needs, in turn restricting the speed of higher-level development tools. Furthermore, Forth places a lot of power in the programmer's hands with little or no checks to limit possible system damage.

Finally, Forth lacks the general-purpose utilities that are common in more popular operating systems, such as sophisticated record and file services and generalized I/O processing. It also lacks higher-level programming constructs. At present, Forth is a high-level language, with incredible power and versatility, targeted only to the best programmers.

Luckily, it is quite malleable and it can be modified as needed. As it becomes more widely used, the language will evolve to meet software engineering requirements. In all probability, there will ultimately be a number of levels of Forth, ranging from a relatively unstructured programming tool to a heavily structured tool under the control of software engineering.□

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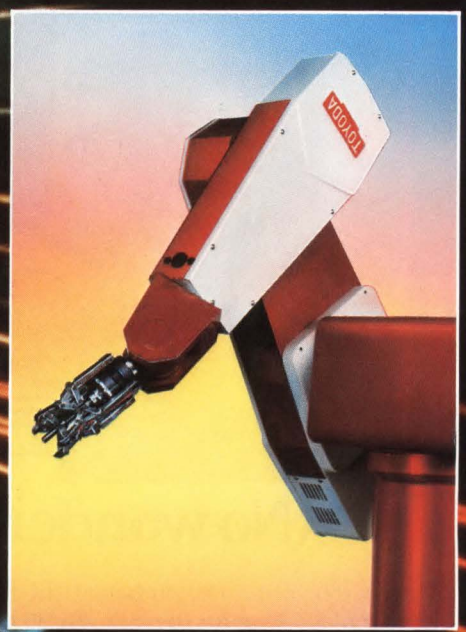

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CIRCLE 30

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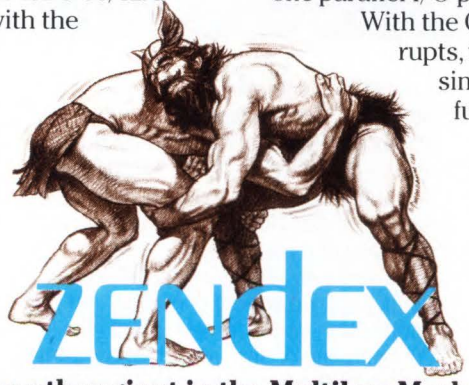

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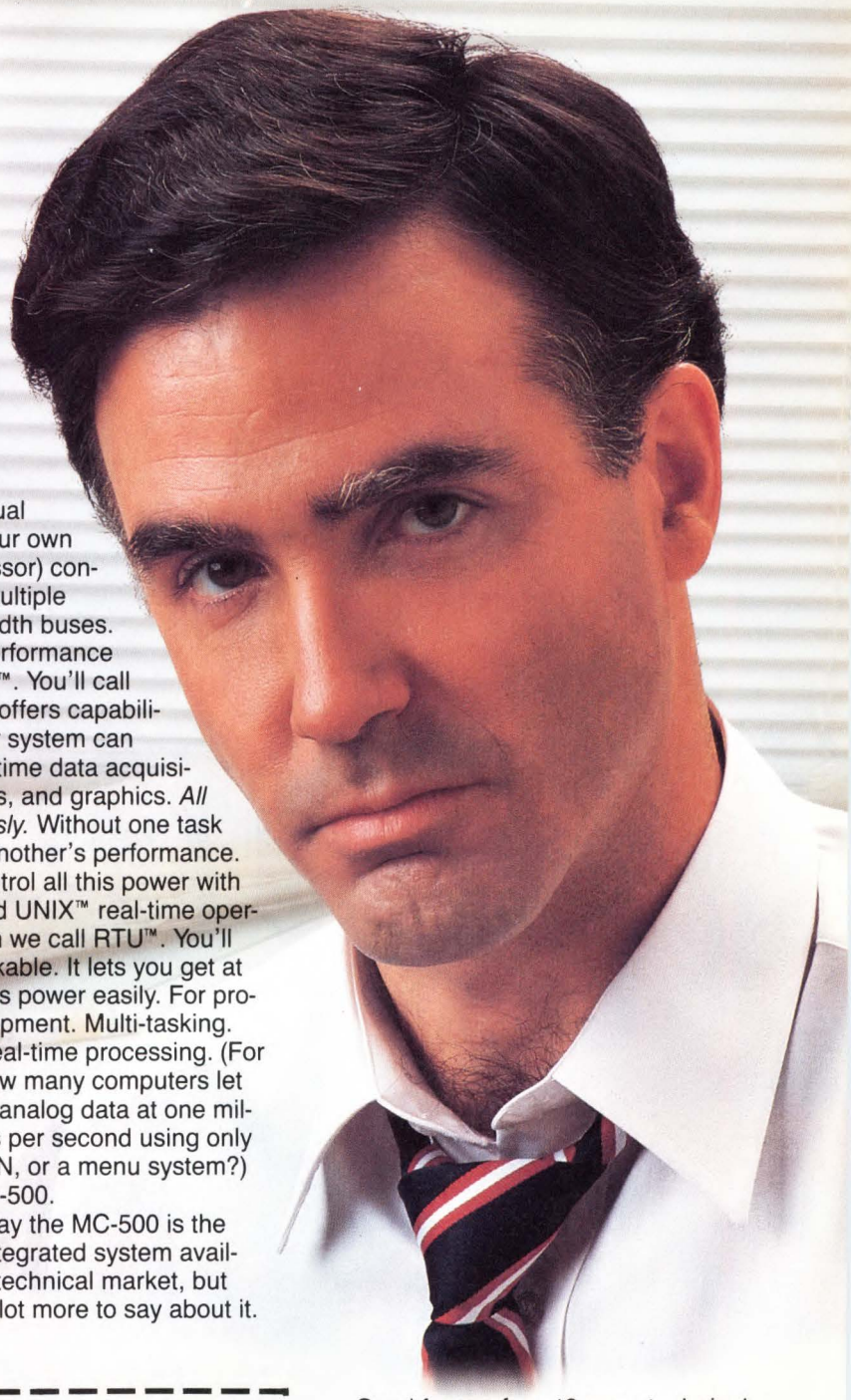

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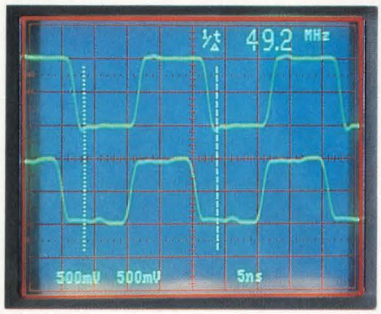

This unretouched photo shows a .8 nsec rise time pulse at the entry point (top wave form) and at the end (bottom wave form) of a 21" Wire-Wrap transmission line. By using twisted pair and properly terminating the line, ringing and reflections are minimal.

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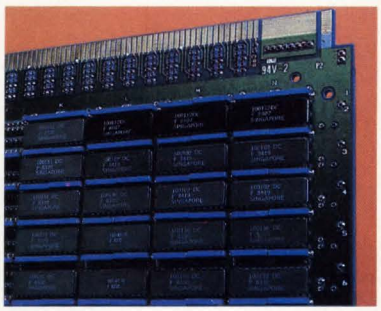

F100K ECL devices and terminating resistors on a Wire-Wrap panel.

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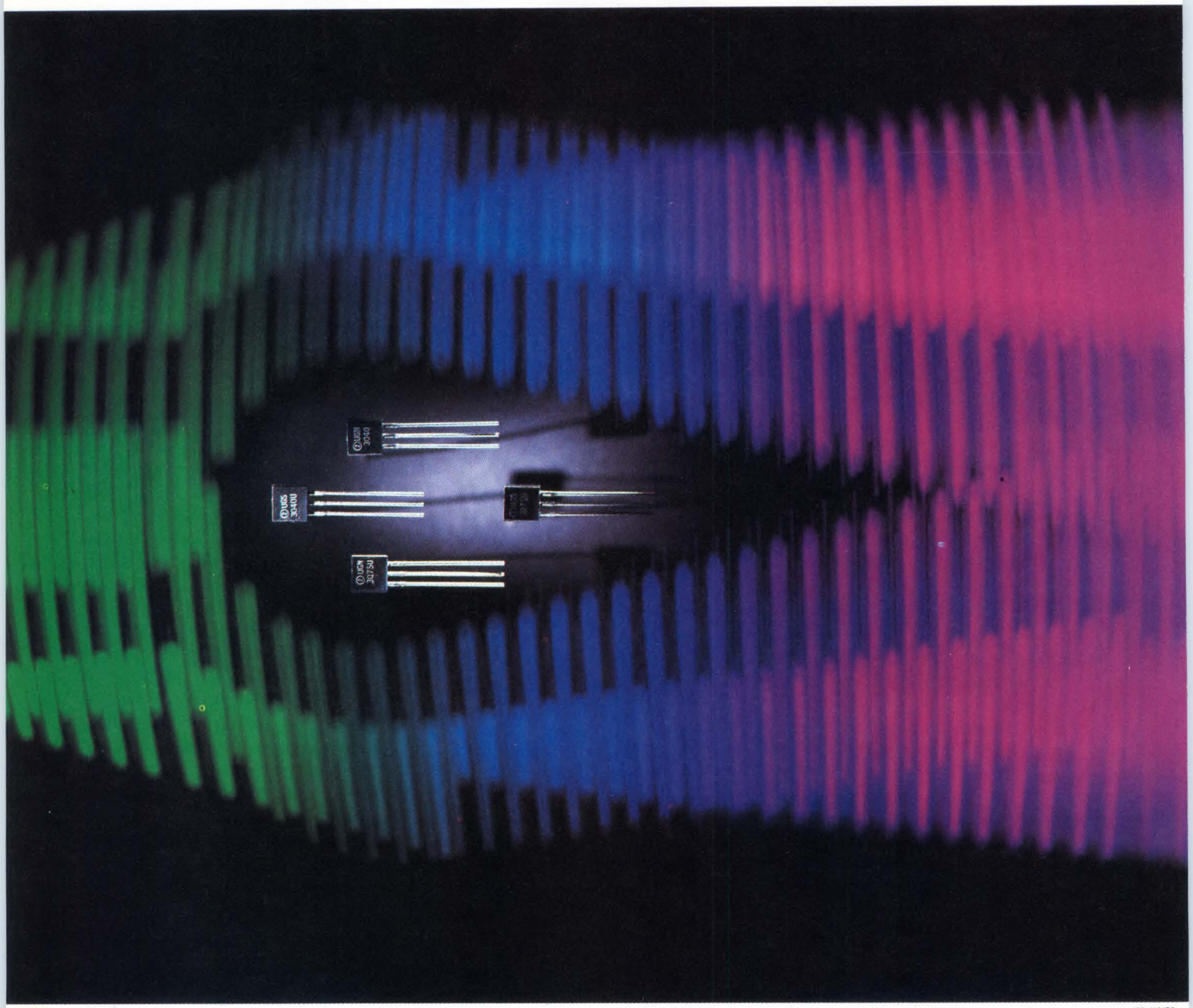

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CIRCLE 32

VIEWPOINT

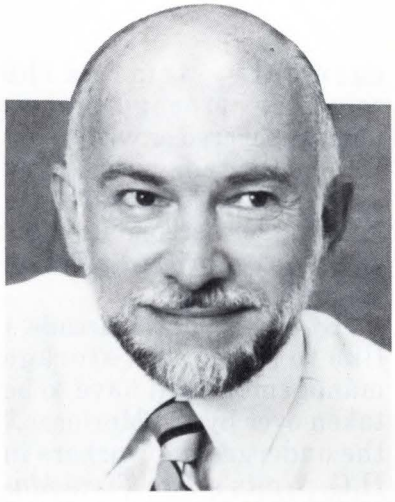
More cooperation is needed from operating system makers to reap the benefits of SCSI

Phil Devin
Marketing Directory
Xebec Corp.
San Jose, Calif.

The Small Computer Systems Interface (SCSI) is not getting the support it needs from operating system manufacturers, who provide the driver subroutines for SCSI storage devices. The reason, suggests Phil Devin, is that most existing operating systems are designed to work with one controlling CPU and not with an intelligent peripheral device within the I/O channel.

The SCSI, which can speed up the process of finding, storing, and organizing information, evolved from the original SASI (Shugart Associates System Interface), which itself has many variations. "SASI controller manufacturers," says Devin, "have traditionally implemented very low-level features of the SCSI command set. In addition, they provide their own software to integrate the device with the host's operating system." This situation, he feels, has led to cautiousness on the part of manufacturers in incorporating full SCSI command sets and in developing drivers that take advantage of its capabilities.

The best of the low-level SCSI drivers can use commands such as Read Capacity, which provides the host with the number representing the logical blocks on a disk or tape and the number of the blocks used in data transfer. The most basic of these drivers, however, implement only Read, Write, and Request Status commands, which make the SASI implementation little more than a dumb-device interface.



Phil Devin has more than twenty years of experience in the computer and peripherals industry. He is currently marketing director at Xebec. He holds a BSEE from Iowa State University.

At the opposite extreme, explains Devin, SCSI implementations resemble IBM block-multiplexed I/O channels and thus would require substantial engineering investments in SCSI driver programs. The block-multiplexed channels typically use intelligent host adapters with a "mailbox" structure, which must be perpetually addressed and maintained by the host. While the mailbox helps cue I/O for peripherals in a multitasking environment, Devin points out that "writing software drivers for those host adapters is a project requiring many man-months of engineering labor."

Operating system manufacturers have a tendency to interpret "I/O performance" as "terminal response time" and have therefore partitioned the available I/O buses according to the way that the host CPU would normally handle data and address transfers.

SCSI controller manufacturers, Devin contends, would like to see the priority for bus access more equally distributed between the host computer and the intelligent pe-

Stephan Ohr

ripheral controller. "This would allow the controller to make more efficient use of the buses, especially when dealing with different peripherals".

For example, Unix has emerged as an outrageous "disk hog" because of its tendency to scatter and gather files on multitasking systems. That problem could be greatly reduced if the operating system were oriented to relinquish some of its priorities for bus control to the intelligent controller.

In many ways, the situation between SCSI intelligence and current operating systems is similar to the situation in which an operating system must accommodate more than one master. Though they have begun to deal with multitasking and concurrency issues, most operating systems still revolve around one CPU juggling many tasks.

In the foreseeable future, Devin projects, "the needs of small computer systems will be less complex, with a single SCSI controller handling the resources of disks and tapes on a multitasking, multi-user machine running under a single host." Already ANSI has proposed allowing a controller to state the level of SCSI intelligence in response to an operating system inquiry.

Devin recognizes that there will be no simple solution to any of the conflicts, though he does suggest that as many as possible of the operating system makers and SCSI controller manufacturers begin a dialog on these issues. The annual SCSI forum, he feels, might be one appropriate place for that to begin.

Storage subsystems will maintain tomorrow's relational data bases

David L. Childs
Vice President
Set-Theoretic
Information Systems Corp.
Ann Arbor, Mich.

The real achievement of relational data bases was wresting the data base itself from the tyranny of a user's organization and management. But to handle the extremely large data bases of tomorrow, asserts David Childs, a further separation is called for. The link between the data-base management system and the secondary storage devices must be severed as well.

In fact, he emphasizes, any system that necessitates knowing how secondary storage is organized will be doomed to failure.

"By the end of the decade, I like to think that storage management will have to be taken over by the Morlocks," the underground workers in H.G. Wells's *The Time Machine*. "They were superbly efficient at such mundane tasks as storage, garbage collection, and maintenance. And in the computers that are on the way, storage-maintenance chores will be handled by computer subsystems that are independent of users."

Childs conceives of these subsystems as intelligent devices coming between the secondary storage and the actual data-base management system. They will be able to transfer access requirements to storage.

Now, a relational record is stored as a physical entity, so whole records are pulled into the computer's buffer during an operation. But 90% of the information brought in is subsequently thrown out be-

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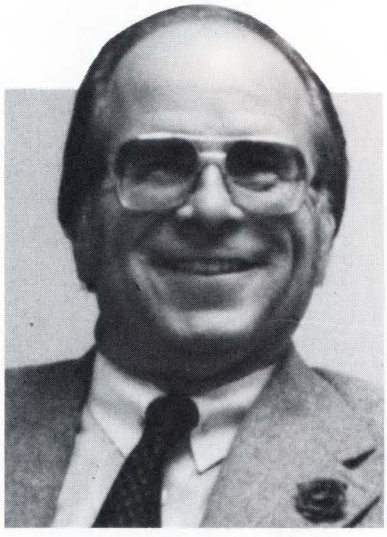
cause only a portion of it is actually needed.

Child's premise is that a record does not have to be stored as a physical entity. "The only criterion should be whether someone can perform a task and get the same record out every time.

Technically, Childs views the problem as "drawing" maps between incompatible types of secondary storage. The solution lies in building subsystems by modeling each storage device using extended set theory, a branch of mathematics that Childs conceived. Using this approach, he can capture the precise internal structure and characteristics of any storage device and simulate the storage environment. Once performance and capacity have been mathematically modeled, "mapping even between incompatible devices is an almost trivial task."



David L. Childs devised the extended set theory. At Set-Theoretic Information Systems, he has applied the concepts to set processing and relational systems. He holds a BS and an MA from the University of Michigan.

"These new systems will be on the go continuously, and they'll never go down." That means that their data bases will have to be maintained, modified, updated, or completely changed while they are running, so automated subsystems for storage management will become critical.

"Sometimes," Childs speculates, "I think we're still toying with computers just to keep our hands on the steering wheel. But subsystems can do the driving for us, and do it better." □

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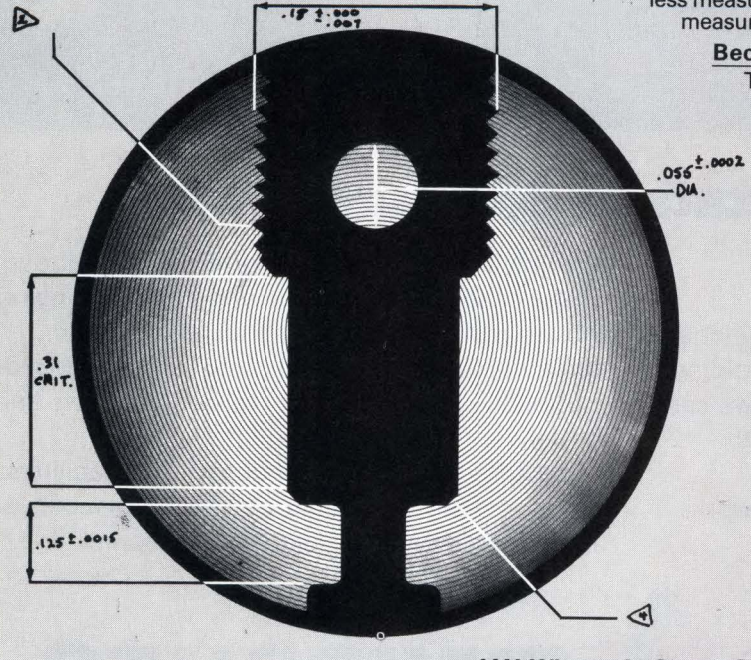

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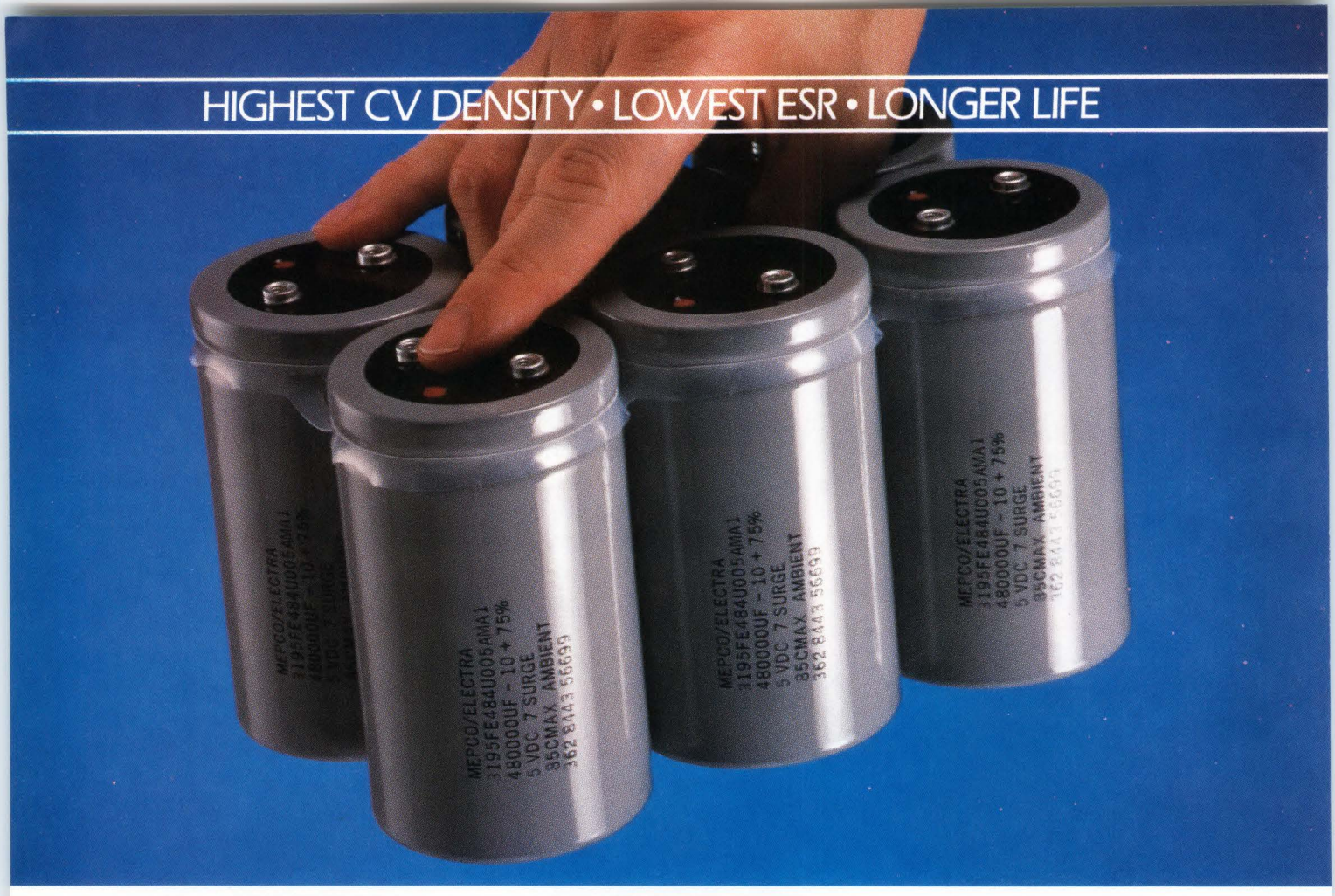

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3194 High Perf. SMPS Input	290 to 11,000	150 – 250	–55 to +105	
3195 High C per volume	2,800 to 1,200,000	5 – 100	–40 to +85	
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Clever techniques adapt CMOS layout software to Schottky TTL circuits

With some tricky maneuvers in the design stage, placement and routing packages geared for CMOS prove acceptable for TTL.

Though industry-standard placement and routing packages afford a safe and fast way of producing cell arrays, they usually are optimized for CMOS designs. TTL designers, for the most part, are left out in the cold, literally forced to handcraft their cell arrays.

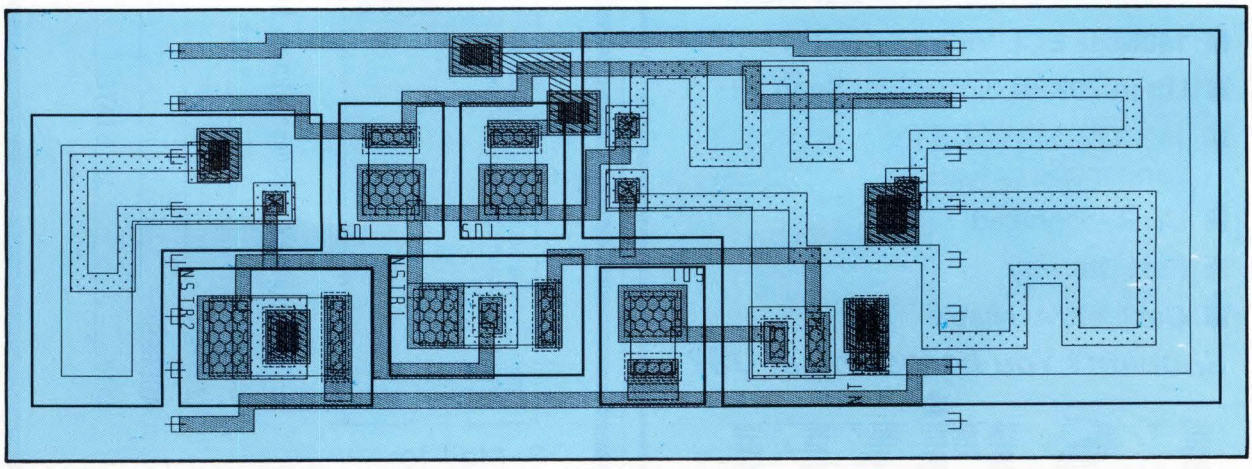
Designers at Siemens AG (Munich, West Germany) have broken that barrier, devising a shrewd strategy for adapting CMOS-optimized software to Schottky TTL arrays—without the 50% size increase normally incurred with that software.

Mitch Beedie

TTL designers encounter two basic problems that complicate the use of CMOS software packages. First, the circuits consume significantly more power than their CMOS equivalents, meaning that resistors with values of up to 20 kΩ must be placed between the circuit elements and ground or V_{CC}. Second, TTL's high output current drive demands power distribution lines with a heftier capacity than provided by either CMOS power lines or TTL signal lines.

A conventional software package would solve those problems by placing the current-limiting resistors in the TTL cell itself consuming silicon area unnecessarily. When manually constructing TTL cells, however, designers normally opt for putting them in the base diffusion region, which lies beneath the routing channels outside the cell. Because CMOS arrays have no such current-limiting requirement, the placement and routing packages cannot accommodate that structural positioning.

Siemens circumvents that obstacle by literally deceiving the placement and routing algorithm. It informs the algorithm that a cell is 150 μm shorter than its actual length



By tricking the placement algorithm into thinking that a TTL cell is 150 μm shorter than it actually is, Siemens can lay interconnections over current-limiting resistors in the base diffusion region—something that CMOS-optimized layout packages cannot do. Here the software puts down the U-shaped resistors so that they project 50 μm over the left end and 100 μm over the right end.

INTERNATIONAL NEWSFRONT

and then fits U-shaped resistors into the extra area (see the figure). Using that information, the algorithm responds by placing the interconnection lines over the base-diffused resistors.

Siemens defines a minimum routing channel width of 200 μm, a figure that prevents overlapping of resistors in different cells. As a result, the TTL cells can be packed more tightly, a trick that ultimately enables the software to cut chip area by up to 40%.

The device can be shrunk further by manually retouching the automatically routed lines on the chip's periphery. In double-metal CMOS circuits, the routing algorithm reserves the first metal layer for X axis interconnections and the second layer for Y axis connections. That treatment proves no problem for CMOS arrays, since the power lines can be as thick as the other connections.

The power lines of TTL circuits, however, must be much heavier than other connections so that they can handle high current drain from many bus drivers. Thin lines, in addition, have too high an inductance, causing unacceptable spikes.

Siemens' solution is straightforward: It leaves the channels between cells intact but routes areas on the periphery of the chip differently. In the I/O region the first metal layer is given to cell interconnections, the second to power lines. When interconnection lines in the first layer must cross, designers manually lay down small bridges to areas in the second layer that are not used by the power lines.

The entire placement and routing technique is now being used in a new generation of Schottky TTL support chips for the 8086/8088 microprocessor family. The chips are about the same size as hand-designed circuits, and were automatically placed and routed using industry-standard software packges, in only a few weeks.□

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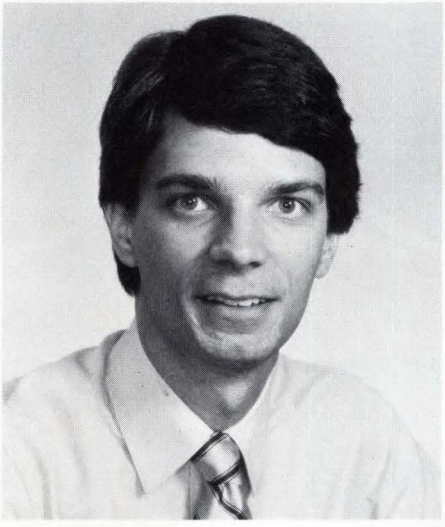

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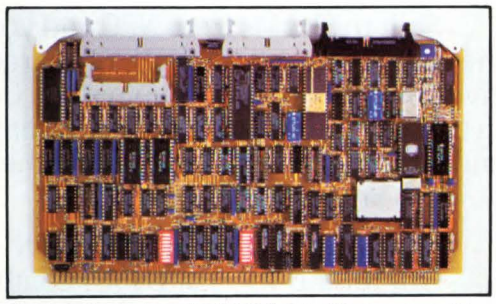
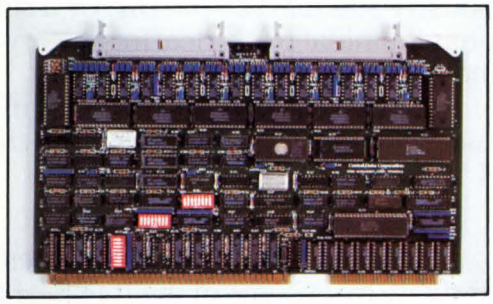


The new **Multibus Multi-Media Controller** is the industry's first to support up to 12 storage media — four each 5¼" Winchester disks, floppies and QIC-02 streaming tape drives, and at an economical price. On-board buffers provide 1:1 interleave transfers and the board supports both bus-vectored and non-bus-vectored interrupts. The board self-tests internally and corrects up to 11-bit burst errors with a 32-bit ECC for Winchester drives. For even greater performance, an optional iLBX* DMA interface is available with the board's (80188) 8/16-bit processor. The **B1030** is available in 100 up pricing at $895.



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INTERNATIONAL MEETINGS

Cadcam International Show, Jan. 8–10. National Exhibition Centre, Birmingham, England. Peter Walker or Landy Hashimi, PWA, 32 Fitzroy Square, London W1P 5HH; (01) 388-9871.

Micro-Computer '85, Jan. 29–Feb. 3. Frankfurt, West Germany. Philippe Hans, German American Chamber of Commerce, 666 5th Ave., New York, N.Y. 10103; (212) 974-8856.

Middle East Electricity and Electronics Exhibition, Feb. 2–6. Jeddah Expo Center, Kingdom of Saudi Arabia. Len Bennett, Logistics, 237 Park Ave., 21st floor, New York, N.Y. 10017; (212) 551-3530.

AFIPS–Asia '84, Feb. 14–March 2. m.v. World Wide Expo, Tokyo, Osaka, Kitakyushu, Taipai, Hong Kong and Singapore. AFIPS, 1899 Preston White Drive, Reston, Va. 22091; (703) 620-8926.

Autotech Hong Kong '85, March 7–8. Hong Kong. Autotech Hong Kong '85, Hong Kong Productivity Center, 12th floor, World Commerce Center, 11 Canton Road, Tsimshatsui, Hong Kong; 3-7235656.

Componentes Electronicos '85, March 12–15. Mexico City, Mexico, March 19–22, Guadalajara, Jal., Mexico. Raquel Polo, United States Trade Center, Liverpool 31 Col., Juárez 06600, Mexico, D.F.; or PO Box 3087, Laredo, Texas 73044.

The Scottish Computer Show and Conference, March 12–14. Anderston Exhibition Centre, Albany Hotel and Holiday Inn Hotel, Glasgow, Scotland. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TWI 3SZ, England; (01) 891-5051.

China Tronic '85, March 14–19. Tianjin Exhibition Centre, Tianjin, Peoples' Republic of China. Asdale Exhibition Services, 109-111 Gloucester Road, 21st floor, Wanchai, Hong Kong; 5-8920511.

Comtel '85, March 18–20. Infomart, Dallas, Texas. Comtel '85, International Computer & Telecommunications Conference, 5080 Spectrum Drive, Suite 707E, Box 17, Dallas, Texas 75248; (214) 631-6482.

Automatic Testing and Test Measurement '85, March 19–21. Rhein-Main-Halle, Wiesbaden, West Germany. Network Events Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, England; (0280) 815226.

Networking '85, March 23–31. Tokyo, Japan. Brad Ketchum, INC. Publishing Corp., 38 Commercial Wharf, Boston, Mass. 02110; (617) 227-4700 or Aki Tsurukame, Pacific Catalyst Group, 650 Grand Ave., Suite 1004, Los Angeles, Calif. 90017; (213) 614-0049.

IEEE Infocom '85, March 25–28. Washington, D.C. Celia L. Desmond, IEEE Infocom '85, Room 1855, 160 Elgin St., Ottowa, Ont., Canada K1G 3J4; (613) 239-4510.

Bit '85 Computer Show and Conference, March 26–29. National Exhibition Centre, Birmingham, England. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TW1 3SZ, England; (01) 891-5051.

Comdex In Japan, March 26–28. Tokyo International Trade Center, Tokyo, Japan. Milton Berns, The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

32nd International Electronics, Energy and Aerospace Exhibition (Riena), March 26–31. Rome, Italy. Riena, Via Crescenzio 9, 00193 Rome, Italy; (06) 6569343/4/5.

Internepcon/Semiconductor International, March 27–30. Korea Exhibition Center (Koex), Seoul, Korea. Cahners Exposition Group, 7315 Wisconsin Ave., PO Box 7007, Washington, D.C. 20088; (301) 657-3090.

Unix Systems Expositions '85, April 2–4. Palais des Congres, Paris, France. Networks Events Limited, Printer Mews, Market Hill, Buckingham, MD18 1JK, England; (0280) 815226.

Electronics and Electrical Engineering Exhibition, April 17–24. Hanover, West Germany. Hanover Fairs, PO Box 338, Whitehouse, N.J. 08888; (800) 526-5978 or (201) 534-9044.

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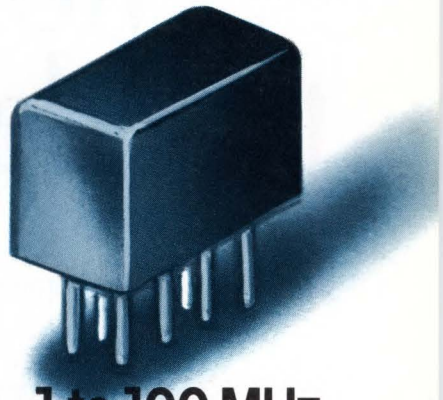

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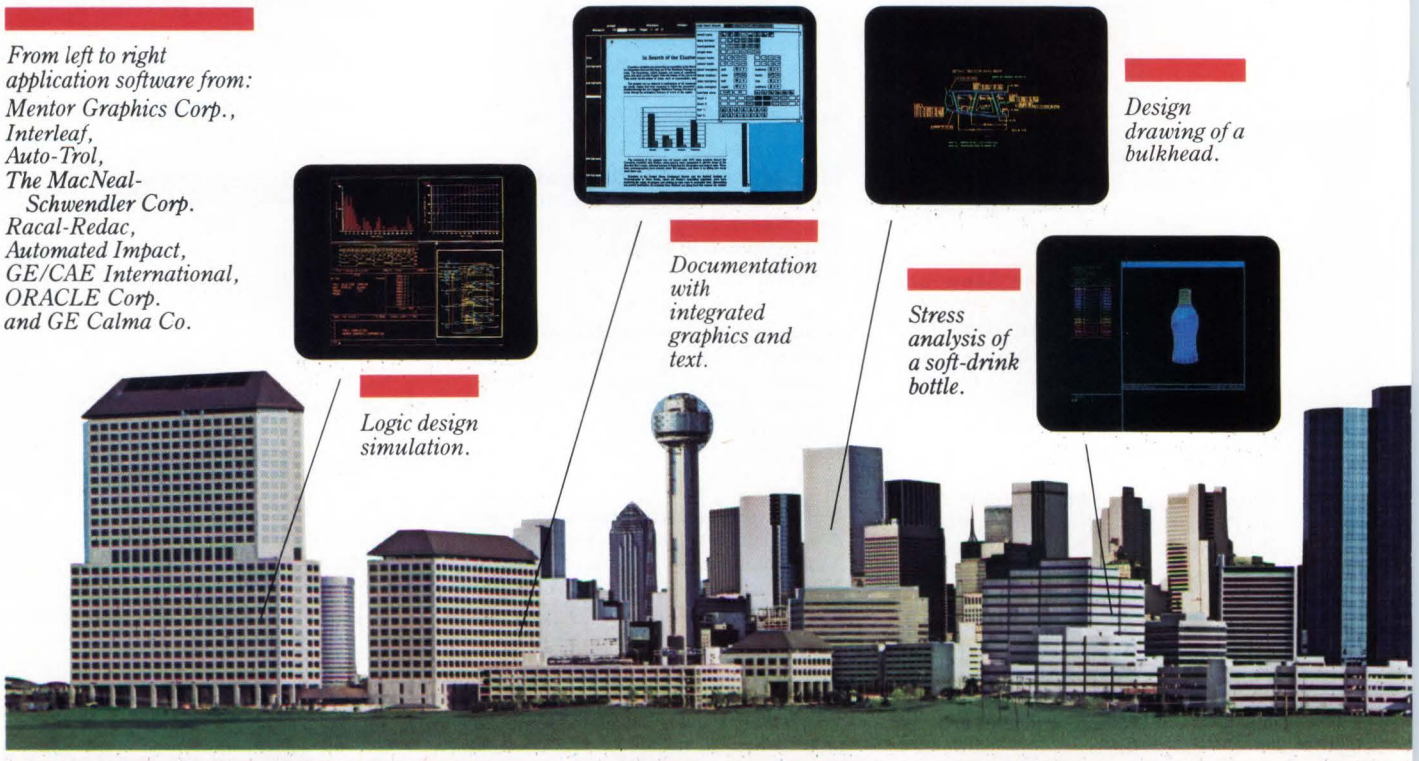

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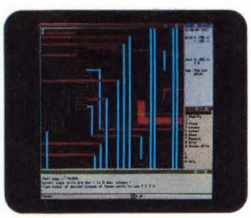

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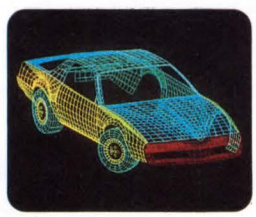

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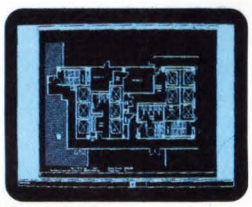

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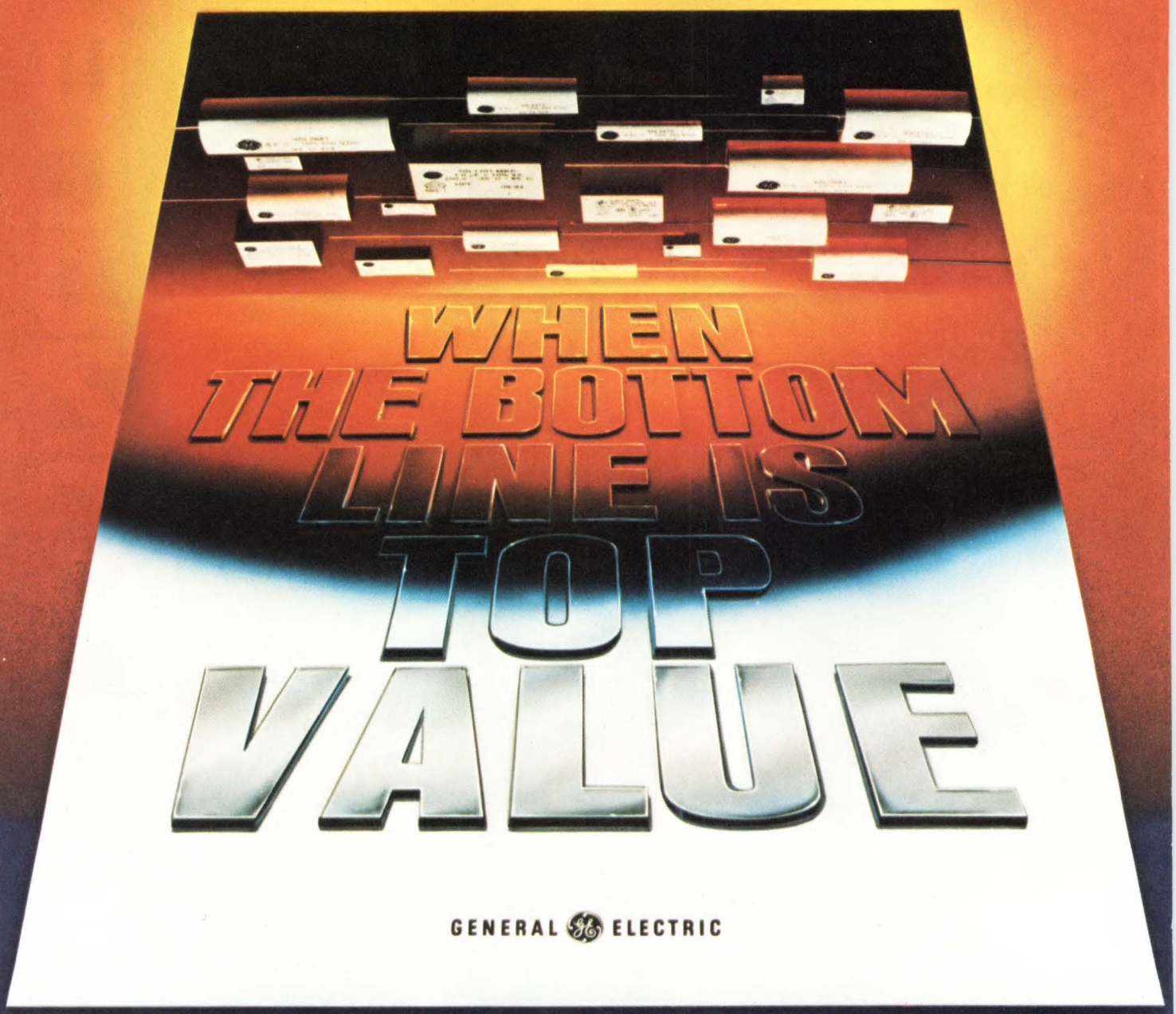

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LM212	48 × 640	270 × 63 × 14 max.	
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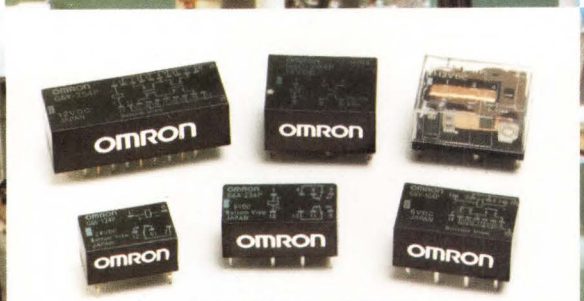
CIRCLE 47



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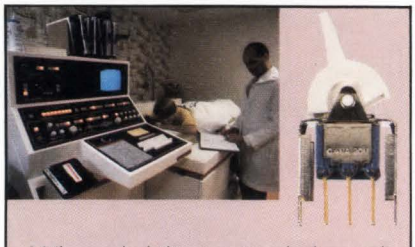

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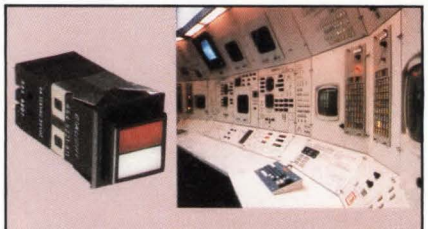

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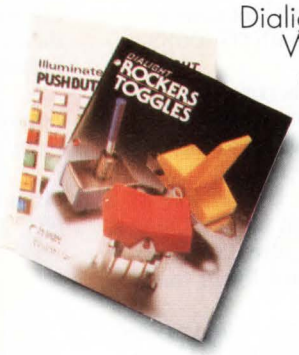

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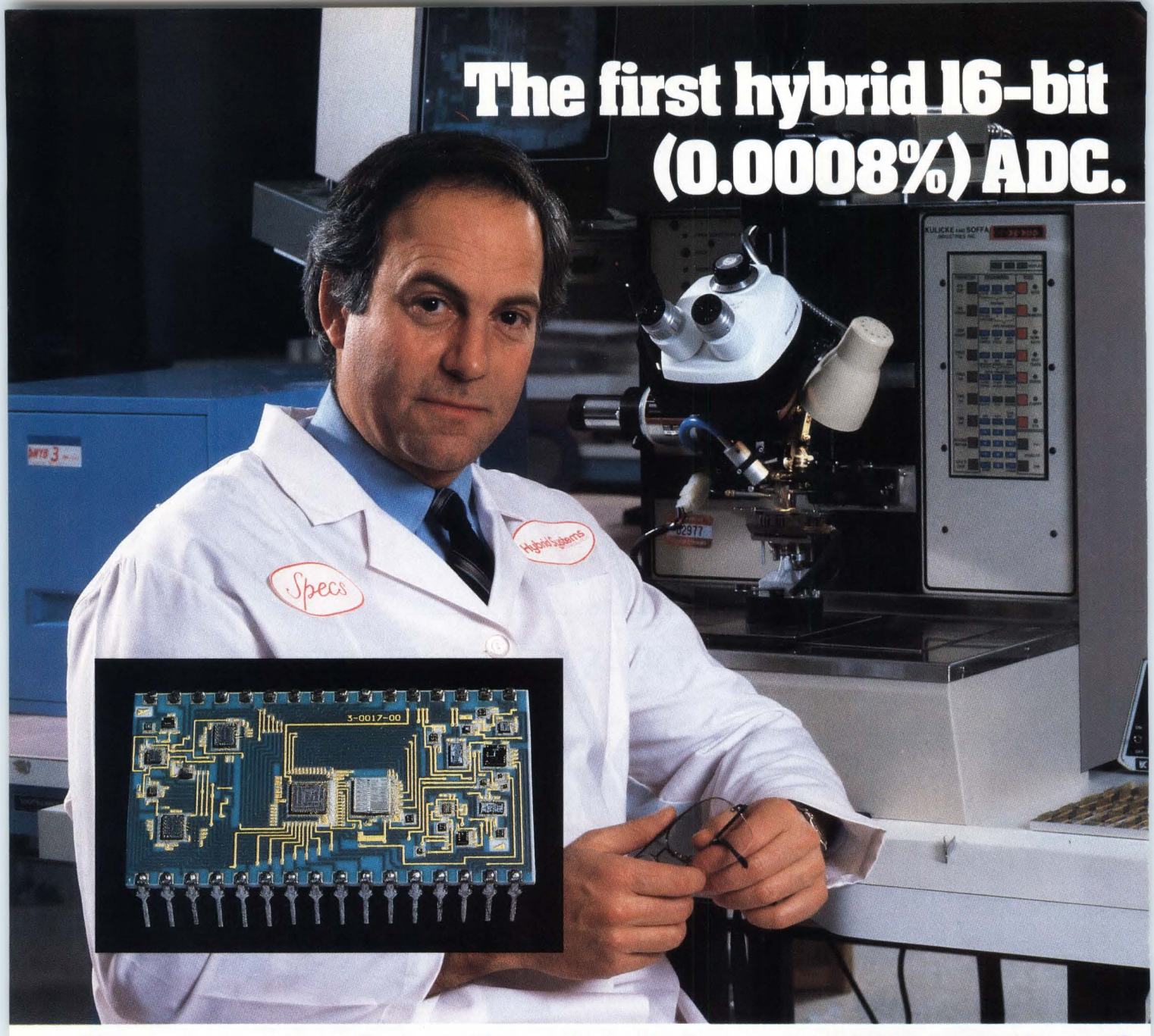

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Precision Data Converters, Hybrid Data Acquisition Systems, and Thin-Film Products.

CIRCLE 50

Software Standards

Designer's Reference

Software is maturing. It has a long way to go, but it has reached the point at which the benefits of standardization clearly outweigh its inhibitory effects. The growing attractiveness of networking, the need to process the same information on different computer systems, and the obvious desirability of having to write just one version of any given application program are all combining to convince even the most independent of designers of the need to standardize.

What standards to adopt, and when to adopt them, are questions that have yet to be answered. In the field of networking, software will probably follow in the footsteps of hardware—that is, several standards are likely to emerge. At present, however, no single set of software protocols, suitable for both local and global networks, has emerged. As our progress report on software standards for networks indicates, work in this direction is proceeding apace. Already the International Standards Organization has released standards for two of the seven layers of its Open Systems Interconnection (OSI) reference model.

For some computer users, the software standards problem is not so much real-time communication as it is simply commonality of language. Chip and board designers, for example, need a standardized hardware description language (HDL), so that different parts of the design process—including test generation—can be carried out by different people on different machines. Progress in this area is covered in our second report, which is on software standards for computer-aided engineering.

The third report in this year's Designer's Reference is on operating systems, specifically Unix. Despite the attractiveness of having to write only one version of any given application program, there is just about no hope of ever developing a single universal operating system. One might think, however, that a single version of a popular operating system like Unix might come into being. But no, as the third report points out, there are four main Unix camps within each of which some progress toward standardization is being made.

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ITT COMPONENTS

CIRCLE 52

Software Standards

Designer's Reference

Local and global networks are inciting the industry to develop standard protocols, albeit slowly

Computer networks are setting the course for distributed processing systems. Besides sharing expensive resources and passing documents back and forth, users can send jobs off to idle computers in the network while their local machine is occupied with something else. In a more advanced network, the computer can automatically break down jobs and send them to other machines, giving the system the power of a mainframe at a fraction of the cost. Moreover, the network could be incrementally expanded to meet changing processing needs.

Though the advantages of global and local networks have already been enjoyed by engineers and others, their benefits ultimately lie in the future, awaiting the establishment of standard protocols for hardware and software. Hardware protocols—such as IEEE-802.3 (Ethernet) or IBM's 2-Mbit/s broadband local network—specify how bits of data travel from one computer to another; software protocols spell out which bits are transferred and what they mean.

Curtis Panasuk

Because of their more abstract nature, software protocols are more difficult to define than hardware ones. Consequently no complete set of software protocols has emerged from any major standards organization. Preliminary steps were taken by the International Standards Organization, which last year released a network protocol (layer 3) and a transport protocol (layer 4) representing only two layers of the seven-layer Open Systems Interconnection (OSI) reference model.

In the absence of official software standards, manufacturers and other organizations have been busily creating their own protocols. A decade ago, long before private companies even embarked on their protocol project, the U.S. Department of Defense developed its Transmission Control Protocol, or TCP, the specifications of which it released immediately.

Three years ago Xerox Corp. (Stamford, Conn.) released the equivalent of layers 3 and 4, which

it calls the Transport layer, along with layer 6, which it calls the Courier, for the Xerox Network Systems protocol, defining them in a functional specification. Though the company has been using a complete protocol since 1981, it publicly released the application layer specifications only last April.

IBM Corp. (Armonk, N.Y.) only recently came on the local network scene: In August it announced PC Network, specifying broadband hardware and several high-level software layers. Though naturally geared for the IBM PC personal computer, the network might well become a de facto standard for any type of computer.

IBM's interest in computer communication did not start with small computers. Its System Network Architecture (SNA) aims at mainframes, and though it proves too inefficient for today's emerging local networks, it can easily handle global systems. Similarly, the X.25 standard of the International Consultative Committee of Telegraphy and Telephony (CCITT) is suited to global networks, but its expensive error-checking mechanism consumes too much processing power for local networks.

The requirements of global and local networks are quite different; consequently it is difficult to design a software package to do both jobs. Consider the basic differences between the two network types. Local networks connect computers over about a mile square with high-speed and reliable hardware. Global systems send data over much longer distances but with less reliable connections—telephone lines, terrestrial microwave radio, and satellite links (Fig. 1). Those connections are susceptible to dropouts caused by bad weather, switching noise, and other conditions.

Most local network software protocols assume a virtual connection that depends on data traveling through the network continuously. Some damaged data could pass, but the system could not tolerate the 1- or 2-second dropouts encountered in global networks. On the other hand, global network software must be able to send data in small packets, carefully logging which packets have been sent or received. In that manner, if a disturbance arises, the system could send the packets again later.

TCP, SNA, and X.25 all have that "datagram" capability and thus are suitable for global networks. However, the ISO's OSI model and the Xerox Network Systems protocol cannot handle datagrams; thus they are limited to local networks.

The ISO is working to rectify that problem by adding the capability to its transport layer. In doing so, it would give the communications industry a worldwide software standard, one that would make possible a single prefabricated software package that could handle any local or global network.

Already the networking industry has seen some prefabricated software packages, though they do not represent a standard protocol. Nevertheless, most adhere to some aspect of the ISO's classification system, which serves essentially as a guide to developing protocols and divides networking into manageable "chunks."

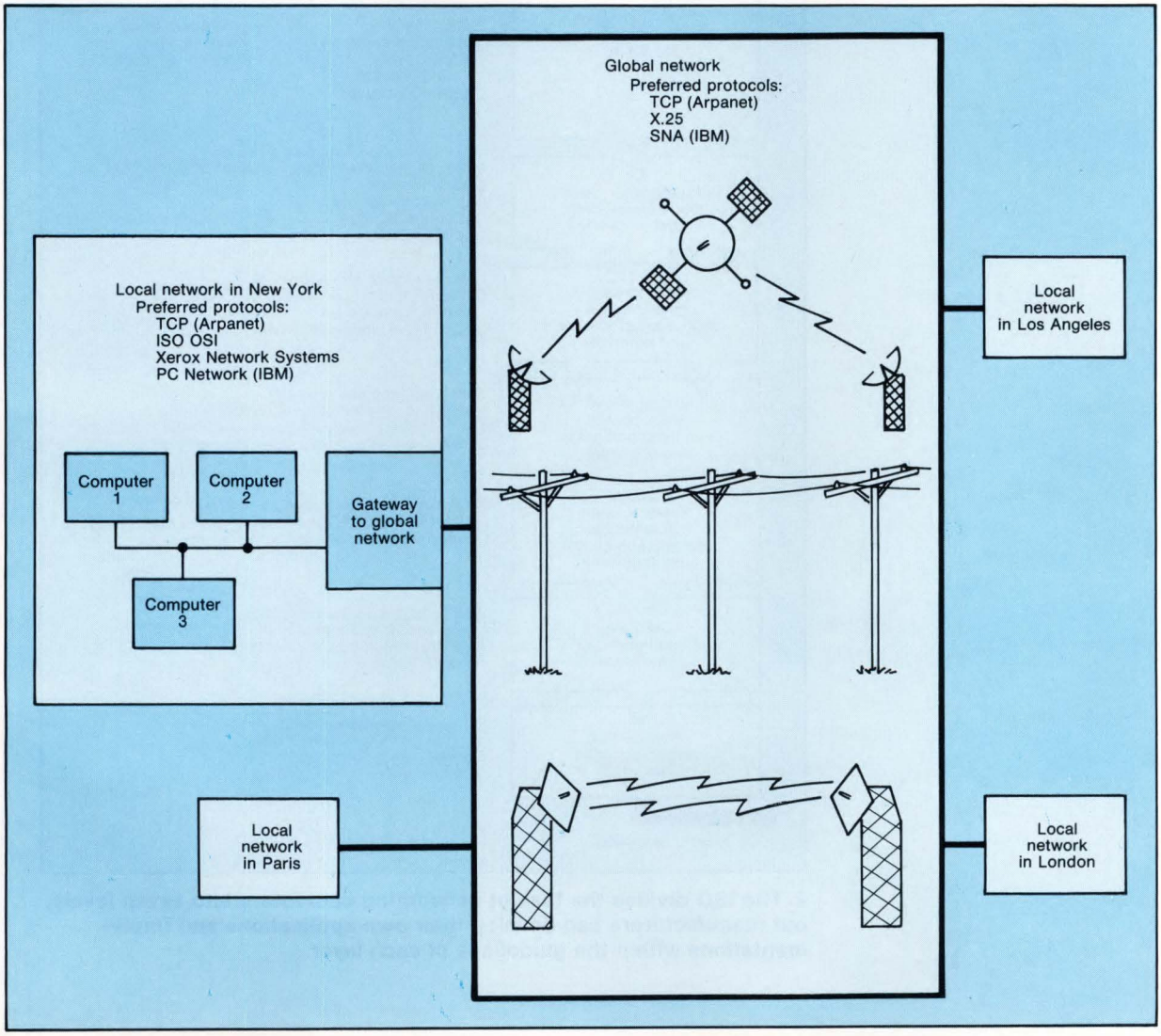
The model divides networking into seven layers, each of which has independent functions (Fig. 2). Technology advances can be applied to the appropriate layer without affecting the other layers. A perfect example is the hardware evolution of the two lowest layers—from a boardful of chips to a microprocessor-firmware combination to a pair of dedicated chips such as those available from Intel, Seeq, and Advanced Micro Devices. In a similar fashion, software layers might be improved with better algorithms or eventually converted into hardware without affecting the layers above or below them.

Layers 1 through 6 are the equivalent of an operating system upon which application programs can be written. Layer 7 hosts another class of programs—subroutines that are called by the application programs, which themselves become the user-machine interface. The amount of code written at layer 7 vastly outweighs the amount written for all six other layers.

The ISO's process of creating standards for these different layers is a formal procedure that starts with a committee of professionals who create a draft. After review by members

worldwide, the committee decides which comments and recommendations to incorporate into the draft. The member countries then vote on the draft, and if a majority approves it, it becomes a draft international standard and is redistributed for further scrutiny. If, after subsequent modification, it receives another majority vote, it is cleared as an international standard. Right now only layers 3 and 4—network and transport levels, respectively—are international standards, but the others are in various stages of proposals and drafts.

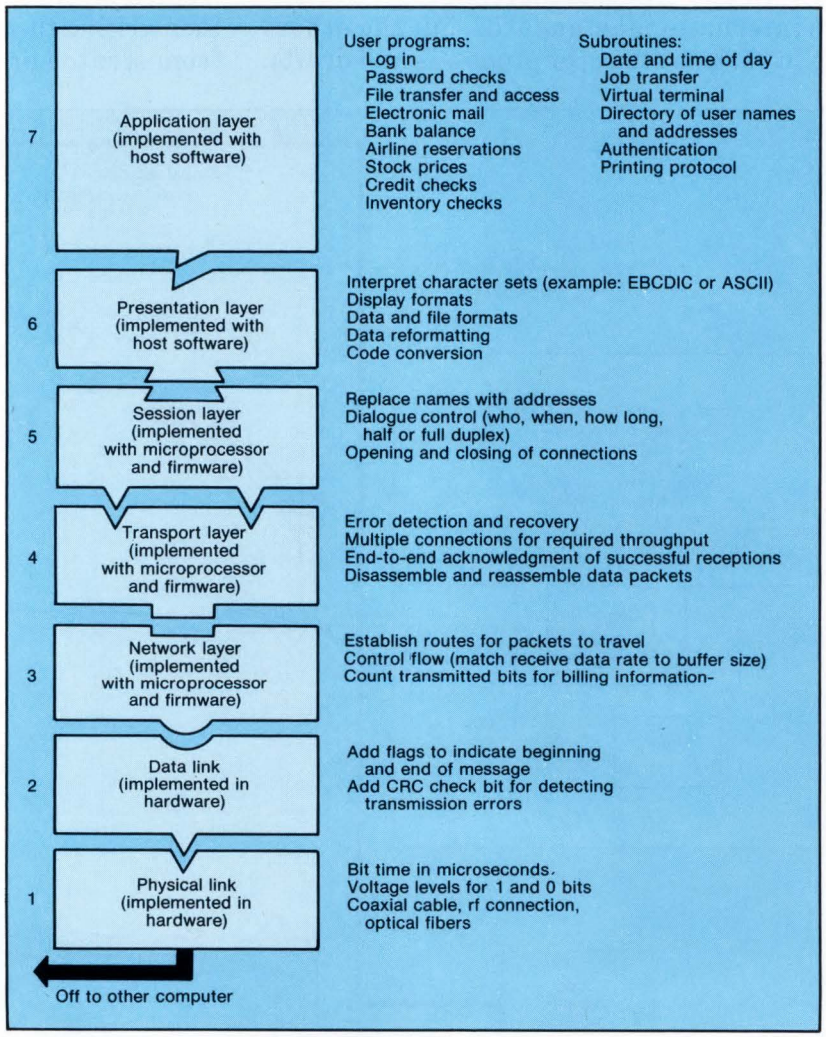
With the standard definition of layers 3 and 4 and with the IEEE standards for the physical and data link hardware, data can flow between computers from different manufacturers. At the National Computer Conference earlier this year, Intel, Hewlett-Packard, IBM, Digital Equipment, and several other industry heavyweights gathered to demonstrate an unusual network. All independently implemented layers 3 and 4 of the ISO standard, either writing the software for those two layers from scratch or buying it—in the form of a



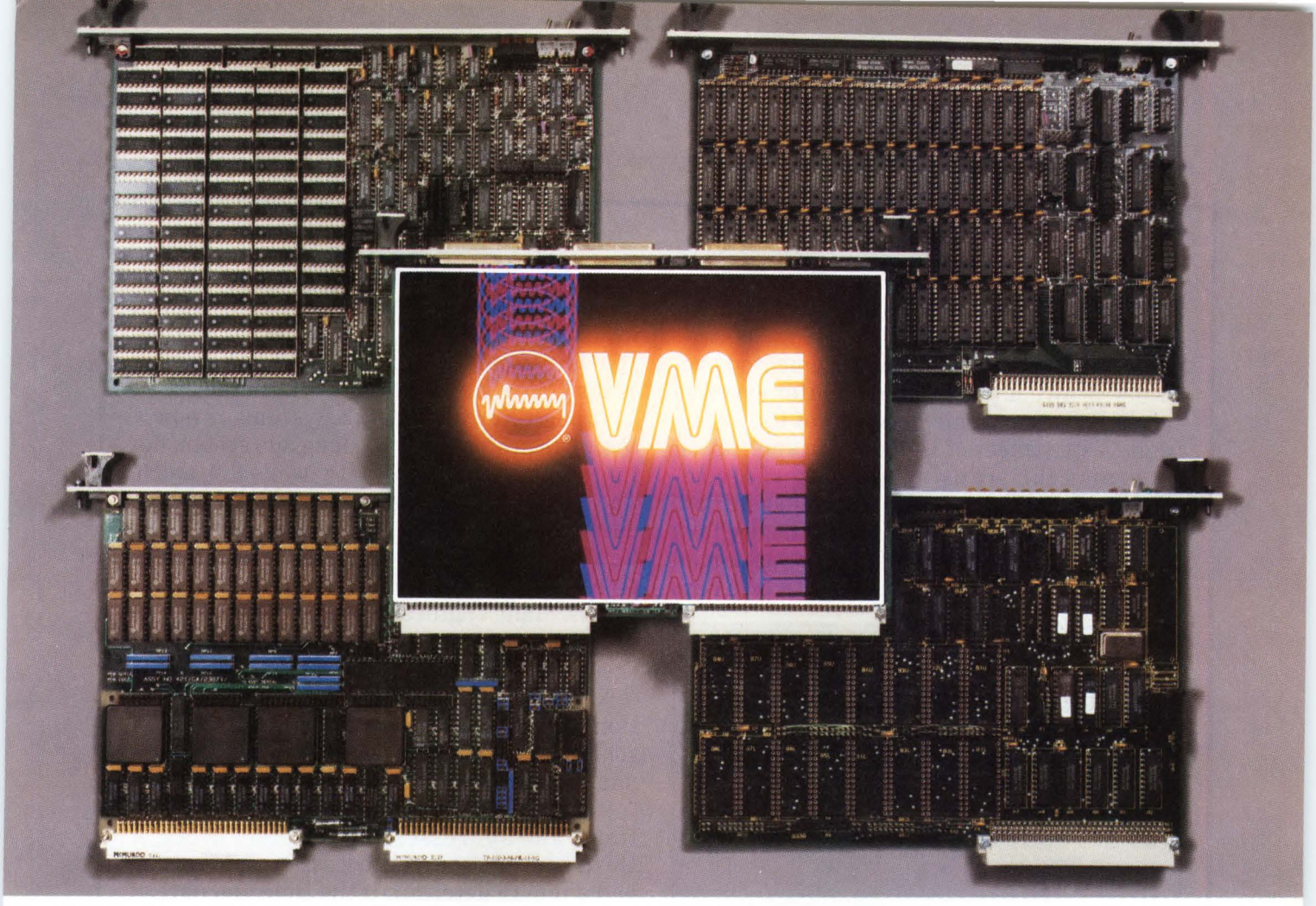
1. Ideally, networking software should be independent of hardware. In reality, the protocols that work best over the telephone-based global networks are not well suited to low-noise high-speed local networks. The Department of Defense's TCP, developed for Arpanet, works well in both types of networks.

board—from Intel or Interlan. The companies also used two hardware standards, the IEEE-802.3 CSMA/CD and the IEEE-802.4 token-passing bus, to show that the software layers were independent of the hardware connection. They agreed to one file-transfer application program, which they implemented on top of layers 3 and 4. Thus they could transfer files among the 10 different computers that were connected to the network.

Since the ISO specification is not complete, an engineer creating a network system has two alternatives. He can base the system on ISO layers 3 and 4 and then add his own implementation of layers 5, 6, and 7, even though his version will probably have to be rewritten when the ISO finalizes those upper layers some time late next year. The other approach



2. The ISO divides the task of networking computers into seven levels, but manufacturers can develop their own applications and implementations within the guidelines of each layer.



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1 Mbyte DRAM*	PME 512EP	•		8/16/32	150	270
3/4 Mbyte DRAM	PME 256EA		•	8/16/32	150	300
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opts for an existing structure—TCP or Xerox Network Systems, in particular—that carries all the required layers.

TCP, one of the most well-documented protocols, is already used by computer systems throughout the country because of its origins in the Department of Defense. Its application programs can transfer files and share resources like printers and plotters. In addition, several ready-made software packages have been devised by companies like Advanced Computer Communications Corp. (Santa Barbara, Calif.), whose software runs on minicomputers, and Excelan Inc. (San Jose, Calif.), which puts its software on Ethernet boards. TCP is also part of Unix version 4.2, developed at the University of California at Berkeley.

Net BIOS activities

Expanded support for networking
- File sharing
- Record locking down to byte level

Program interface with network software
- Redirection control
- Installation checking
- Direct execution of Net BIOS functions
- Multiple servers

IBM PC Network program

Full-screen interface

Redirector
- Allows use of shared printers
- Allows use of shared disks and directories
- Provides capability to send messages

File servers
- Password protection
- Variety of access modes supported (e.g., read only)
- Record locking to control multiple updates

Printer server
- Shared use of named printers
- Password protection against unauthorized access
- Automatic spooling and queuing or output
- Queue management facilities on server station

Message server
- Interactive message editing, transmission, reception
- Preserves foreground application context
- Automatic notification or logging to disk printer

Though Xerox Network Systems is now a complete protocol, not too long ago system designers could work only with layers 3, 4, and 6. The first two (the Transport product) transfer data reliably between computers, the last (the Courier product) sets up high-level subroutines that can be called by application programs. Many engineers decided to go with the well-defined layers and fill in the blanks with their own implementations.

Xerox has since introduced its own application software, including one program that can send a document to any printer in the network and another program that essentially acts as a "clearinghouse," holding the names, descriptions, and addresses of all system users. A third package controls access authorization, and a fourth determines the time and date of transmissions. Advanced Computer Communications develops XNS software in addition to TCP packages.

Faced with the problem of how to link its personal computers, IBM chose to develop its own software protocol. Its PC Network promises to have a major impact on data communications, diverting engineers' attention from the ISO standards. PC Network provides workable software protocols up through the equivalent of layer 5 of the OSI Model. The interface with this network software is known as Net BIOS, and like MS-DOS, it will foster an explosion of application programs—from electronic mail and airline reservations to inventory control and hotel reservations.

Net BIOS handles such functions as file sharing and record locking—down to the byte level. Record locking ensures that if someone is using a file no one else can access it; thus there is no chance that one user might be loading a file with new information while another one is accessing the old file information. Net BIOS works with passwords, shares the use of named disks, and undertakes similar duties (see the table, opposite).

Those functions, coupled with the inevitable

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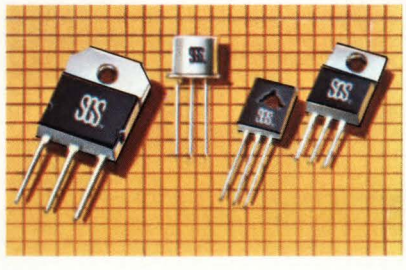

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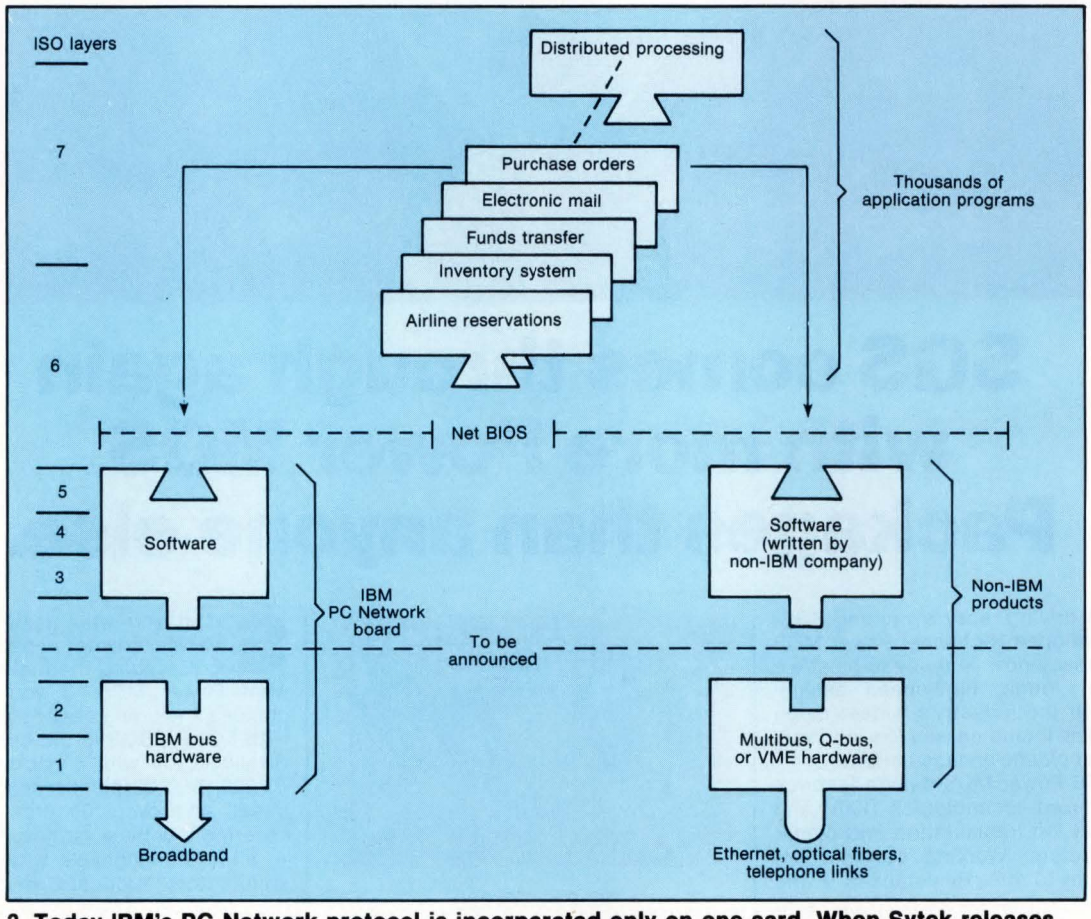
Created by Martz & Assoc.

CIRCLE 54

application programs, may make PC Network the software protocol of choice for new networks. Today, however, the protocol is available only on an IBM board that ties into the personal computer's bus on one end and a 2-Mbit/s broadband connection on the other.

Engineers are currently stymied in applying the protocol to Q-bus, Multibus, or VME-based systems. Moreover, the broadband connection means that the protocol cannot be adapted to Ethernet or optical links. Finally, since the software is built into a board, there is no way to write drivers for the protocol.

Many of these limitations are expected to end when Sytek Inc. (Mountain View, Calif.), which actually designed the hardware and software specifications for the PC Network protocol, releases a complete description of the structure. Hardware and software makers will quickly translate the description into a tremendous assortment of network building blocks (Fig. 3), which will ultimately link computers and peripherals from IBM and many other companies. □



3. Today IBM's PC Network protocol is incorporated only on one card. When Sytek releases the specifications, an explosion of software and hardware products will no doubt make it easy for the PC Network to tie together computers from other companies.

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CIRCLE 55

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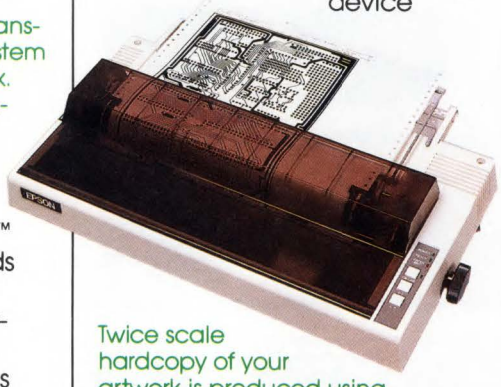

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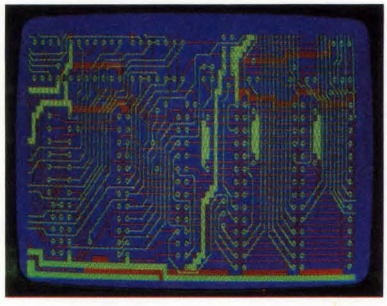

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Software Standards

Designer's Reference

Languages and data formats vie as potential standards in the CAE design loop

Computer-aided engineering (CAE) is a nightmare of incompatible formats and a Babel of different languages. No standard hardware description language exists, and because each manufacturer's workstation and software forms an integrated package, translators must be devised.

The translation problem is complex because the number of translators required grows as the square of the number of workstations involved. (To be precise, N workstations require $N(N-1)$ translators. Thus, 12 translators are needed before a network of four workstations can "speak" to each other.) And, with no standard data format for transmitting a finished design to a silicon foundry for fabrication, even more translation may be required.

The standards ferment

Plenty of work is now underway to standardize both hardware languages and data formats and, five years from now, a chip designer may be able to buy a standard that covers all elements of design, interface and communication exchanges. But today, no single solution exists. The current situation is chaotic, with independent standards groups, the U.S. government, and even individual manufactuers all formulating their own versions, none of which do the whole job.

Vying with each other as possible standards are hardware description languages developed by two commercial companies—TIDAL and GAIL from Texas Instruments and Daisy Systems Inc., respectively. A third language (VHDL) is being developed under government contract. Also playing a role is a method for storing CAD data developed by commercial firms (The Electronic Design Interchange Format—EDIF). Competing against it is the Initial Graphics Exchange Specification—IGES. And, if that is not enough, standard means for defining terms and definitions for digital gate arrays (already defined in EDIF) are being developed by the Electronic Industries Association's Joint Electronics Design

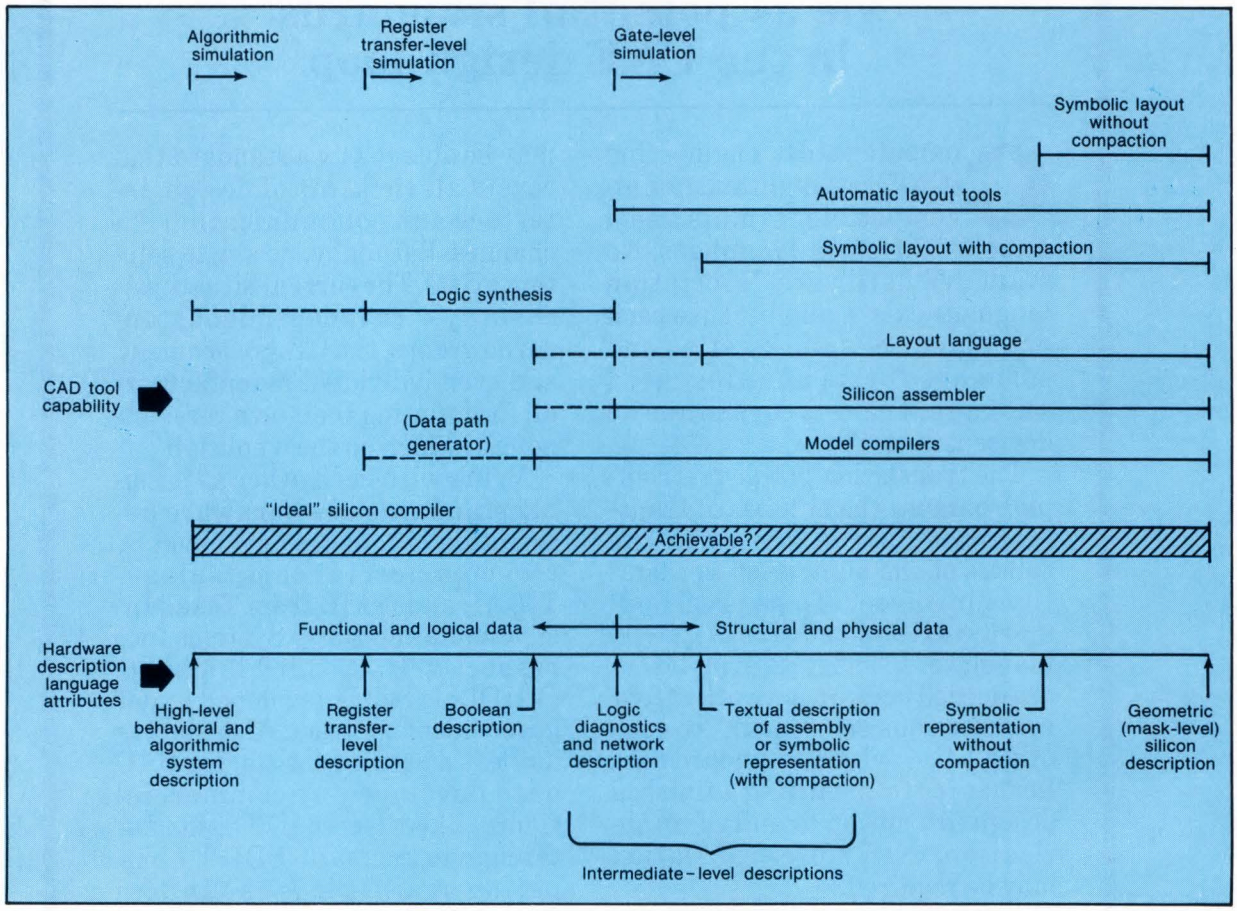
Carole Patton

Engineering Council—JEDEC.

A procedural layout is needed in circuit design ("Do" files, for example) and many workstations use Lisp, now a de facto language standard. But designers also envision a standard hardware description language that can adequately describe the elements of IC design and test, and can store, transmit and even execute design programs (Fig. 1). One such language, an outgrowth of the Defense Department's Very High Speed Integrated Circuits (VHSIC) program, is called VHSIC Hardware Description Language (VHDL). An extension of ADA, it is still being refined, and the timetable for producing an executable version spans several years.

Another contender is the Transportable Integrated Design Language—TIDAL—a hardware description language developed by Texas Instruments Inc. TIDAL was devised but never implemented, though some parts of it are procedural. In fact, many of the structural concepts of TIDAL have since been incorporated into EDIF (Fig. 2).

Still another language, this one addressing layout specification, is the Gate Array Inter-

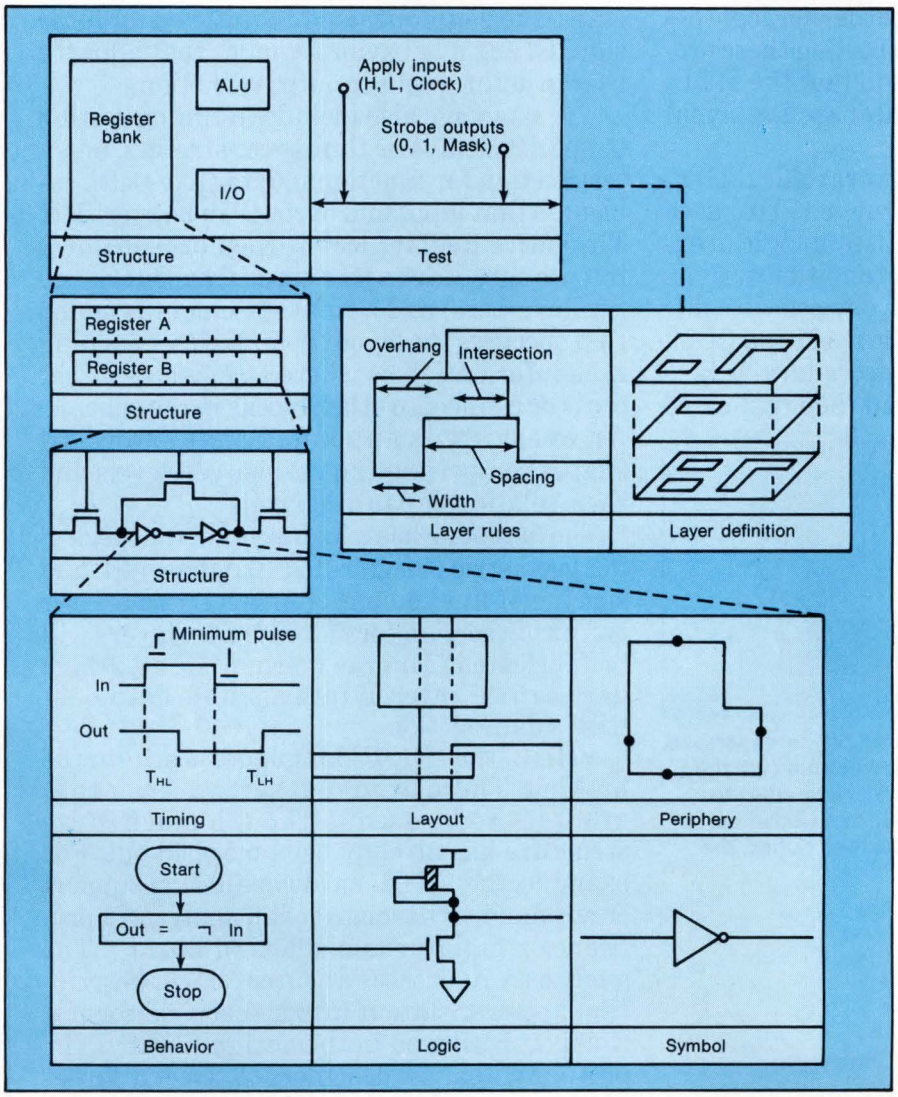


1. The kind of hardware description language being envisioned as a standard must map the entire design process. Computer-aided-design tools do only part of the job; the ideal silicon compiler will automate much of the process, but would still need an architectural description as input.

face Language—GAIL—developed by Daisy Systems Corp. (Sunnyvale, Calif.). It can be used to transfer generic gate arrays and macro designs from library patterns between the gate array manufacturer and the Daisy Gatemaster workstation. It also allows gate-array layouts to be transferred between mainframe-based CAD systems. GAIL does not have the semantic power to detail a logic design. It does, however, fill a gap as a precise way to move layouts between systems. Some aspects of GAIL have also been included in EDIF.

Tracking the development of TIDAL is as good a way as any to understand the needs of chip designers for a working HDL. Initially, hardware description languages were used to drive simulators that provided logic design engineers with logic verification and test abilities such as circuit analysis programs, logic simulators, and test pattern graders. But because each application required a specialized format and input, the designer was required to "speak" many different computer languages fluently.

As design automation took hold, the HDLs were refined to include more precise terms

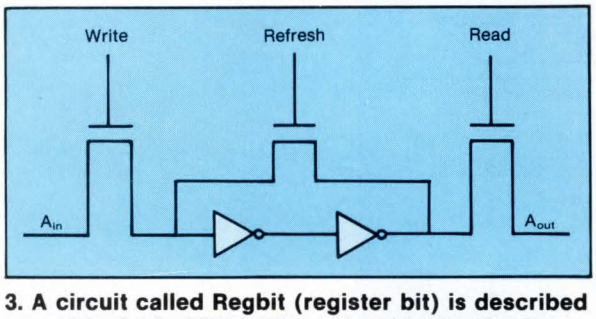


2. Data sections in TIDAL for describing structures, layout, timing, behavior, logic, and even complex layer rules and definitions are included in EDIF.

(like "clock" for registers and "clear" for counters) and more design features (like wiring programs for placement of circuits). More refinements included a hierarchical design concept, beginning with broad specifications and working downward to cell levels. A part of a circuit or chip subsystem that was replicated often was defined as a "macro" so it could be referenced as a single entity.

But, with each HDL creating different data in different formats, data reformatting was necessary at each level, and errors could be introduced. Also, two different databases and two languages were generally required, one for the circuit layout and another for logic design. One of the first steps in pulling these processes together was to consolidate the HDLs and develop one common database for layout applications.

TIDAL is a meld of TI's hierarchical HDL and its test description language (TDL) used to tie gate array and semicustom logic users into the company's design automation system. TIDAL uses cells to describe devices with different I/O characteristics like RAM and ROM. Each cell, which is called a procedural cell, is first designed in software and then replicated to create the complete circuit function. One TIDAL "block" can contain as many as 12 sections that describe circuit functions, and an entire chip design might encompass several TIDAL blocks.



3. A circuit called Regbit (register bit) is described as a "block" in TIDAL. Two other blocks (for the inverter and the MOS transistor) are needed to complete the design. Each block can house as many as 12 data sections that further define the circuit.

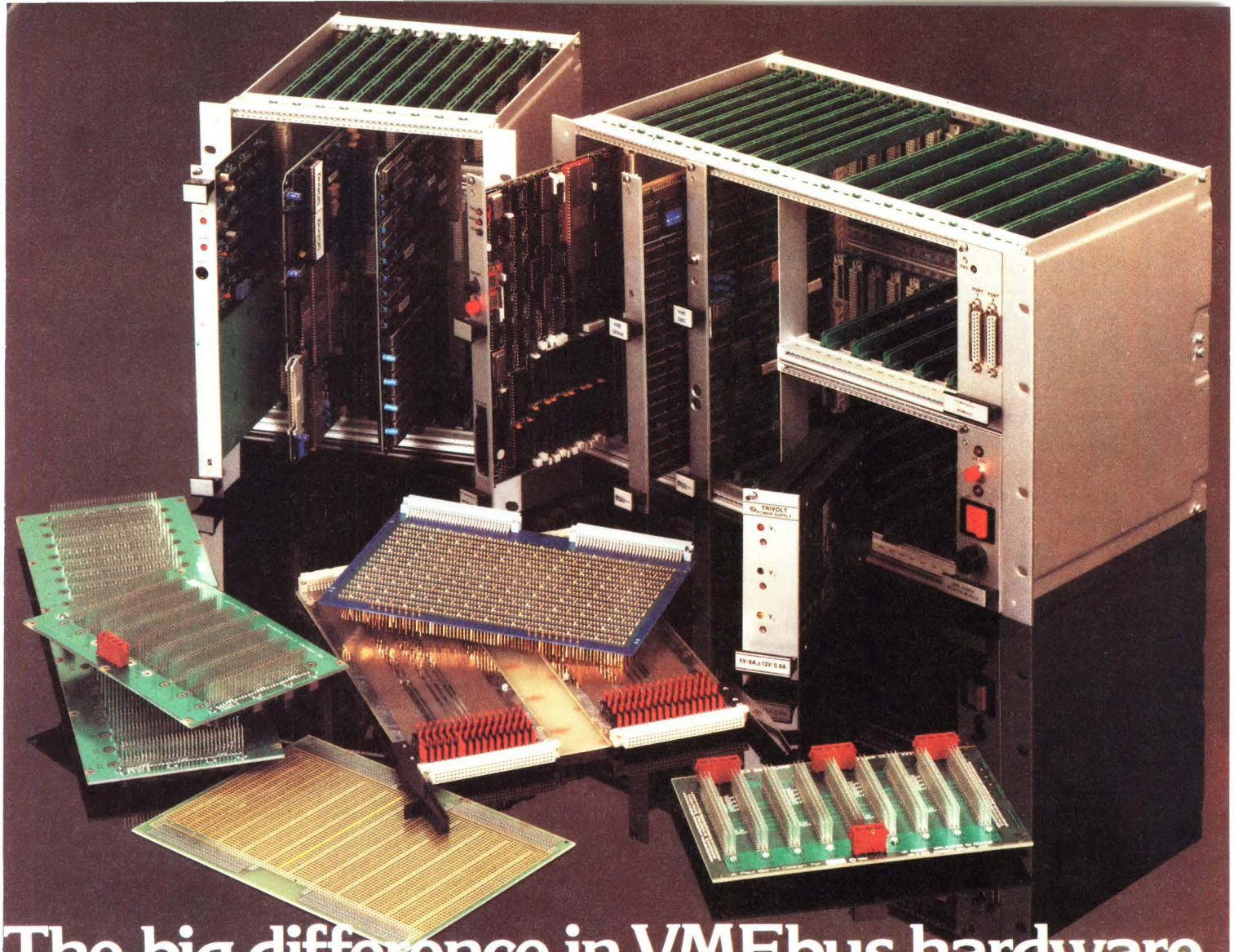
For example, a TIDAL circuit block called Regbit (register bit) consists of three MOS transistors and two inverters (Fig. 3). Two other blocks, describing the inverter and the MOS transistor, are needed to complete the design. In use, a block statement (called Block Regbit) defines the input and output signals (such as A_{in}, write, refresh, read) and the output signal (A_{out}). Following the block statement is a declarative segment used to define any logic signals, and a behavior segment that allows a user to define input to output functions.

The language also includes a timing section to specify delays or timing constraints, and a test section for functional data (like truth tables) so that input and output can be specified. The entire Regbit block is then broken down into its subsections (the three transistors and two inverters) and a final statement is added that specifies the layout boundaries, including such information as where I/O signals might cross or connect to other blocks in the scheme. An overview is appended that shows all shapes comprising the various cell levels and their relationship to other cells.

The language has a logic section for specifying geometric design rules, like the width and spacing of lines on one chip layer, and a layer definition section for showing how layers will be fabricated from the mask. Also, all design data can be entered into a single data base with a data section.

VHDL, the VHSIC language, is still in the making. There is no real software yet that allows it to be used, although much of its structure has already been mapped out. For example, the VHDL hardware design support environment will consist of an analyzer, a profiler, a simulator and a design library. The analyzer will process a source VHDL description and translate it into a specified format that can be stored in the design library. The profiler will allow designers to select a subset of a hardware description for simulation.

Intrinsic to the VHDL structure is the



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CIRCLE 57

concept of a "design entity"—composed of an interface and one or more "bodies." The interface specifies the characteristics of a component that are visible externally, while the "body" describes a component's internal structure. Visible characteristics, for instance, might include I/O ports, their modes and their types, and their generic parameters.

The idea of generic features should enhance the reusability of descriptions, because they represent, essentially, an entire class of objects. Any particular member of that class can be specified by assigning a particular value to the generic parameters, and the parameters themselves can be used to capture technical dependencies . . . like propagation delay, noise margin, or fan-out of hardware components.

Body-building basics

In VHDL, the functional characteristics of a design entity are specified in the body, which is composed of a declaration followed by a group of statements. Declarations describe types, subtypes, etc., while the statements operate on visible data structures and perform any necessary transformations.

In this scheme, a body may be either behavioral or architectural. A behavioral body is one used to represent the functional characteristics of a component in algorithmic terms, much like any program written in a high-level language. Most of the data transformations that take place in a behavioral body are transformations on variables—nouns with assignable definitions.

An architectural body, on the other hand, describes the flow of data. The main category of statement in an architectural body is a guarded signal assignment statement. For instance:

```
if enable = '1' then output (=not data after 5 ns;
and if;
```

Here, "enable = '1'" is the guard that controls the value of the signal "output." The guard of signal assignment is a boolean expression and is evaluated when one or more of its inputs change. The assignment statement is evaluated when its guard is true, and one of its inputs has changed, so any change in signal value causes the evalution of a signal assignment statement.

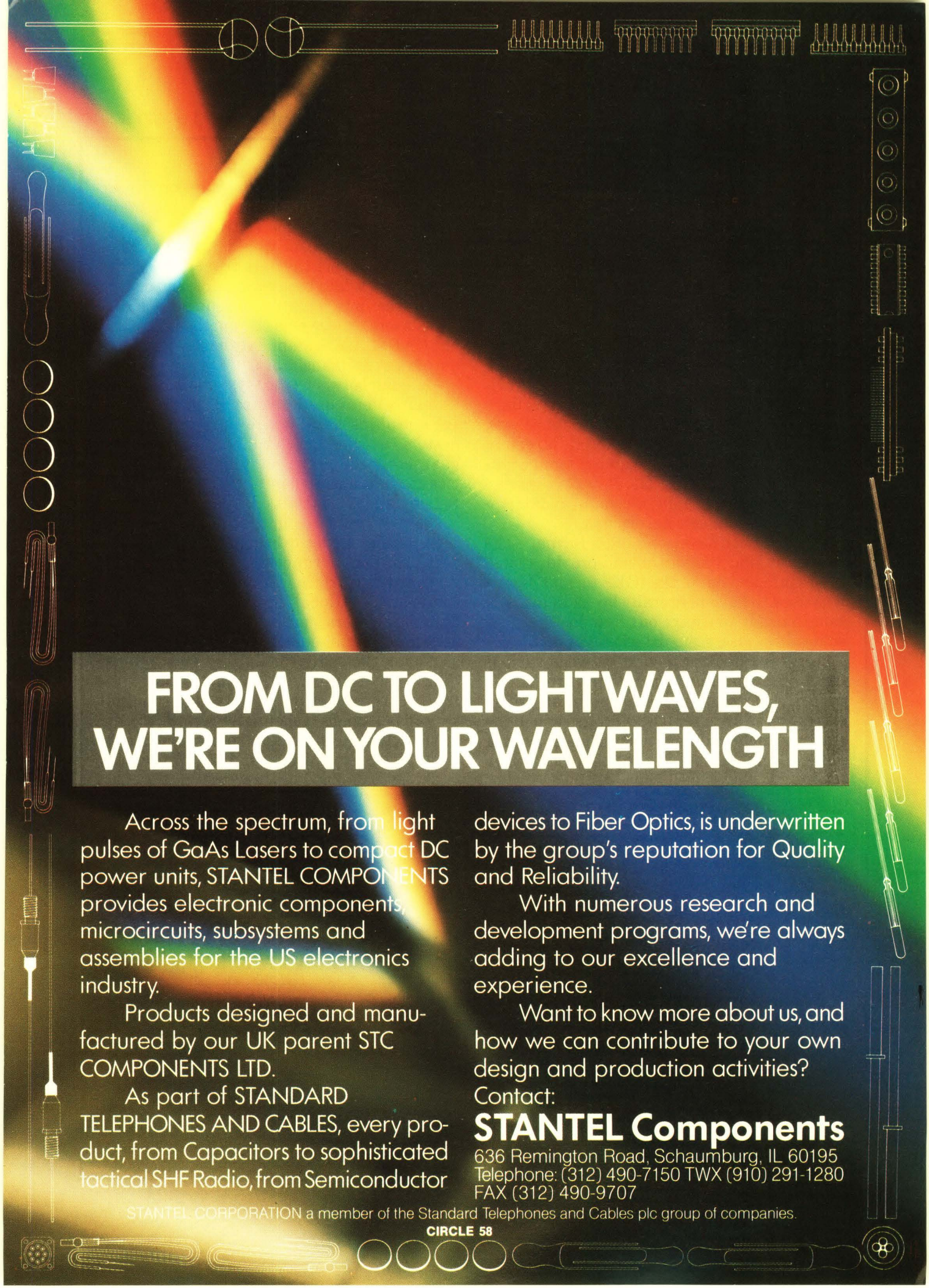
In this particular example, evaluation causes the value of "data" to be assigned to "output" 5 ns later. Because any change in the target signal of one statement may in turn cause the evaluation of other statements, the flow of data through component hardware can be described.

The "signal" idea is an important difference between the VHDL and the way most programming languages handle the concept of time. Expressing time in terms of variables is difficult, but a signal has a history and a future that can be projected. This timing model in VHDL mirrors the timing characteristics of hardware components, and allows a designer to project future values while still referencing current and past ones. So, the timing model allows for a description of synchronous, asynchronous, and mixed designs.

Both TIDAL and VHDL are being viewed as possible hardware language standards, but VHDL has an ace in the hole: as part of the VHSC program it is government-sponsored. In fact, an IEEE Standards Subcommittee (IEEE SCC20 ATPG) charged this fall with developing an HDL language standard, is seriously considering VHDL.

The CAE incompatibility problem is, however, much broader than the design of semicustom ICs. It extends throughout most of industry in general. Different manufacturers have always solved problems in different ways, and products from different CAD manufacturers most often do not communicate with each other, nor can they talk to dissimilar products or numerically-controlled machine tools.

Historically, equipment vendors have been loath to relinquish their own investments in a proprietary product for the sake of standardization and have preferred a custom interface approach, developing special gateways or translators between their equipment and equipment from other manufacturers. There does not seem to be a vendor in the world who doesn't prefer to sell his customers on a "total solution"—made up solely of his products. But no one vendor makes all the computer systems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that most users need.

CAE relies very heavily on computer graphics, one reason why the Initial Graphics Exchange Specification—IGES—has attempted to expand its standards activity to areas like printed circuit boards. IGES began as a solution to the interface problem for CAD equipment using wire-frame figures from assorted manufacturers and is being extended to geometric solids and plane figures.

But even though IGES is mechanically oriented, it is currently the only official standard interface for specifying printed circuit boards. IGES is accepted by the National Bureau of Standards and the American National Standards Institute (ANSI). The July 1982, version 2, of IGES went beyond mechanical descriptions to include electrical designs.

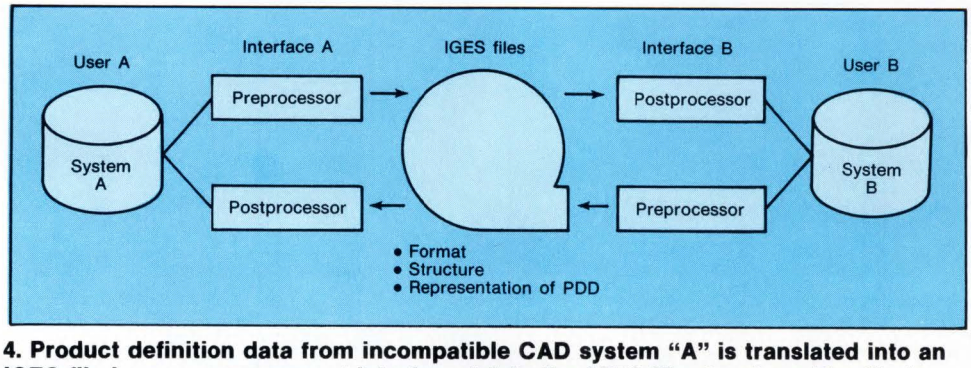
IGES is both a concept and a format—the concept is that vendors should provide translators into and out of the IGES format. Users, who used to have to literally break in to a system in order to figure out how to send data somewhere else, seem to be in favor of it.

IGES is a neutral format between various CAD system vendors. For instance, one CAD/CAM system may represent an arc by choosing the arc's center point, its radius, the starting angle and the finishing angle as data points. Another may take the arc's center point, its diameter, and some point on the arc where a segment starts and another point where a segment stops. To transfer data between systems, a user would have to mathematically convert the data from one form to another via a data base translator, and do it in both directions. This would require $N(N-1)$ translators, where N is the number of different CAD/CAM system databases. IGES requires just 2N translators.

Mapping between CAD systems is difficult. Calma systems use 12-character string labels for graphics data, while Computervision systems use 8-character labels. But while 12 characters cannot be compressed into 8, circles can be translated into circles and lines into lines, and this is the tack taken by IGES.

An IGES file is composed of 80-character records, and all records belong to one of five sections. For instance, the "Start": section gives the file originator a place for general comments; a "Global" section defines general data parameters such as delimiters used, the sending system, destination system, units, and even the scale. The next two sections, "Directory Entry" and "Parameter Data," actually carry the graphics data, and the final section is a single "Terminate" record.

The actual mechanics of cross-translation is done with preprocessors and post processors



4. Product definition data from incompatible CAD system "A" is translated into an IGES file by a preprocessor at interface A into the IGES file structure. The file is translated again for System "B" by another preprocessor at interface B, allowing both CAD devices to work on the same design data.

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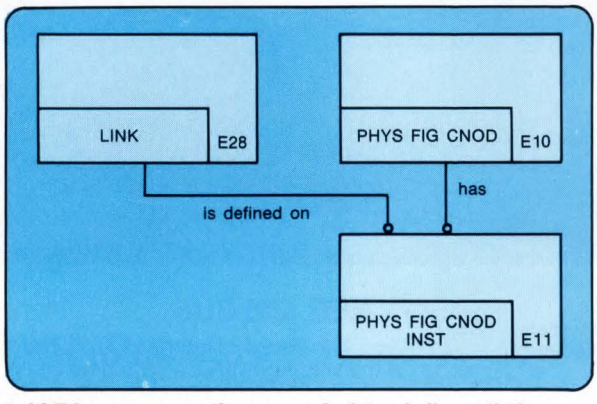
(Fig. 4). A preprocessor is a software module that takes in information structured in one specific format and translates it into an IGES communications file. The post-processor takes information structured in the communications-file format and translates it into the correct format for some other manufacturer's equipment. The idea not only takes the burden of translation off the user, but gives him a file that can be stored on magnetic tape or disc for future use and transmission.

With IGES, graphics elements can be separated into three categories: structure (with annotation), associativity, and property. Some examples of associativity might be "signal," or "view list," and examples of properties might be "part number" or "pin number." Elements like "macro" and "subfigure" are harder to typecast, but each element's parameter record can point to any number of associativities or properties. Translating text is not a problem since text is stored as ASCII strings in nearly all systems. But positioning text can be a problem because different vendors locate text in the drawing space in different ways.

IGES was standardized in 1981 and Version 2.1 (to be released this month) will include new geometries and new capabilities for finite element modeling and electrical properties. Right now, it is the only official format for specifying printed circuit boards, schematics, cabling, and ICs (chip and board-to-board interconnections on a chassis) (Fig. 5).



5. IGES was recently expanded to define all the elements of a printed board assembly. In this example a connection point (CNOD) on a physical figure is stored along with any physical connections (LINK) between electrical entities. CNOD can be used to locate pins, pads, or holes in the graphic representation of the figure.

The missing link

But important elements are missing. IGES defines neither an exchange language nor a hardware definition language. And, in fact, a graphics standard may not be the best solution for some CAE applications where specific meanings must be applied to symbols. While IGES lets a user put objects on the screen, an IC designer needs to give meaning to those symbols. Symbols alone mean very little to an integrated circuit layout.

A circuit designer not only needs a way to give semantic meaning to the symbols used, but must also specify electrical data and, for instance, map things like connectivity (Fig. 6). Using IGES, it is not possible to place cells on a rectangular grid and interconnect them . The concepts are there, but the terminology is not. In short, while IGES makes it possible to do systems design, doing it at gate level is another story. Some gates are impossible to express using IGES.

And, some see compatibility problems down the line for IGES, not because the IGES interface will change, but because the CAD systems undergoing translation will. In fact, one ever-present fly in the ointment is the fast pace at which new technology emerges throughout the design automation field.

The Electronic Design Interchange Format (EDIF) technical committee is not an official standards organization by any means. Rather, it is a cooperative venture, with representatives from Tektronix Inc., Daisy Systems Corp, Mentor Graphics Corp., Texas Instruments, National Semiconductor Corp. and Motorola Inc., all with a vested interest in moving data between in-house design systems via a standard interchange format. In its present incarnation—Version 1.0—EDIF provides a method for storing and transmitting design data. It is neither a programming

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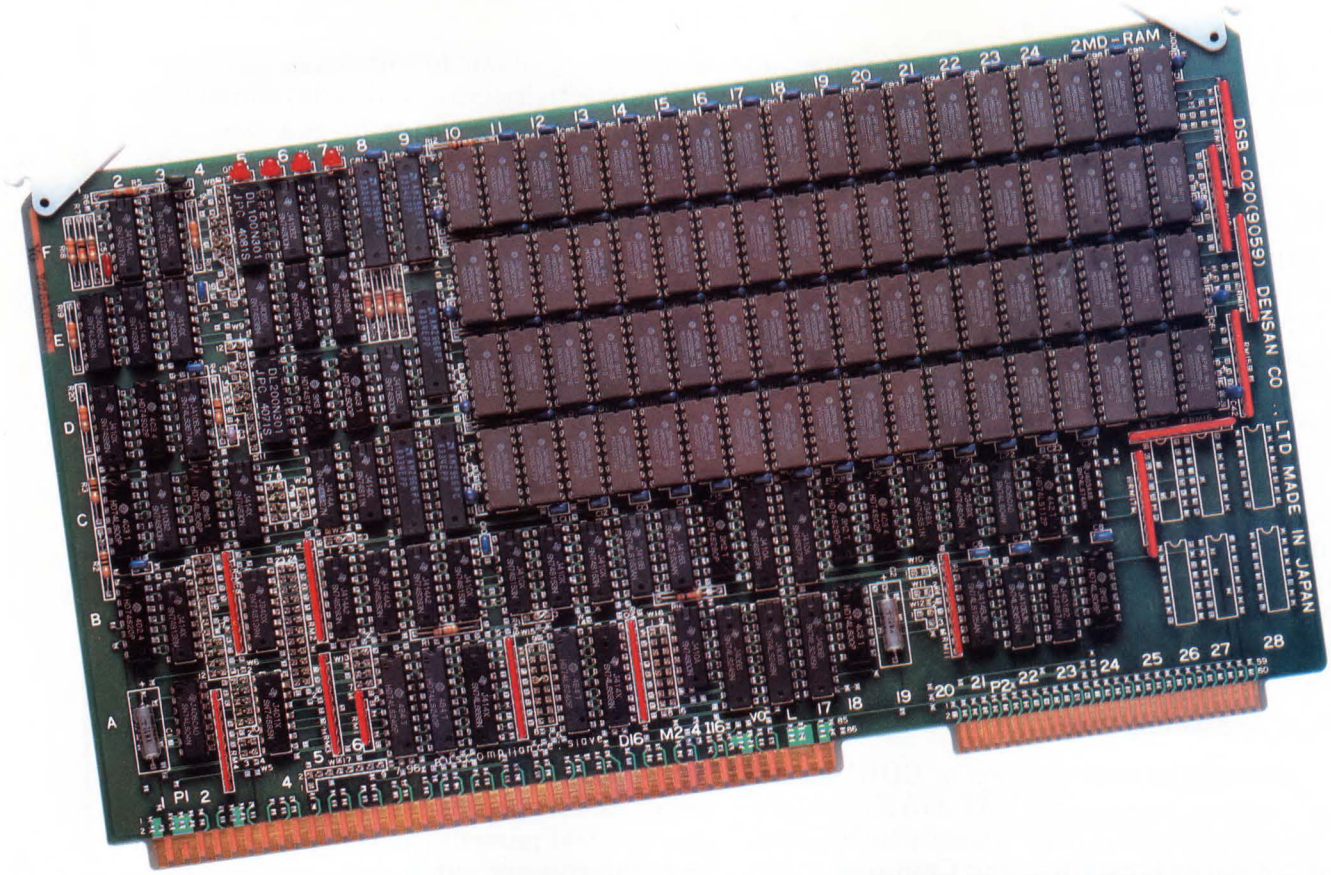

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CIRCLE 60

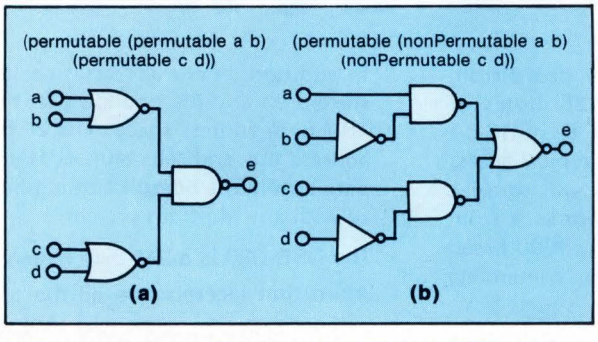
language nor a data-base system *per se*, although the addition of a hardware description language may be on the agenda.

With the workstation marketplace virtually exploding, EDIF's members found themselves dissatisfied with all existing interchange formats and hardware description languages, including some devised by their own companies. The group faulted some formats as too proprietary, and thus too limited, others as too narrow because only specific aspects of design data (like mask artwork or net list information) was addressed.

Another complaint was that evolving formats tend to become too difficult to work with, and too difficult to extend—expecially as new facets are added to IC design. The group was also concerned about developing a standard independent of any particular hardware, design style, or design tool.

Read and writing EDIF

The most current version of EDIF is actually a consolidation of TIDAL, GAIL, Technology Definition File (TDF) devised by Motorola and Mentor Graphics, and Common Interchange Description Format (CDIF) developed at UC Berkeley for transmitting schematic



6. Connectivity—what is connected to what, and whether ports can have their arranged order shifted without affecting logical properties—cannot be communicated completely with IGES. EDIF handles connectivity by specifying links with "permutability" constructs. For example, circuit pairs A, B, and C, D, are designated permutable (not connected) (a) and nonpermutable (b).

diagrams, symbolic layout, mask-level layout and connectivity information. It is intended to be both read and written by machine, but to maintain enough legibility to allow manipulation by human programmers. But, to be human-readible, EDIF would have to be formatted out of a program, and into a non-LISP structure.

It's syntax is similar to that of LISP, in that data are represented as symbolic expressions. EDIF's "atoms" are data primitives, such as strings, signals, ports, figureGroups (for representing mask layers or colors in an illustration), numbers and identifiers.

More complex structures are built by forming parenthesized lists whose elements are data primitives, or other lists. But in every case, the first element of a list is a keyword, reserved by the format definition to provide meaning for subsequent elements by their positions in the list. The idea here is that, since the semantic weight is borne by keywords and not by the syntax, new keywords can be added as demands change without changing existing parsers. Old parsers can continue to extract their information, while new ones can use the new information in any extended format.

One interesting footnote to EDIF is that its files need not be complete to be used. A file can contain partial descriptions of designs that express some details and intentionally omit others, allowing, for instance, a silicon foundry to send a file of several base arrays, or a library of macro cells.

In terms of overall structure, EDIF is expressed in the form of a hierarchy that is abstract at higher levels, and becomes progressively more detailed as it descends the hierarchy. At the highest level, an EDIF file contains a single logic file which may contain several designs and several libraries of cell definitions. Each library is a collection of relevant design information including a group of cells with common characteristics. For instance, a file might contain separate cell libraries for different technologies.

Much like TIDAL, EDIF has design blocks that provide an entry point for the user by indicating which cell in which library contains the top-level description of a design. A sample

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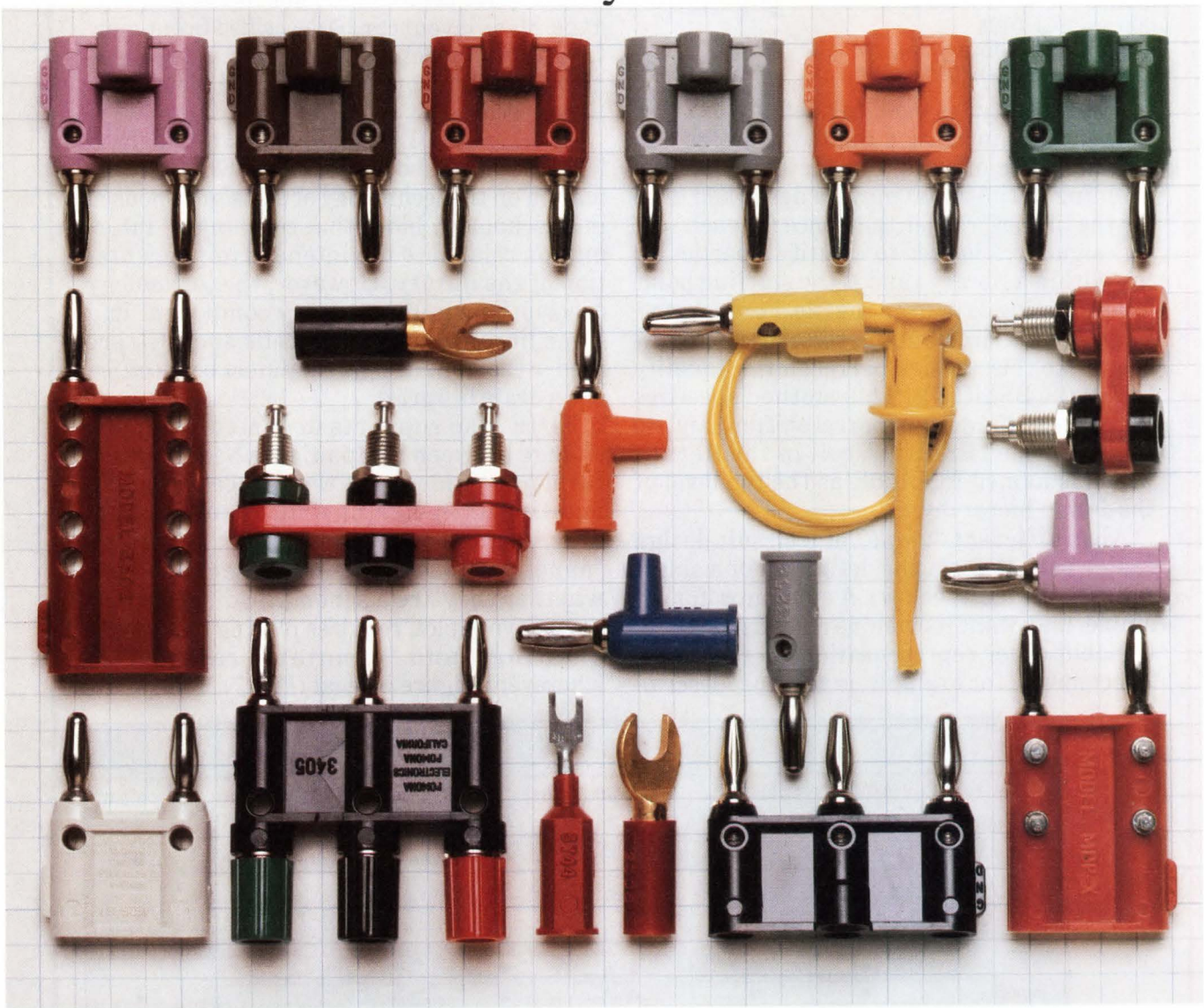

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CIRCLE 61

EDIF file might look like this:

```
(status . . . )
(library ECL100k . . . )
(library nMOSlibrary)
(design Barrel shifter . . . )
```

A cell library is used for definitions and technology information related to design and manufacture of cells. Characteristics (like gridding definitions) may be described once for the library, rather than once for each cell. A design block is used to identify a particular cell within a library , and is the starting point for extracting data from the file. For instance, a design for a circuit might refer to the ECL library like this: (design barrel shifter (qualify ECL100K BShiftE)). This method specifies the name of the design (barrel shifter), and its root cell, the "BShiftE" cell in the library which is named ECL100K as the top level of the design hierarchy.

Also, different "views" of a circuit design can be used to form the definition of a single cell (see the table, below). A simulator, for example, may want its view as a net list description, but other representations are possible. "Document," for example, is a textual description of a design, while "stranger" is a catchall category for cells that do not fit the standard type. Mask layout can be described in one view, behavioral modeling in another, and schematic representation in still a third view of the same circuit.

As with VHDL, both physical and behavioral views can be expressed in EDIF. Information on the technology of a design is housed in a technology block that contains all information related to the intended implementation of the library. However, the technology description applies to every component in a given library, so if CMOS cells and ECL are used in the same design, they must be specified in separate libraries.

EDIF also supports documentation exchange between companies, whether in the form of comments in test procedures, annotating drawings, or writing full, textual descriptions of design elements with an "annotate" construct. Annotating drawings, whether they are a schematic diagram or a mask layout plot, requires placing text within drawings, and "annotate" can be used wherever a figure is legal (Fig. 7). Two points

Legal contents in EDIF viewtypes

View type	Net list	Schematic	Symbolic	Mask layout	Behavior	Document	Stranger
annotate		●	●				●
criticalSignal	●	●	●				●
declare	●	●	●	●	●		●
figureGroup				●			●
global	●	●	●	●			●
instance	●	●	●	●			●
joined	●	●	●	●			●
logicModel					●		●
measured	●	●	●				●
mustJoin	●	●	●	●			●
rename	●	●	●	●	●		●
required	●	●	●				●
section						●	●
unused	●	●	●	●			●
userData	●	●	●	●	●	●	●
wire		●	●				●

SURELY IT WILL COME TO PASS...
THOU SHALT HAVE NO OTHER O.S. BEFORE S1
THOU SHALT NOT TAKE THE NAME S1 IN VAIN
THOU SHALT NOT grep
THOU SHALT NOT sag
NEITHER SHALT THOU ratfor
THOU SHALT NOT MAKE THEE ANY uux
NEITHER SHALT THOU scat
THOU SHALT NOT DESIRE xargs
THOU SHALT NOT BEAR FALSE yacc
THOU SHALT NOT COMMIT shmop
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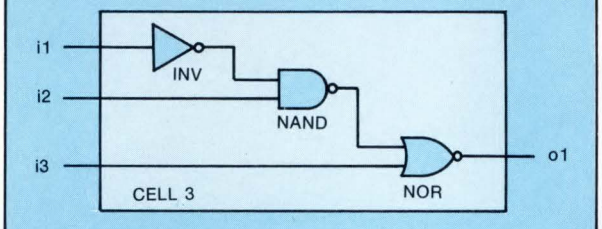
are required following the character string, to describe a containing figure. Another construct—"justify"—is used to locate the text within the containing figure. It is left to the interpreting device to give shape to the characters.

EDIF's interchange format for transferring data in final form, is expressed in simple, geometric primitives. To keep things simple, yet still have procedural descriptions for those who need them, EDIF descriptions are specified on three different levels depending on the amount of complexity required. The most basic is Level 0, where only constant values are allowed. The second stage, Level 1, includes Level 0 with the addition of variables and expressions. Similarly, Level 2 includes Level 1 with the addition of procedures and more complex data types. On one hand, this offers some additional flexibility, with each level a subset of the higher one, it is possible to move down to a lower level by replacing parametric values with constant values. But in doing so, errors and ambiguities could creep in.




```
(cell cell3
  (view Schematic cell3_Schematic
    (interface
      (body
        (figureGroup SCHEMATIC_SYMBOL
          (rectangle (point 1750  1300) (point 5600 3100))
          (annotate "CELL3" (point 4800 1800) (point 5400
            2000) UPPERLEFT)
          (path (point 1600 2800) (point 1900 2800))
          (annotate "I1" (point 1600 2850) (point 1700 2950)
            LOWERRIGHT)
          (path (point 1600 2200) (point 1900 2200))
          (annotate "I2" (point 1600 2250) (point 1700 2350)
            LOWERRIGHT)
          (path (point 1600 1600) (point 1900 1600))
          (annotate "I3" (point 1600 1650) (point 1700 1750)
            LOWERRIGHT)
          (path (point 5450 1900) (point 5750 1900))
          (annotate "O1" (point 5650 1950) (point 5750 2050)
            LOWERLEFT)
          (annotate "INV" (point 2200 2850) (point 2400 2950)
            LOWERLEFT)
          (annotate "NAND" (point 2400 2200) (point 2800
            2300) UPPERLEFT)
          (annotate "NOR" (point 4900 1900) (point 5100 2000)
            UPPERLEFT)
))))
```

7. The "annotate" construct in EDIF can be used wherever a figure is legal. Another construct, "justify," is used to place text in the rectangle. Here, a schematic view of a cell has been created using the "annotate" construct.

EDIF seems to contain almost all of the essentials needed for storing and transmitting IC data between designer and foundry—connectivity description, simulation, mask layout information for checking and building, and test data for testing and debugging. However, it lacks a means of expressing logic design rules as fully as they need to be. For instance, a standard cell designer might want to indicate that two cells cannot be driven with any one cell, but there is no way to express it now. Also, testability rules need expanding, but this is on the agenda.

EDIF may eventually be adopted by a standards body. Its members have been approached by the Electronic Industries Association's Joint Electronics Design Engineering Council (JEDEC). JEDEC has been working at developing standards for digital gate arrays. Last year, JEDEC's JC44 subcommittee defined terms and definitions for gate arrays, and voltage standards for semicustom ICs. The group has also defined a gate-array performance benchmark consisting of MSI-level macros.

Currently, JC44 has split off into two groups, one for gate arrays and the second for standard cells. They have completed much of the work of generating a macro set and are looking at interface standards for transferring test vectors from one CAD system to another.

Some overlap among these standards-makers is not a bad thing. It means that all bases will probably be covered—eventually. On the other hand, if the various groups fail to coordinate their activities, some groups may find they have wasted a lot of valuable time duplicating work that is already being done.□

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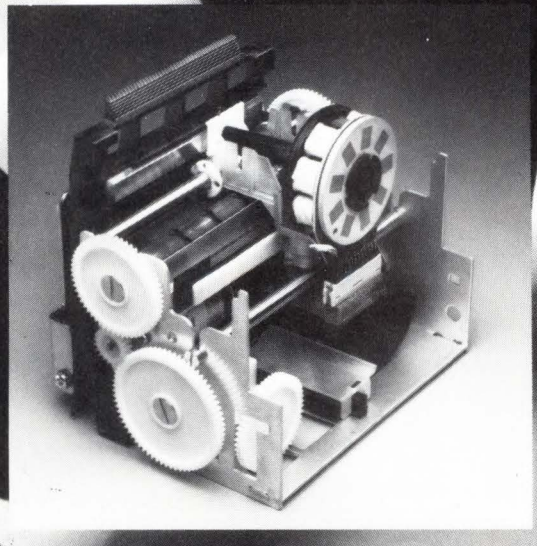

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CIRCLE 63

Software Standards

Designer's Reference

Although the four main schools of Unix remain apart, standardization within them has begun

Standardization for Unix is now under way, eliminating the last major obstacle to further proliferation of the increasingly popular operating system. In one form or another, Unix is now available on most minis, supermicros, and 16-bit microcomputers. In fact, it is the most widely used operating system available today, despite the fact that a lack of standardized definitions and functions has hampered the development of application software that can run on all Unix-based computers (see "What is Unix?," p. 121).

Standardizing Unix sounds simple: Build a set of definitions for the various implementations of Unix that enables application programs to be moved easily from one host system to another, regardless of the details of the system's hardware or software base. In other words, specify the application interface to the Unix system independently of how the hardware and software below it are implemented. Furthermore, see to it that a minimum of processing is necessary to adapt a software package from one Unix system to another; only a recompilation of the package should be needed. Simple as this sounds, it is made difficult by the large number of Unix and Unix-like operating systems available today.

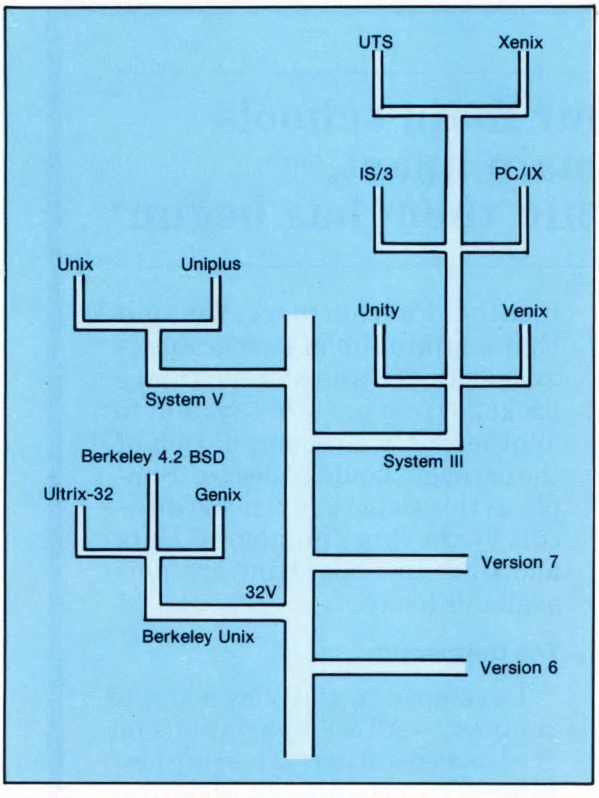
Ray Weiss

The Unix world

Developed initially by a single company—AT&T—variations on the Unix operating system are now offered by a number of organizations. At present, there are four main groups of Unix systems. Not only is there no standardization between any two of these groups, there is also none within any of them. The good news is that this is changing: the majority of these groups are moving toward some form of internal uniformity of implementation. The bad news is that the groups show no sign of combining into one overall standard, although they are sharing or interchanging technology.

The four major groups are:

AT&T (System III and System V), Berkeley Unix, Microsoft Unix (Xenix), and pre-System V (Fig. 1). The first group consists of AT&T and the licensed implementations that are committed to a common standardization path. The second group, the Berkeley Unix set, is made up of those implementations whose starting point is the Unix implementation developed at the University of California at Berkeley under funding by the Advanced Research Projects Agency (ARPA).



1. As the Unix family tree indicates, there are three main Unix braches: Berkeley Unix, which began with Unix 32V; mainstream Unix, which is based on System V; and Xenix, which branches off System III. A fourth group of Unix lookalikes (not shown) includes implementations based on earlier versions.

The third group is a single implementation—the Microsoft Xenix system. Today, Xenix accounts for about half of the AT&T-licensed systems in the marketplace. The last group encompasses the remaining implementations, some of which are licensed from earlier versions of Unix, some of which are combinations of other operating systems and Unix, and others that are unlicensed versions of Unix that were designed from the ground up.

An early success at standardization

The first steps toward standardization have already been taken. The /usr/group, an independent trade association for the Unix community, has developed a vendor-independent standard for Unix systems based on the System III release. The standard, assembled by a special committee on standardization, has been accepted on a mail vote by the over 1400 /usr/group members. The committee is made up of individuals from most of the major organizations involved in the development of Unix systems. While the committee members do not officially represent their parent organizations, the fact that they reached an agreement on such a standard portends a new era of cooperation and standarization.

The/usr/group effort represents the coming together of the first Unix grouping—the Unix systems that are System III- and V-specific, and are moving in the direction of AT&T's System V evolution. In the spirit of concession, the new standard is based on System III, with provisions for the earlier Version 7 release, and is aimed at moving towards System V. By adopting this approach, the committee has provided a path to System V compatibility for many of the Unix systems based on these earlier systems.

The /usr/group standard attempts to provide application portability by defining standards for the Unix system calls and the C language library functions. An application program interfaces with the user (usually through system utilities), the C program library, and the Unix system kernel. The set of Unix utilities is also used by an application

What is Unix?

Unix is more than an operating system. It is actually an operating or programming environment. It combines the basics of an operating system with an interface that is particularly easy for programmers to use. Developed in the late 1960s and early 1970s, Unix carries some of the flavor of languages that were developing at the same time—languages like Lisp and Forth. Like them, Unix is highly interactive, giving the user an easily modified unstructured environment that can be tailored to meet individual requirement. But, as with those languages, easy tailoring can lead to unique problems.

A number of landmark features in Unix are still being gradually accepted. A major concept was that instead of building one large program with a main control routine and a number of subprograms, a number of smaller routines and utilities can be assembled to handle the job. Features like program redirection, pipes, forks, filters, and a set of general utilities that could easily be added to, made this approach viable.

Another feature that makes Unix so attractive to programmers is the way I/O is handled—all I/O is similar, just a string of bytes with a simple set of commands. All detailed I/O processing is handled by the operating system, eliminating the need for programmers to learn complex I/O sequences and record blocking. Also files are easily defined and found within a simple hierarchical file system with multiple-level directories. A shell or interface language allows the user to program the operating system and resources directly or indirectly via files or programs. The shell can be tailored to meet individual user needs.

A model system

Unix was one of the first programming systems to provide a comprehensive set of programming tools to build, debug, and maintain programs. Some of these tools, such as SCCS (source code control system), Make (version builder), and Lint (source code analysis checker) serve as models for current software engineering tools.

Unix consists of the kernel—the basic operating system—the shell containing the basic programming system, and a large number of utilities, including languages and other programs.

The C language was developed for Unix, and the system is programmed in it. C is a language midway between assembly language and the higher level languages. It is sufficiently high level to provide structured programming constructs and symbolic addressing, but low level enough to allow bit manipulation and pointer manipulation. C is a very simple and sparse language that is fairly easy to learn. Most C compilers are built from the standard AT&T portable C compiler.

An application that interfaces through the high-level Unix system calls should have no problem in portability beyond the need for recompiling for each new host. However, if the application takes advantage of the host hardware architecture or interfaces directly with hardware or accesses kernel functions then it will have to be modified to run on a different system. Even so, the transporting of application programs among Unix systems is orders of magnitude easier than moving programs among dissimilar operating systems and computers.

The Unix set of operating systems is not yet stable enough to allow applications to be transported between systems without experienced programmer help. For one thing, each Unix system can be different in that the system is tailored differently and may have a different set of utilities.

Good, but not perfect

Unix is not the ideal solution to all operating systems needs. To paraphrase Winston Churchill: Unix is not that good an operating system, until you compare it with all the others. A number of problems revolve around the Unix file system. While easy for the programmer to use, it cannot support heavy file usage because of the mechanism used for file allocation: It lacks adequate journalization and recovery features and it lacks a sophisticated record organization. Files in Unix are just strings of bytes, and the system cannot index files. Unix, with the exception of Berkeley Unix, is not designed for real-time processing and lacks virtual memory capability. Also, the communications features are not a sophisticated as they should be.

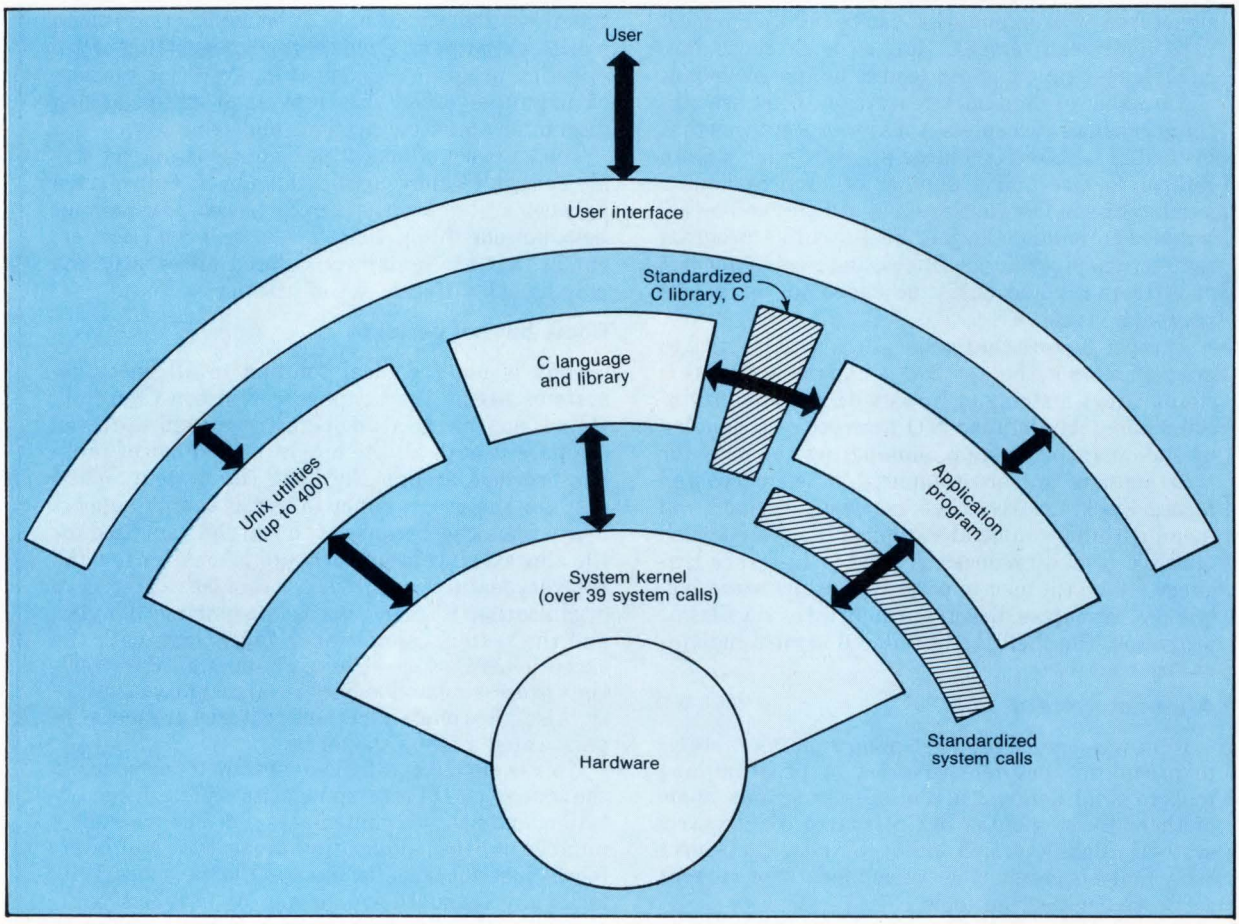
Unix is also a very difficult system to learn due to the conciseness of its language, its cryptic documentation, and poor user interfaces. For business and a number of other application areas, the shell interface is just not friendly enough. Furthermore, Unix lacks any standard windowing or graphics packages. Another problem arises from the ease of adapting Unix to individual needs—it is difficult to control the system when so many different variations can be created. Programmers become accustomed to their own utility set, making common utility bases difficult to maintain.

Furthermore, Unix is a very large system: it can contain over 400 utilities and its source code can run to over 10 Mbytes on hard disks. Maintenance and system programming can therefore be quite a chore in many cases.

program via system calls. Thus, if the interfaces to an application are given standard definitions and if all accessible functions have common definitions, then application programs can be easily moved among different Unix systems.

Thirty-nine system calls for the system kernel are defined for the interface between an application program and the kernel (Fig. 2). Given Unix systems based on those definitions, applications would still have to be recompiled to the new system, but further modification would be minimal. The utilities and user interface are not defined in this standard.

One of the major flaws of Unix—the absence of a file- or record-locking feature—has been corrected under the /usr/group standard. Here a system call is defined for record-level locking, which will eliminate the problems of concurrent access to a record by



2. Fixing the system calls to the kernel and the C language library is the first step toward applications portability. Applications interface with the kernel only through system calls. The /usr/group standards define the system calls and the C language library routines.

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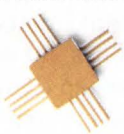

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different processes. The Lockf function will lock the area for the exclusive use of the requesting process; if the area is already locked, the process will "sleep" until the area becomes available. If locking the area causes a deadlock between requesting Lockf processes, the area will not be locked, and an error message will be returned to the requesting processes.

The /usr/group approach to file locking has been adapted by AT&T Technologies Inc. for later release. A subroutine function is being added to that release to emulate the standards approach to file locking. But, System V will be upgraded to furnish this feature—an indication of the acceptance and the need for standardization by the Unix community.

Furthermore, an IEEE committee, the working group on Unix Operating System Standards, has been formed to develop Unix standards. This committee will use the /usr/group standards as a base document. The committee will be examining application portability, user interfacing, media compatibility, and communications standardization issues. Also, an ANSI committee has been formed to develop standards for the C language. All in all, standardization seems to be the next step for Unix.

AT&T moves toward standardization

Meanwhile, AT&T Technologies is also taking significant steps toward the standardization of Unix. First, it is working closely with the standards committees and is willing to use developments from that standardization effort in its product—Unix System V. Second, it wants System V to be accepted as an industry-wide standard for Unix operating systems. And finally, it wants to standardize Unix itself so it can be a stable base for both software and hardware. It has already promised to continue to sell or license Unix, as well as to keep it an open system that vendors and developers can rely on as an operating systems base.

Specifically, AT&T is going to define the System V interfaces to create a standard with which applications programs can mesh. While Unix System V is provided by AT&T and its licensees, the System V interfaces will be defined for all systems, licensed or not.

These interfaces will be specified by a document, "The System V Interface Definition," which is now in limited distribution and will be available for general distribution in January 1985. This document defines the minimum set of system calls and library routines common to all operating systems meeting the System V standard. The remaining commands and utilities are ordered into a set of optional extensions to the basic system. The definitions specify the software interfaces and the run-time behavior (not the implementations) of the function or utility. They follow in the footsteps of the /usr/group standards for the earlier System III version.

By this method, the System V command and utilities are unbundled into sets or logical extensions that can be added as needed to the basic system. This enables System V to be used in systems that cannot accommodate all 250 system calls and utilities. The following extensions will be defined: kernel, basic utilities, software development, network services, large machine administration, graphics, basic text processing, user interface, and data base.

To ensure standardization on the microcomputer level, AT&T has made arrangements with some of the manufacturers of the major microcomputer chip sets to develop derivatives of System V for their systems. These manufacturers include Motorola (for the MC68000), Intel (for the 80386), National Semiconductor (for the 32016), and Zilog (for the Z80000). The Motorola version has been completed (ELECTRONIC DESIGN, April 19, p. 268), and the National version will be released early next year.

A test is coming

To test for conformance to the System V interface definitions, a validation suite for system licensees will be made available in 1985. This set of programs will validate any proposed System V-compatible operating system to ensure conformity to the interface definitions.

The Berkeley Unix community—the University of California at Berkeley, Digital Equipment, Sun Computers, Masscomp, and

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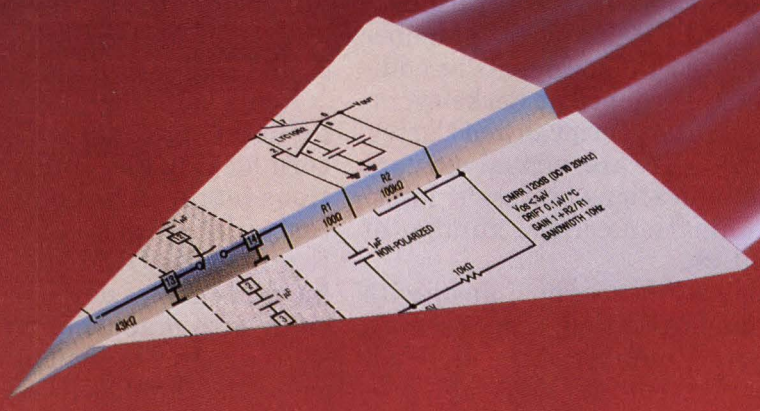

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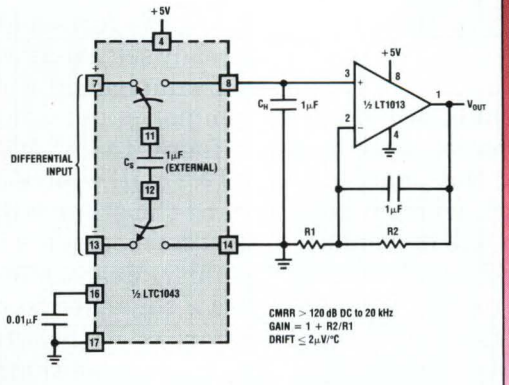

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others—are now holding talks to coordinate new developments and set up standards for the existing Berkeley design as well as forthcoming enhancements. These organizations do not follow the System V standards, preferring to direct the Unix operating system toward the larger research and development problems, rather than toward a more rigid, unbundled system.

Berkeley beginnings

Berkeley Unix, typically called BSD 4.x, was developed from Unix 32V by the University of California at Berkeley for the DEC VAX. Subsequently, it was enhanced under government funding for various ARPA projects. A number of the more advanced enhancements or additions to Unix were developed at Berkeley, including Vi, a text editor; Termcap and Curses, terminal interface software; virtual memory processing communications protocols; interprocess communications; and a number of operational utilities.

Though Berkeley Unix does not join up with System V for standardization, it does serve a valuable function. A number of the more advanced utilities, system functions, and programs have come to Unix from the Berkeley research community. It acts as the point man for future Unix developments. Developments from Berkeley Unix, especially in communications and distributed processing, will continue to add to the mainstream Unix systems.

Toward compatibility

One interesting development is the appearance of systems that are compatible with both System V and Berkeley Unix. National Semiconductor currently has Genix, which is compatible with BSD 4.1 and soon will be compatible with 4.2, and will have a System V version early in 1985. Both will run on the National 32000 series of microcomputers and will share a number of functions and resources. The Pyramid Technology OSX operating system allows the user to select which of the two Unix operating systems to use for execution; it uses the Berkeley variation for its internal system.

Microsoft Xenix is based on Unix Version 7 and System III. It has been recently upgraded to some of the System V features, but there are no plans to bring it into conformity with System V. Xenix will, for the time being, go its own way. Its goal is to bring Unix to the higher level of personal computers. It should be noted that over half of the existing licensed Unix systems are Xenix.

Playing with the PC/AT

In pursuit of its goal, Xenix is currently being optimized for the Intel 286 microcomputer and will be supplied by IBM for the new 286-based PC/AT. Xenix has already been unbundled—that is, subset to fit onto the smaller microcomputers; its kernel occupies 100 kbytes of memory, and it requires from 3.0 to 7.5 Mbytes of hard disk space.

Xenix is farther down the path than Unix for its intended market. It already provides record locking and interprocess communications features, but only the first feature is compatible with system V. Microcosoft plans to provide an OEM kit—a binary adaptation kit that enables developers to adapt Xenix to their own machines without the need for source code. This can be done for the 286 because the chip has its own memory management unit; thus the system does not have to be adapted to differing memory management schemes.

Future trends

For the foreseeable future, the trends are already set; a majority of the System III and V Unix implementations will draw together in a common standardization effort that will tend to follow the AT&T System V evolution. But, AT&T will evolve System V with an eye toward the standards groups and toward any new developments in the Berkeley Unix community. Meanwhile, the latter community will draw together to standardize its systems, whereas Microsoft will continue along its path, and the remaining Unix or Unix-like systems will either migrate towards System V or develop niche markets (Fig. 3).

Standardization efforts will also proceed on the C language—a standard of C will greatly aid the portability of system software as well as applications. The standard will be based on

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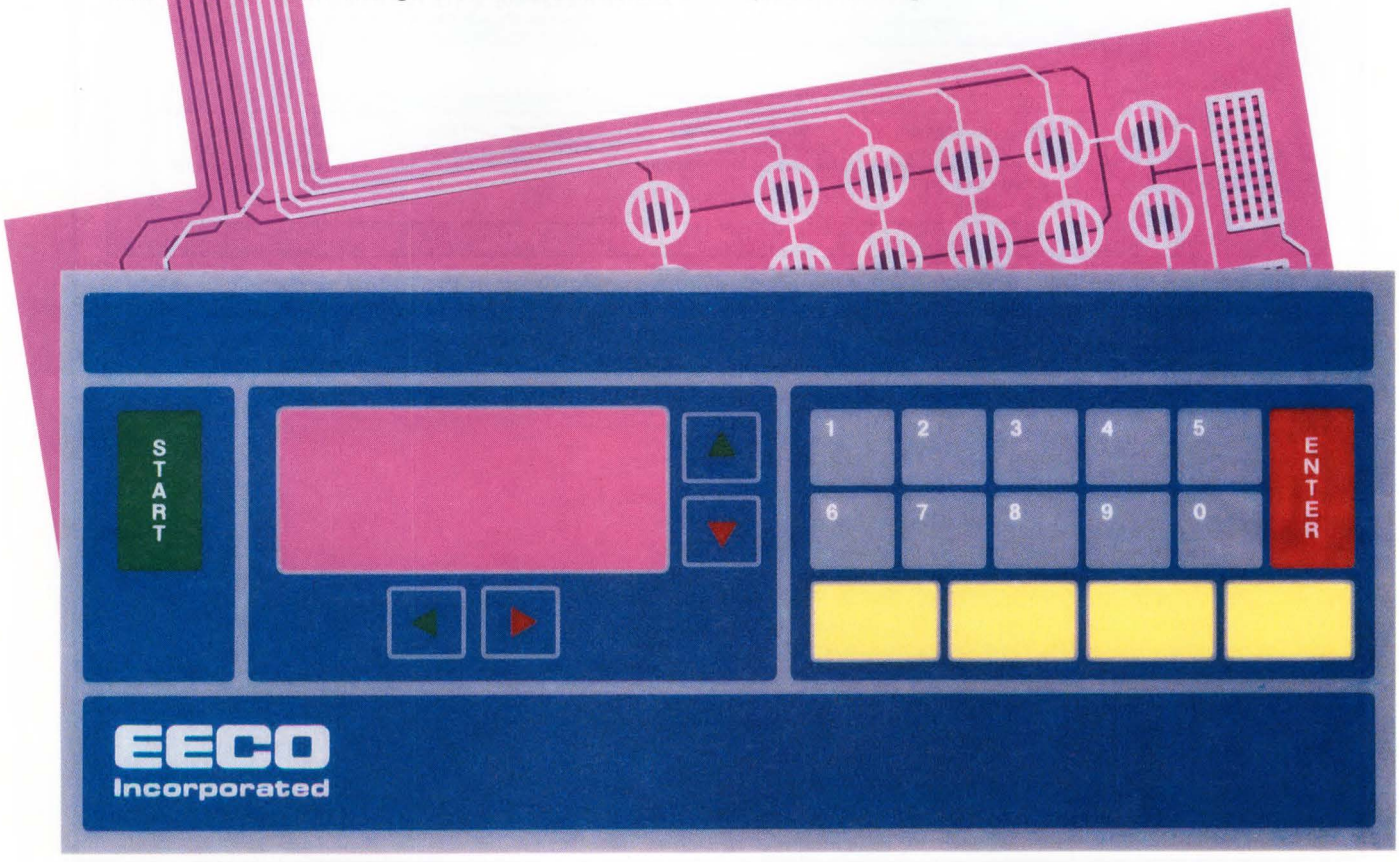
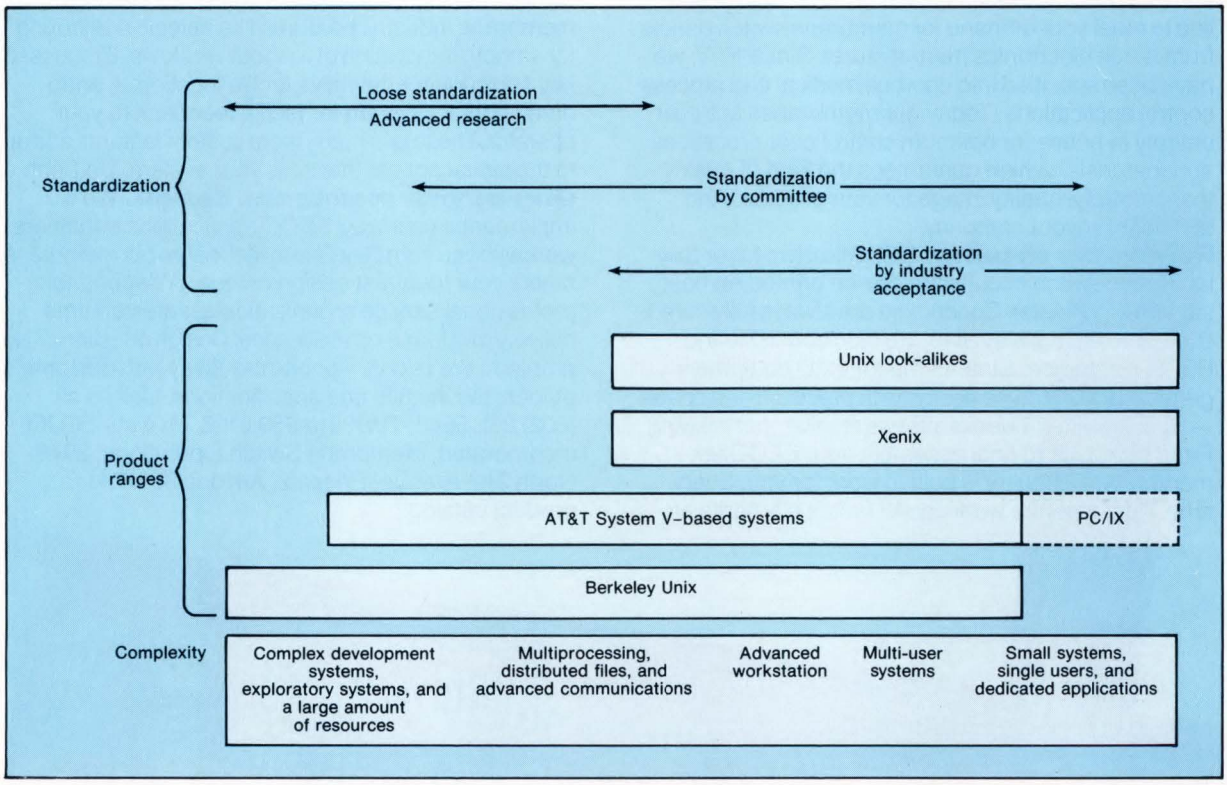


the Portable C Compiler from AT&T.

Standardization of Unix will create a stable base that can be supported through expert systems. One research system currently in development is the Unix Consultant. The goal of the program is to provide the new user with a natural language "help" facility that will enable the user to learn and use the Unix system. When in doubt as to how to do something, the user can simply ask the system for guidance. The program, developed at Berkeley under government grant, is partially operational now. Its speed and range will grow as research continues into the underlying technologies.□



3. The low end of the Unix operating systems arena will be standardized in the future by decisions made in the marketplace. The middle ground will be standardized by industry and organized committees. The upper end will permit advanced research through a loose, but cooperative, approach to standardization.

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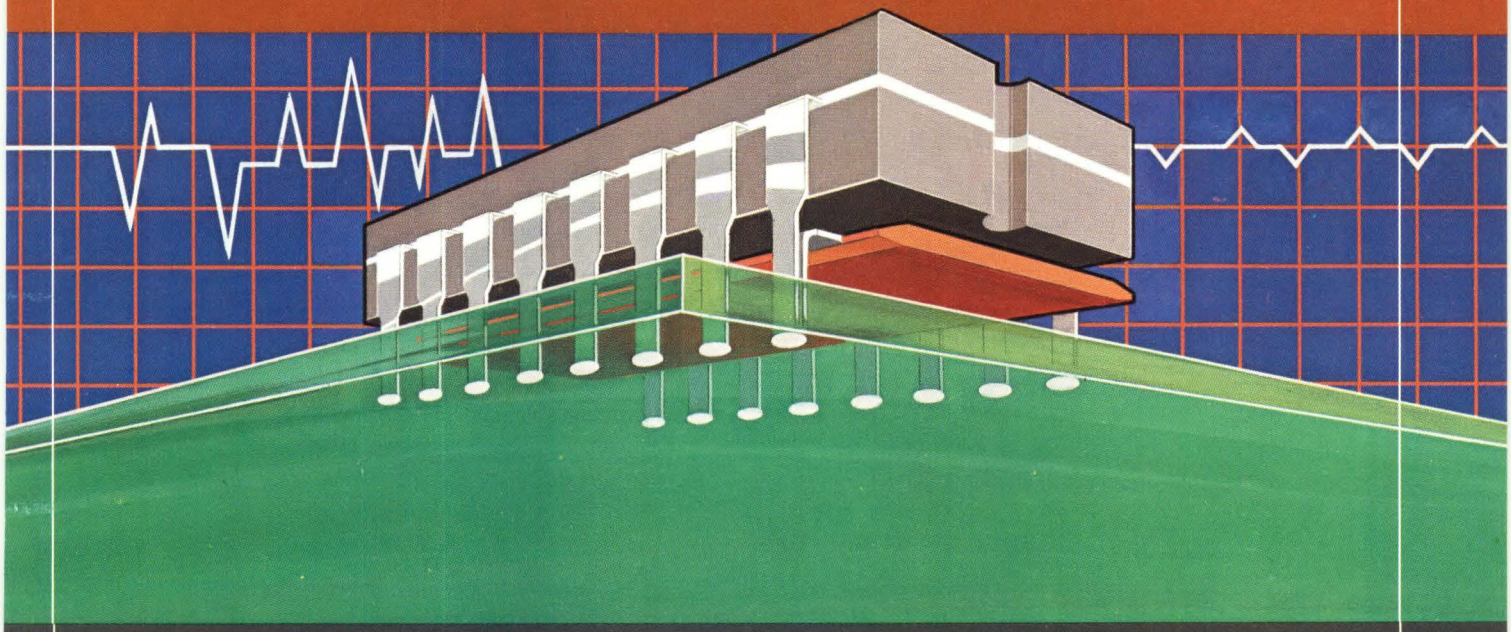

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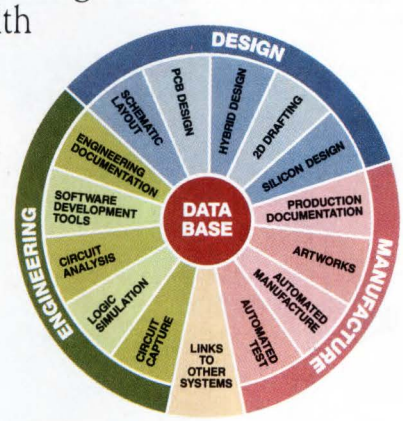

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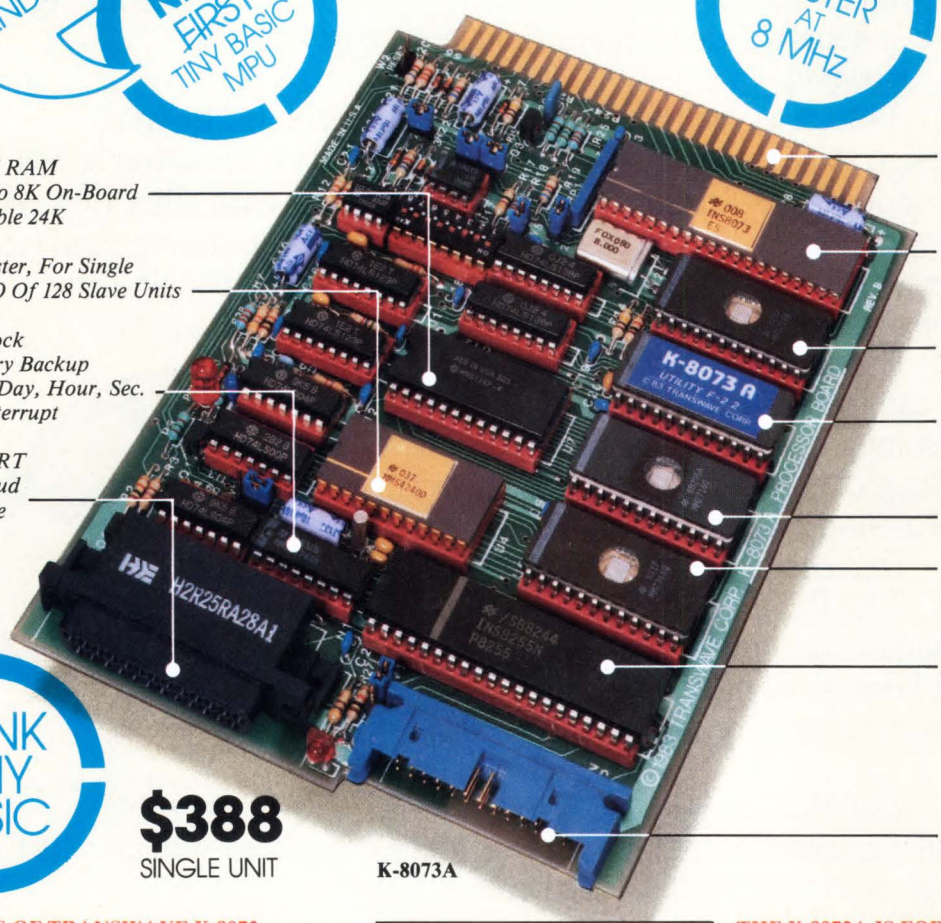

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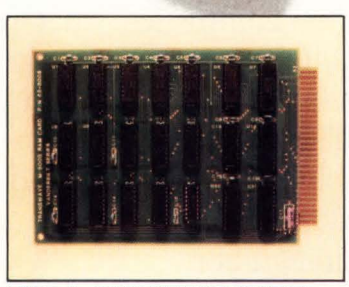

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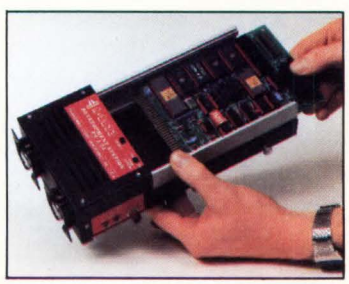

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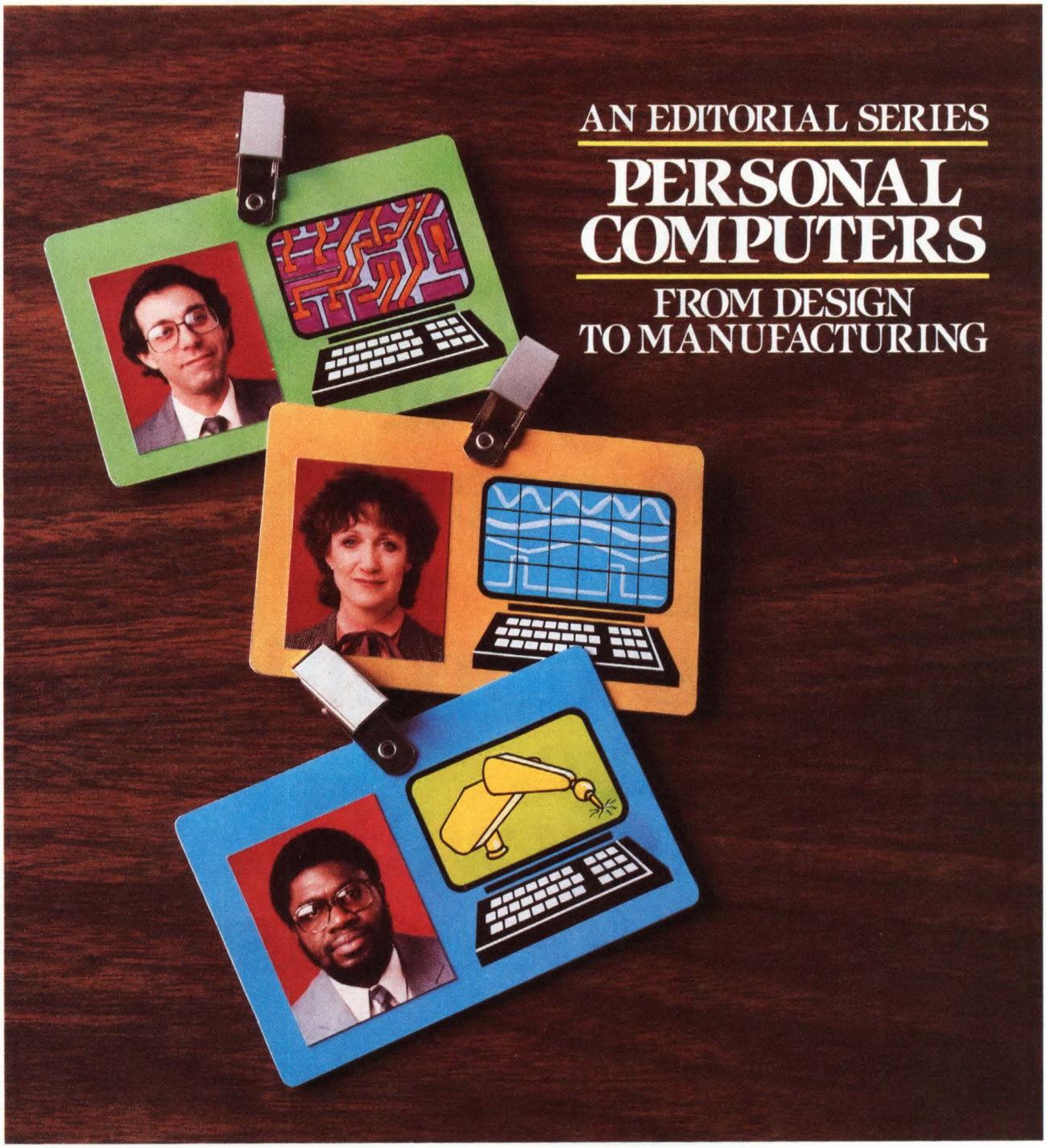


As personal computers become more powerful–and more commonplace–user demands grow. With engineers perceiving greater shortcomings all the time, technology will have to rise to the occasion.

Jesse Shereff

Clearly, personal computers are solidly entrenched in the workplace. Today's engineer or manager has to function as comfortably with a computer as he does with a telephone or pencil. This trend will surely continue, and in a few years we should find that virtually everyone will be using computers in the workplace, with the workstation becoming an even greater aid on the job.

Most readers who responded to ELECTRONIC DESIGN's survey about their personal computer-based workstations are happy with their setups and claim their machines are completely adequate for their current needs. However, only slightly fewer than half feel that their present systems will be sufficient over the next three to five years. As a group, they look forward to a wide variety of improvements in personal computers in the foreseeable future.

The area in personal computer technology rated highest in importance, in terms of needing improvement, by readers of ELECTRONIC DESIGN is ease of use. Though "bigger and better"—speed, memory, mass storage, graphics, and so forth—is usually the battle cry of users everywhere, the desire to avoid complicated command structures is the major concern.

The first half of the survey (ELECTRONIC DESIGN, Nov. 29, p. 161) showed that 90% of respondents use personal computers or similar equipment on their jobs, and another 7% plan to obtain such systems soon. The majority of users employ 16- or 8-bit systems, with the scales tipped heavily in favor of the IBM PC personal computer and its lookalikes. Only 4% work on the more powerful, graphics-ori-

Figure 1

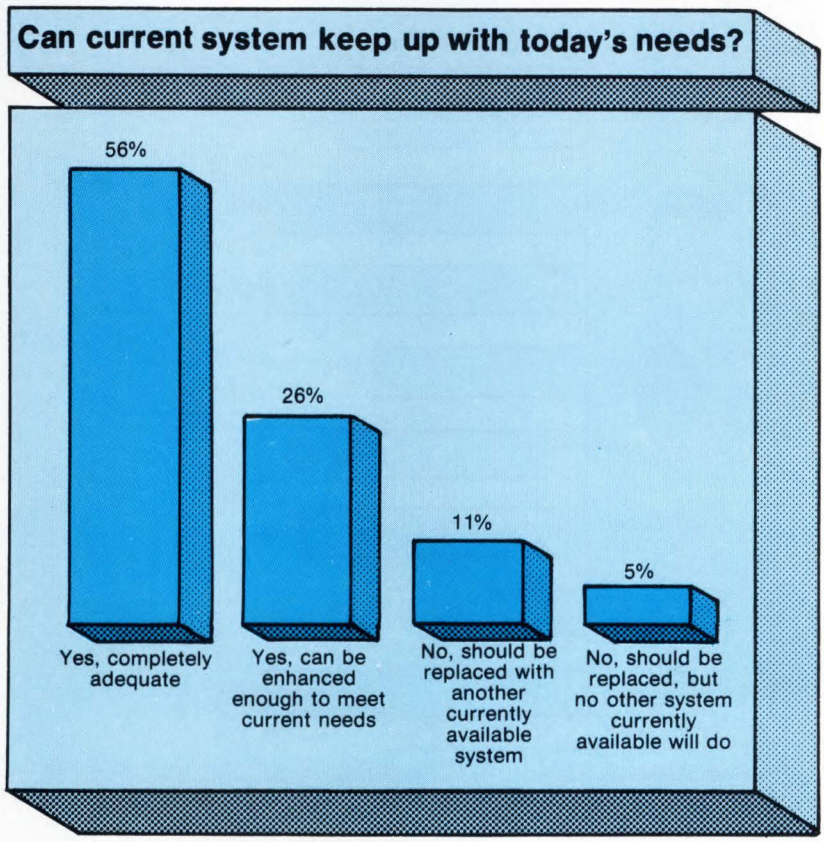
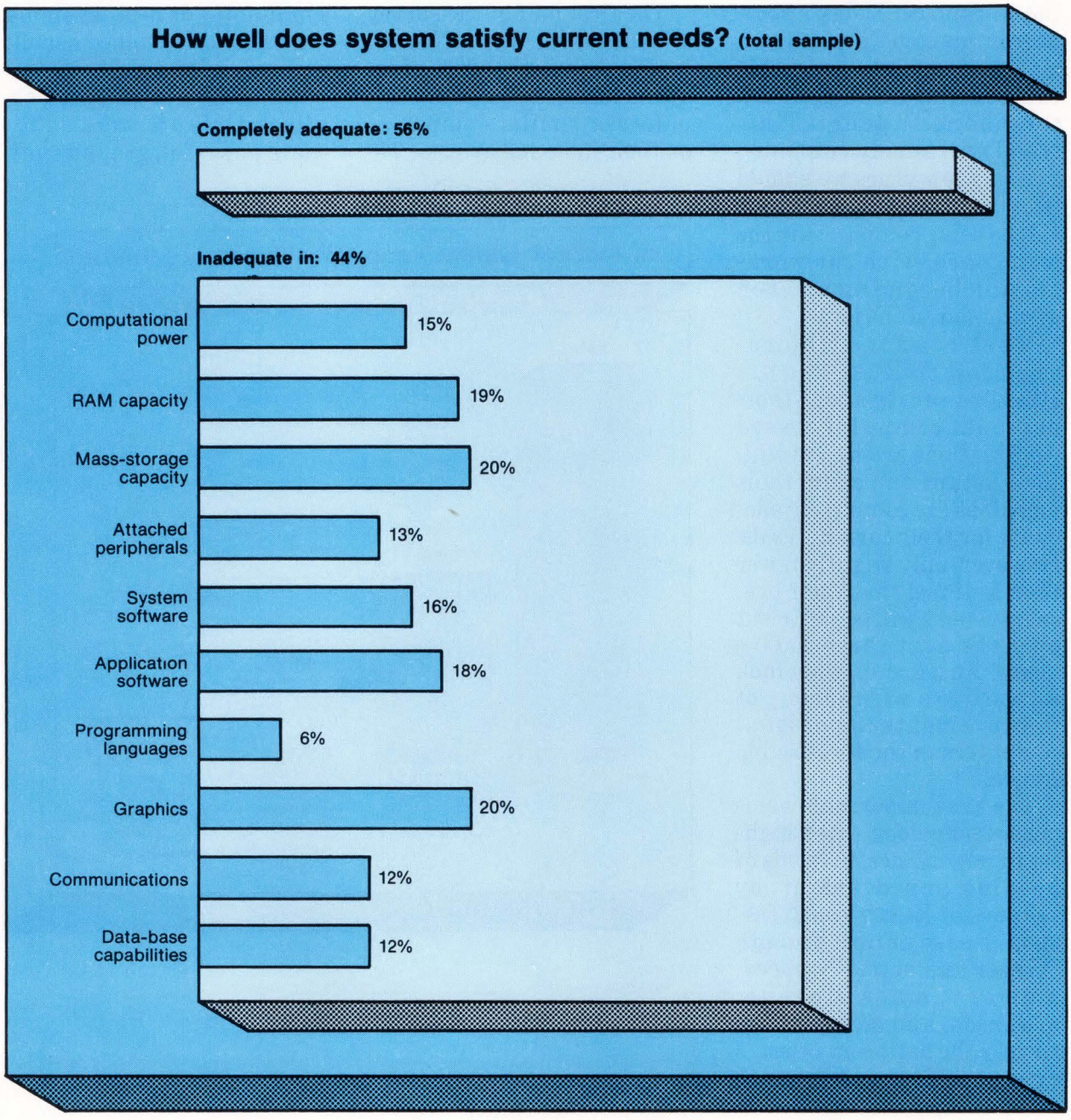


Figure 2


How well does system satisfy current needs? (total sample)
Completely adequate: 56%
Inadequate in: 44%
Computational power
15%
RAM capacity
19%
Mass-storage capacity
20%
Attached peripherals
13%
System software
16%
Application software
18%
Programming languages
6%
Graphics
20%
Communications
12%
Data-base capabilities
12%

ented 32-bit systems, which, incidentally, are inherently more suitable for CAD/CAE applications.

Typically, engineers and other readers use their microcomputers for such applications as word processing, project scheduling and management, data bases, and financial analysis rather than for engineering tasks like design, control, testing, and measurement. The exception to this pattern is the writing and debugging of programs, which more than half the respondents do themselves.

Who uses PCs?

Of the 2000 readers who were sent the questionnaire, about 20% responded. The results are rounded off to the nearest percentage point. Some respondents failed to answer sections of a multipart question, and other questions called for multiple answers. Consequently, the total of all categories in a given situation does not always equal 100%.

The survey reveals that the average personal computer user is a 42-year-old engineering manager specializing in design and development. He uses an IBM PC with 256 to 512 kbytes of RAM and 10 Mbytes of mass storage. His programming is generally done in interpretive Basic or assembler, and when compiling, he most frequently uses compiled Basic or Fortran. PC-DOS or MS-DOS is by and large the operating system of choice, although a significant minority opts for CP/M.

The average system is connected to the outside world via telephone, local networks, and, in about 20% of the cases, an interface for real-time instruments or processes. Aside from communication facilities, the most common hardware enhancements are a floating-point math coprocessor (38%) and high-resolution, bit-mapped graphics screens, both monochromatic (36%) and color (30%). All other hardware add-ons, as well as advanced software features like multitasking, virtual memory, RAM disk, and so forth, are found on less than 30% of the systems.

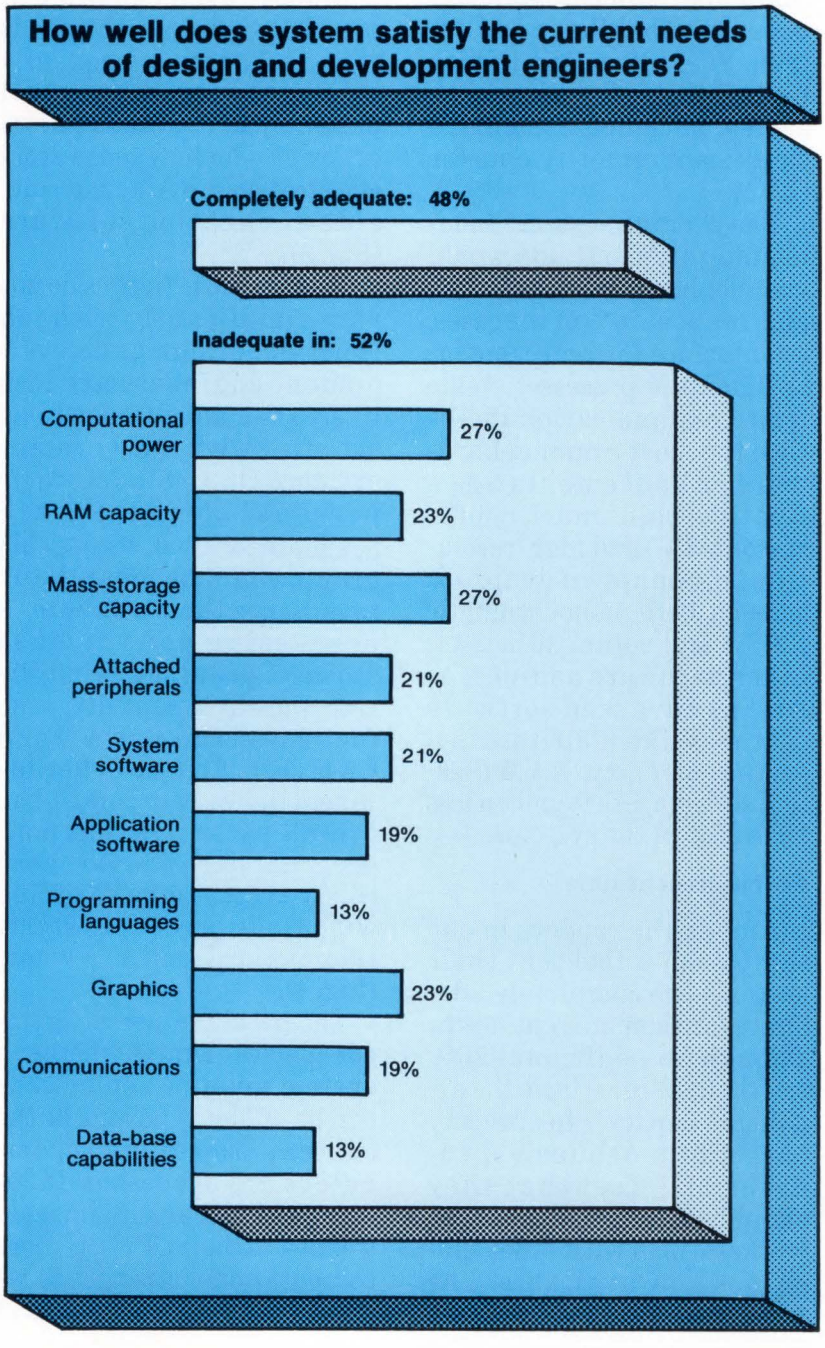
At the present time

Among the readers in our sample, 56% feel that their systems are completely adequate for their current needs. Though an additional 26% say their systems have the expansion capacity to cure any current inadequacies, another 11% feel that they should replace their present workstations with other machines now available. The most demanding lot, 5%, see nothing in today's personal computer arena capable of meeting their current needs (Fig. 1). The most frequently cited shortcomings—all picked by 20% of the readers or fewer—include mass storage, graphics, RAM, and suitable application software (Fig. 2).

Though those figures do not vary significantly with job function, design and development engineers are less likely than anyone else to be satisfied with their present systems. Only 48% feel their personal computers are adequate for their needs. This group would be most likely to enhance their computer's processing power, mass storage, graphics capabilities, and RAM capacity—the facilities vital to CAD and CAE (Fig. 3). One other interesting exception to the overall pattern is that nonprogrammers are far more likely (73%) to be satisfied with their present systems than is the group as a whole (Fig. 4).

The nature of perceived inadequacies dictates whether a system must be replaced or can be enhanced. None of the current crop of microcomputers are processor-independent—all are intimately wedded to their CPUs. If more computational strength is required, the only solution is to

Figure 3



obtain a system with a more powerful CPU. Similarly, the upper RAM addressing limitation of 8- and 16-bit computers can be quite a severe impediment for many engineering applications. Where a multimegabyte memory is needed, a 32-bit system is the answer. Graphics capabilities are similarly system-dependent.

Future needs

Looking into the future, more than half the users think they will need more powerful workstations over the next three to five years to meet their job requirements. Only 17% feel that their present systems will be completely adequate over that stretch, and another 31% can add enough facilities to cure any projected shortcomings. Here too, processor power, mass storage, RAM, and graphics head the list of areas most often deemed to be inadequate, this time by 31% to 40% (Fig. 5).

Once again, design and development engineers are more pessimistic about how their current personal computers will stack up in the future. A full 55% foresee deficiencies in computational power alone. Fewer than one in ten engineers are confident that their systems will be able to handle the difficult assign-

Figure 4

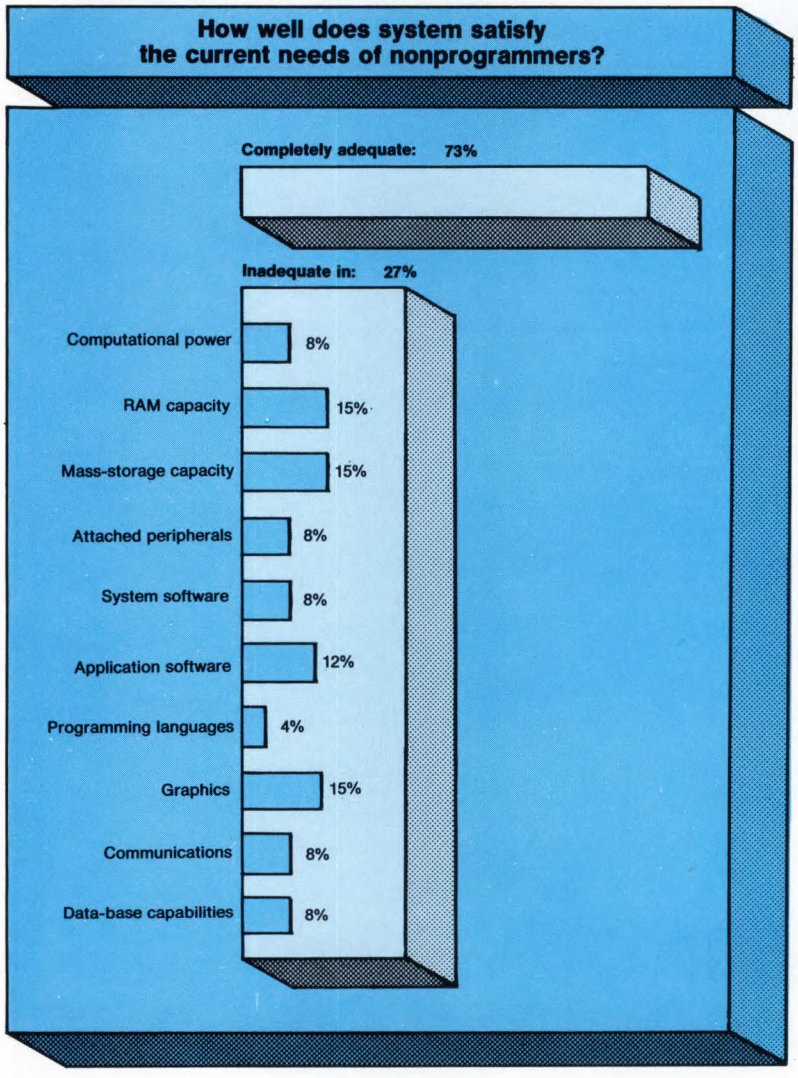
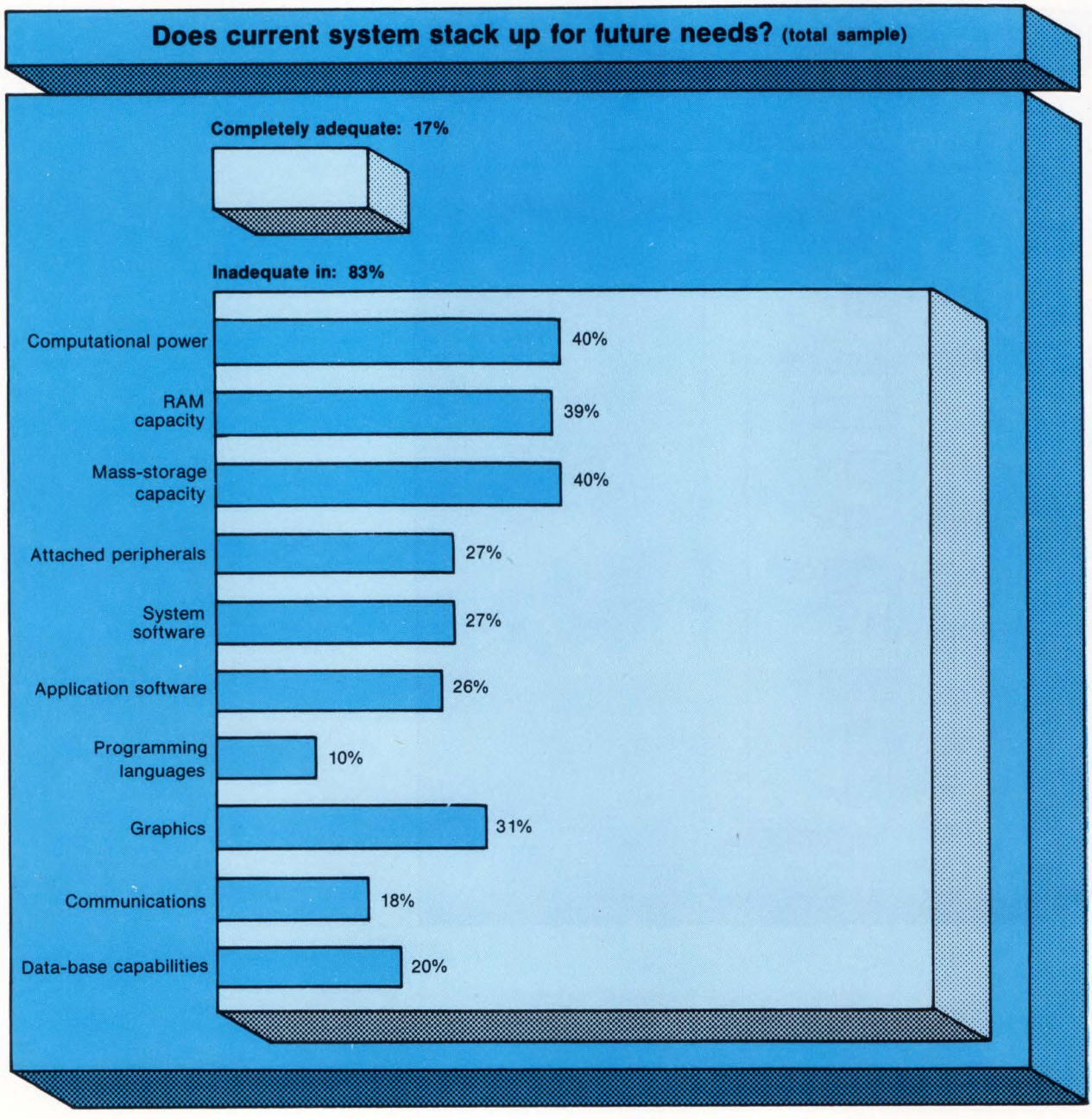

How well does system satisfy the current needs of nonprogrammers?
Completely adequate: 73%
Inadequate in: 27%
Computational power 8%
RAM capacity 15%
Mass-storage capacity 15%
Attached peripherals 8%
System software 8%
Application software 12%
Programming languages 4%
Graphics 15%
Communications 8%
Data-base capabilities 8%

Figure 5


Does current system stack up for future needs? (total sample)
Completely adequate: 17%
Inadequate in: 83%
Computational power
40%
RAM capacity
39%
Mass-storage capacity
40%
Attached peripherals
27%
System software
27%
Application software
26%
Programming languages
10%
Graphics
31%
Communications
18%
Data-base capabilities
20%

ments that lie ahead (Fig. 6). For nonprogrammers, panic is not quite as imminent: 31% feel that their current systems will satisfy their future needs (Fig. 7), and 35% believe their current systems can be enhanced.

With many users looking to replace their workstations in the near future, most are confident that suitable alternatives will be commercially available when they are needed. The big question in many readers' list is whether they will be able to convince management to invest the necessary capital. Only 2% fear that their projected requirements will outpace any advances in personal computer technology (Fig. 8).

User friendliness

When asked to name the area of personal computer technology in most need of improvement, ease of use and the user interface topped our readers' list (Fig. 9). Only 27% consider this area to be relatively unimportant.

To busy managers, who are not necessarily computer professionals, a computer is just a tool and not an end in itself. They are either unable or unwilling to spend precious weeks learning each aspect of a new tool. One can sympathize with the novice who must absorb an operating system and several application programs—each with its own command structures and a set of fat (and often incomprehensible) manuals—before he can profitably use his workstation.

Pet peeves

One Compaq and IBM PC XT user pinpoints his pet peeve as trying to remember which key to push for a given result, especially when the same key has different meanings in different contexts and application programs. He feels that manufacturers should add a new interface device (not a mouse) that will allow him to enjoy a multitude of utilities without extensive reading and memorization. This solution is similar to that of a dedicated word-processing computer, which assigns each key one function during the course of a program. It would, however, limit the flexibility and adaptability of a general-purpose computer.

Facing the interface

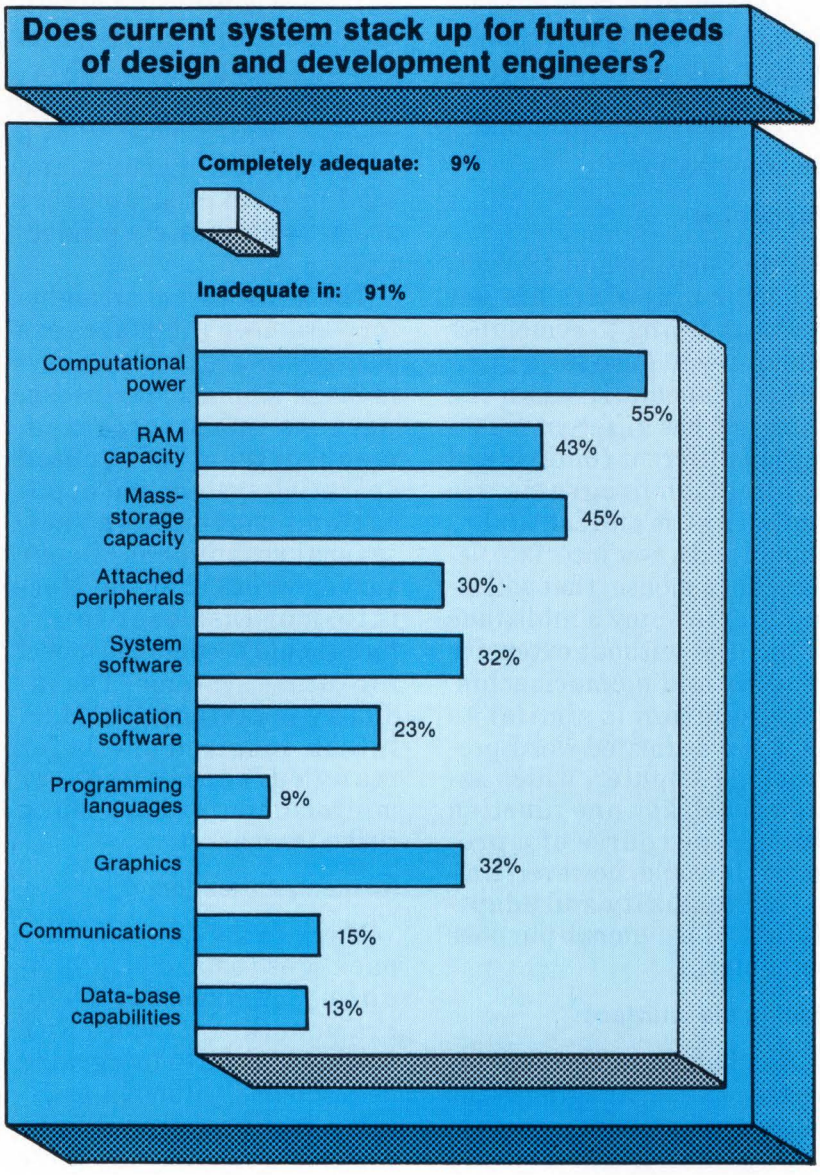
A debate over the user interface has been raging in the microcomputer industry. On the one hand, experienced users know that once a software package is mastered, constant iterations through a nested menu selection process become cumbersome, time-consuming, and irritating. Software containing extensive menu shells also tends to be large and expensive. Novice users, on the other hand, frequently are turned off by a lengthy learning curve and tend to avoid programs that are not immediately productive.

The advocates of straightforward user interfaces are clearly winning the day, as evident in Apple's Macintosh, with its image-oriented, menu-driven, integrated operating system and application programs. In fact, several respondents to our survey wrote that the Macintosh or Lisa user interface should become the model for future systems. The industry is taking note: Macintosh-inspired shells for many currently popular microcomputers are being rushed to market.

No manuals needed

Many fancy new software packages (dBase III, Symphony, WordStar 2000, Framework) are loaded with on-line and fully integrated help screens, tutorials, assistance facilities, and menus. Engineers can fully use these sophisticated packages almost without reading a manual. In the better-designed programs, these aids can be bypassed for direct command

Figure 6



control. The added help facilities require substantially more RAM, mass storage, and processing power than their predecessors.

Speaking frankly

Another group of readers would like voice recognition to become the mechanism of man-machine interaction, with the machine having the ability to recognize ordinary English commands. This has been a prime area of research and development since the beginning of computer history.

Texas Instruments recently demonstrated a rudimentary voice activation system on its Professional Computer—one that could lead to a truly personal computer. The user prerecords a select group of words, which the system recognizes when spoken by the same individual. However, the user must remember the exact commands he recorded and speak them in the same manner all the time.

Other target areas

Processor power and speed are the second most important areas of concern to our readers. Several users of 8- and 16-bit machines would like their next system to use an MC68020 or similar 32-bit CPU. Others just wish for 100 times more speed than their current personal computers

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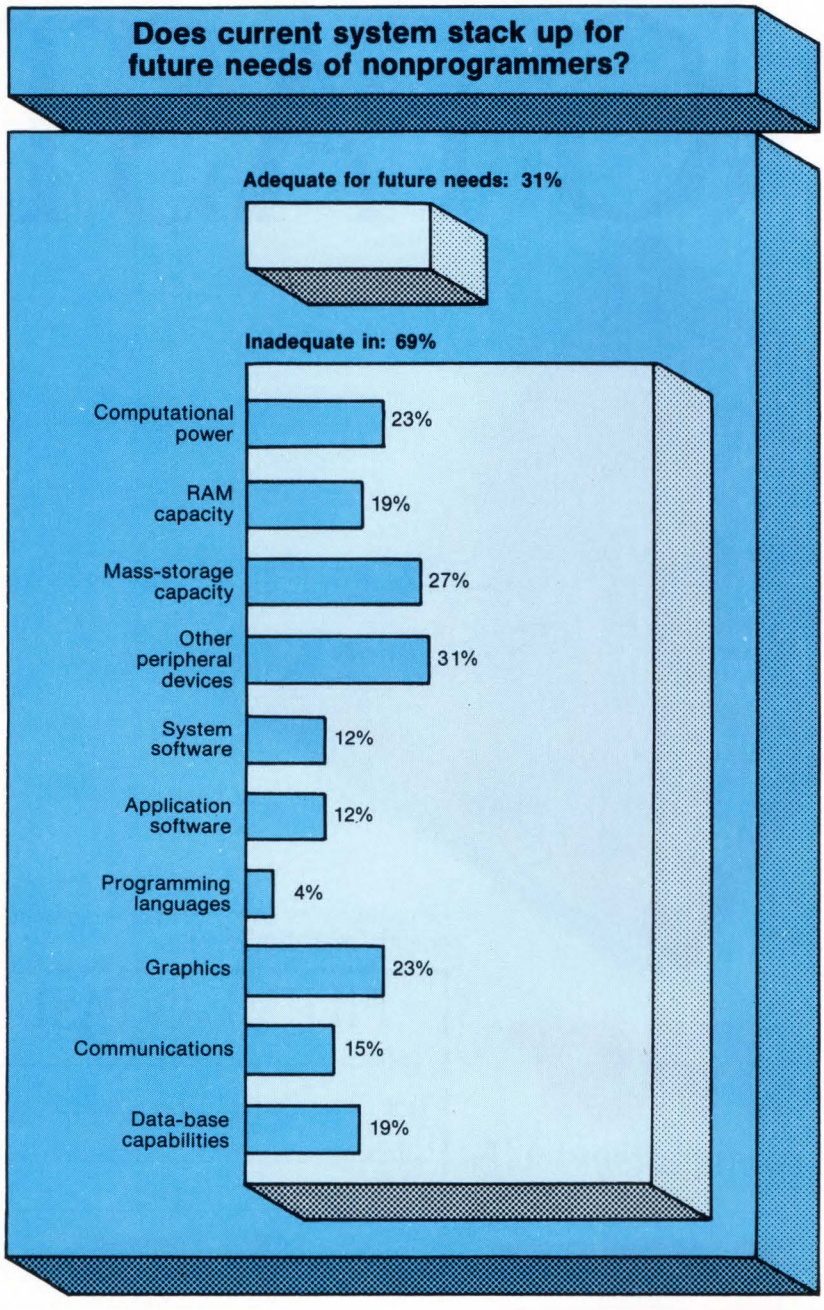
Figure 7



can deliver.

Of course, overall system speed is dependent on much more than raw processor capability. The fastest CPU can appear to be crawling because of inefficient operating systems or application programs or as a result of many calls to slow memory devices, such as floppy disks. The software involved in creating a simple user interface can also exacerbate that inefficiency.

More resolution

Significantly better graphics capability is another high priority. Certainly, the resolution offered by an IBM PC or any 8-bit system is not conducive to IC design. Some 16-bit systems come with enhanced graphics, but at a cost of introducing severe incompatibility with the IBM system. Many graphics systems being developed for 32-bit micros should be capable of supporting the most demanding applications.

More RAM wanted

As soon as any engineer gets used to a computer system, he longs for more RAM and mass storage—a universal plaint. Many readers tell us that they want 1 to 4 Mbytes of RAM and 100 Mbytes to 1 Gbyte of mass storage on their personal

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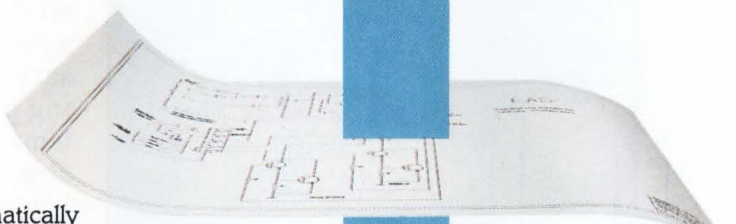

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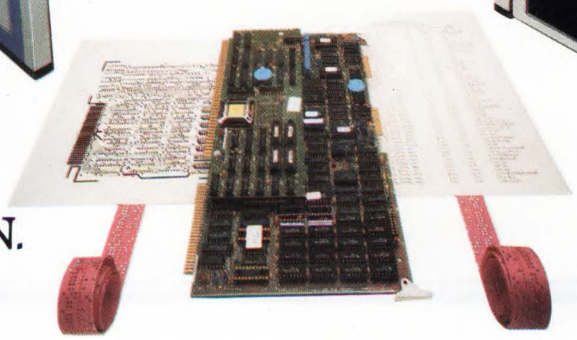

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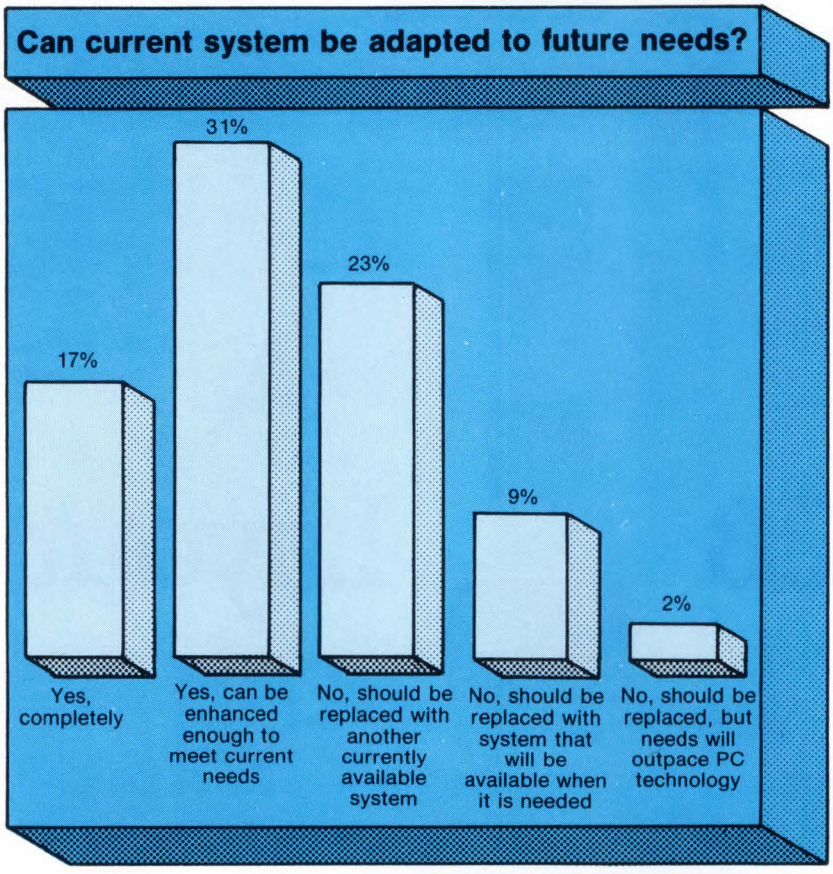
Figure 8



computers.

One engineering manager thinks RAM should never be a primary limitation. A workstation with 2 to 4 Mbytes of RAM and over 100 Mbytes of mass storage, plus an efficient virtual memory management system, should satisfy almost any demanding user. Several such systems are commercially available.

Also on the horizon

Future improvements in application software, local network connections, and printers are also sought. Networking is a relatively new feature and, like application software, is in a stage of rapid development and evolution. Several good networks for larger microcomputers exist today, among them Ethernet, which has become a semi-official standard. One of the most sophisticated is Apollo's Domain network, in which a workstation can take advantage of the computational facilities of remote nodes in addition to shared peripheral devices and files.

Printers advance

The revolution in printer technology has been almost as dramatic as the revolution in microcomputers. Printouts from small systems were all but unreadable. Today, many

YOUR MIND WAS OUR MODEL.

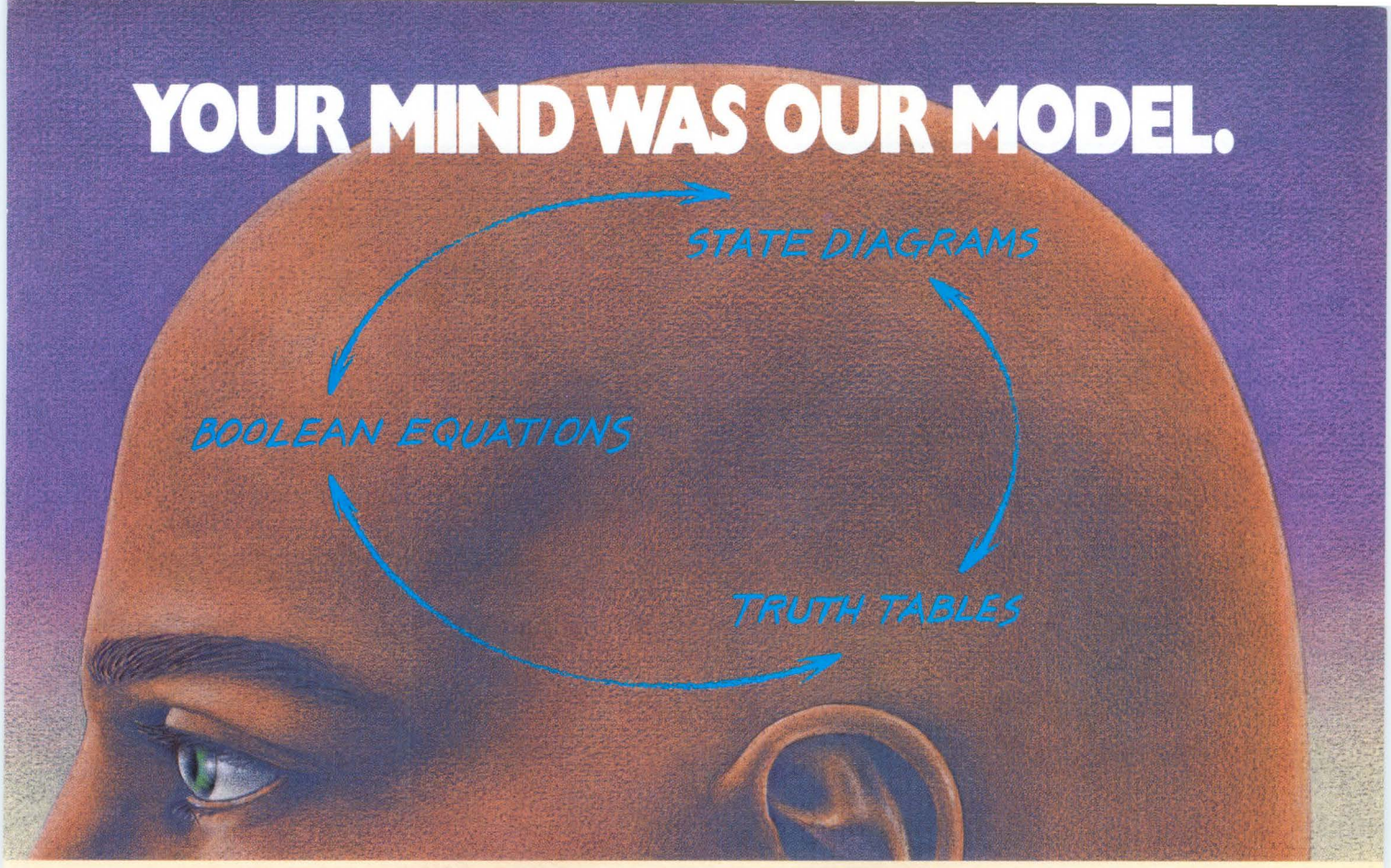


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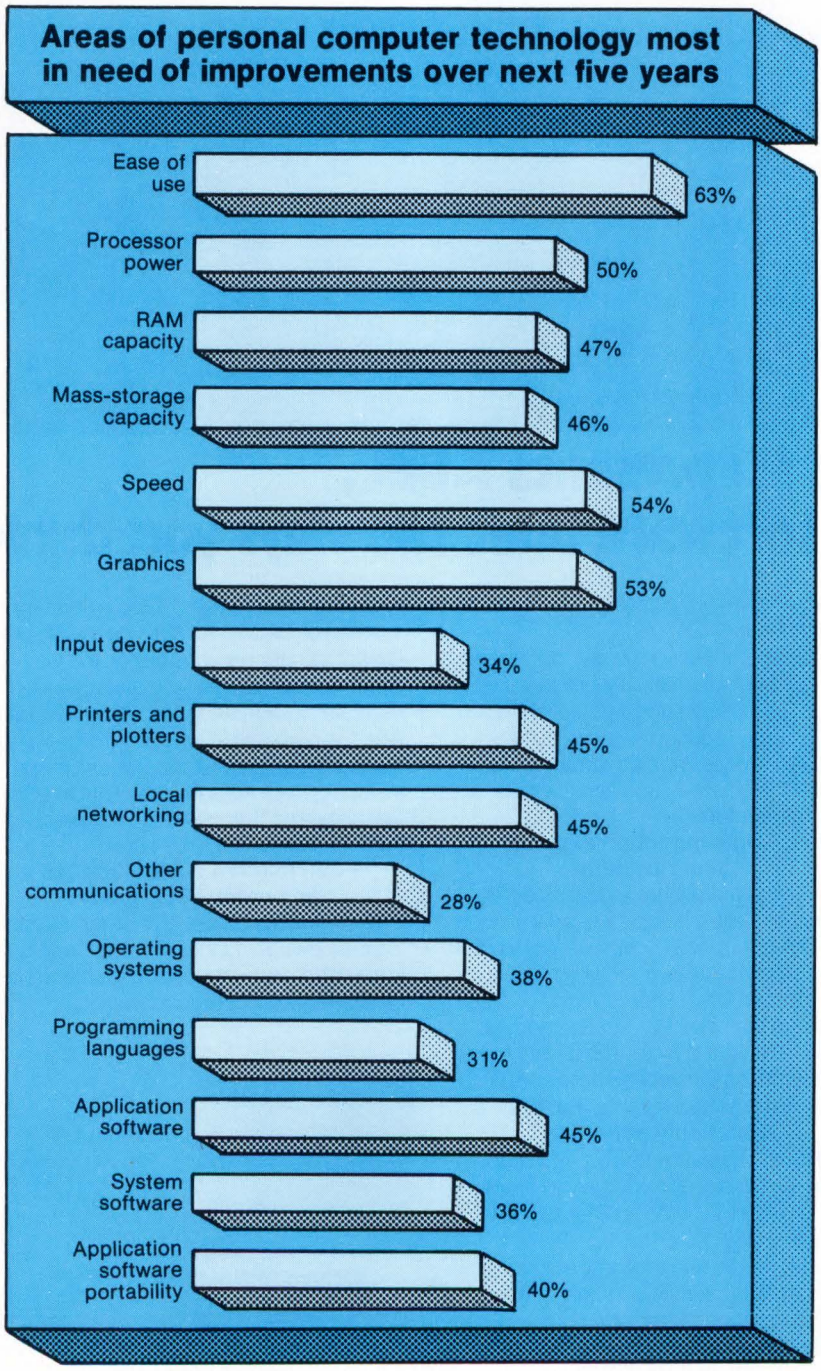
Figure 9



inexpensive printers yield high-quality output. Several readers express a desire for an inexpensive color laser printer. Hewlett-Packard's new single-color Laserjet, which costs around $3000 and is designed for personal computers, is becoming very popular, but several years will elapse before a fast, inexpensive, high-quality color printer is available.

Software portability

It is somewhat surprising that compatibility and system software portability are not higher on the list of priorities. Perhaps the users really do view their workstations as personal computers and thus do not worry about running their programs on other systems. As long as data can be transferred, either through networks or modems, our respondents seem content.

Many of their wishes for future workstations can be satisfied today by the various 32-bit workstations, with their advanced graphics abilities, power, speed, and memory capacity. More and better application software is being offered for these workstations every day. Of course, these systems cost significantly more than the IBM PC, but if recent history is any indication, their prices are bound to come down, too.□

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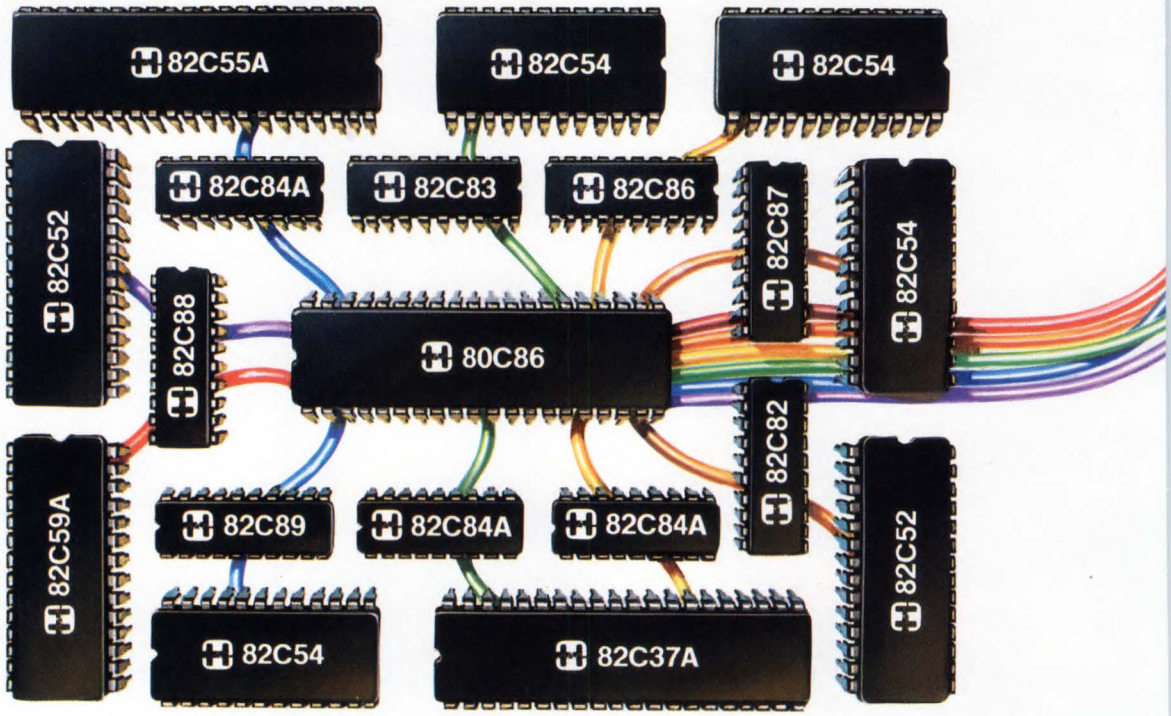

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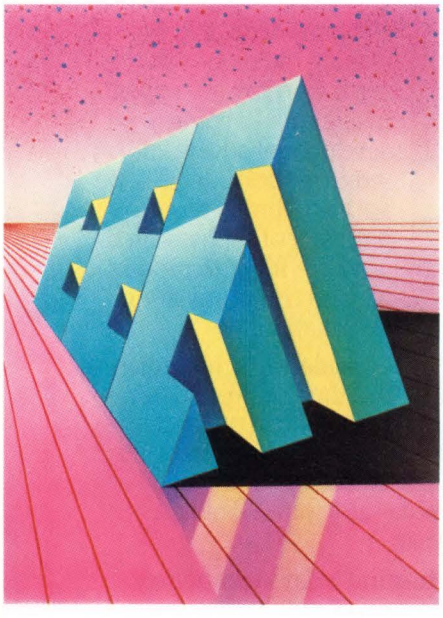

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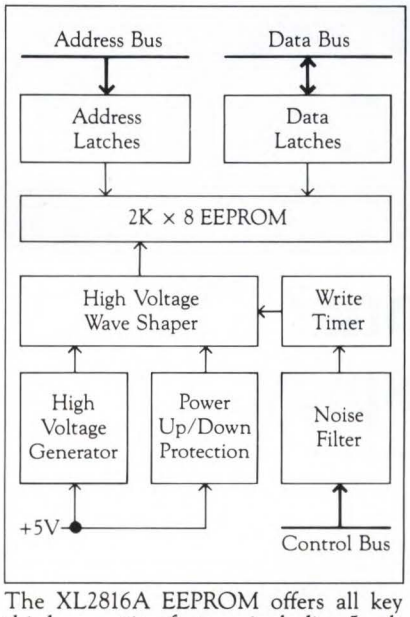

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Pipelined static RAM endows cache memories with 1-ns speed

Synchronizing and overlapping its inputs and outputs on chip, a GaAs RAM passes its 1-ns cycle time to an array with no loss in performance.

A computer can function no faster than its memory will permit. Thus for high-speed machines, designers will often favor cache memory, and for cache memory, they favor arrays of fast static RAMs. After all, every nanosecond saved in RAM access time typically means an equal saving in machine cycle time.

Quick as they are, though, today's RAMs are inadequate for tomorrow's high-performance computers, which will need a machine cycle of 5 ns or less to deliver their proposed 200 million instructions/s. The static RAMs now available demand 7 to 10 ns to be accessed. Arrays of them do still worse, because imprecise timing and skews at the board level add significant delays.

Andy Graham and **Stewart Sando**
GigaBit Logic Inc.

Andy Graham is director of RAM development at GigaBit Logic in Newbury Park, Calif. He holds a BSEE from the University of Texas at Austin. Previously, he designed MOS memory components at Mostek and later led high-density dynamic RAM development teams.

Stewart Sando held memory marketing positions at Intel before becoming director of strategic marketing at GigaBit Logic. He holds a BS in physics and an MSEE, both from the California Institute of Technology, and an MBA from Stanford University.

Speeding to the rescue comes a gallium arsenide static RAM with a 1-ns cycle time—or about the same as the typical transit time of signals across a memory board. Since a signal can propagate at only 15 cm/ns in a transmission line trace, and since a typical cache array can easily span 15 cm even with surface-mounted packages, the RAM design must break with tradition to confer its nanosecond performance on a cache memory.

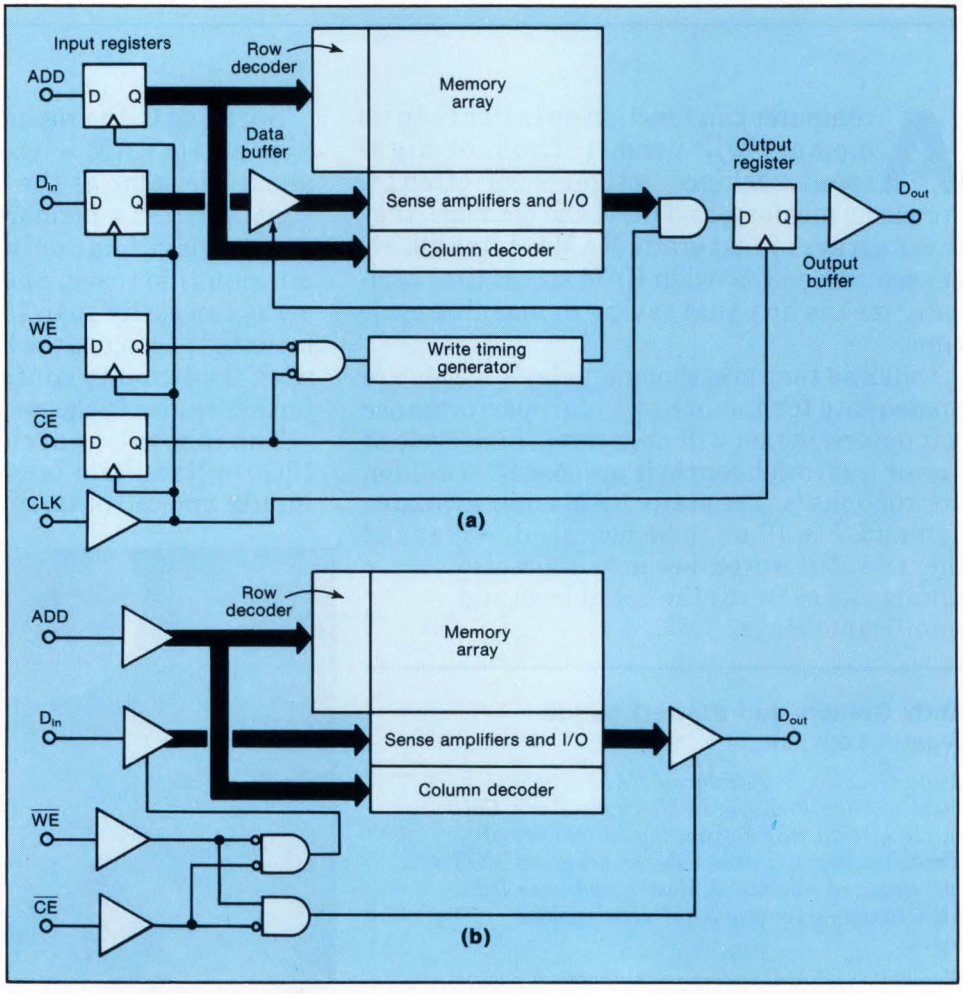
The innovative architecture of the 1-kbit 12G014 NanoRam latches and pipelines both inputs and outputs, internally generates all

needed write cycle timing signals, and is totally controlled by a single clock input (Fig. 1a). Write cycles work in almost the same way and at exactly the same speed as read cycles—another unique feature. Timing complexities are minimal, even at gigabit-per-second data rates. Indeed, the emphasis on speed reaches right down to the memory cell itself (see "Designed for Speed," opposite).

A traditional static RAM, in contrast, does not overlap inputs and outputs but necessitates that address and control information remain stable until output data has left the chip. For cycle times below 5 ns, that requirement is difficult to meet. Also, variations in write cycle timing become extremely difficult to deal with as the write pulse shrinks almost to the vanishing point.

One of the most obvious differences between the architectures of the GaAs memory chip and its conventional static counterpart can be seen in the way in which addresses, data, and control signals are presented to it (Fig. 1b). Normally, these inputs are asynchronous, yet they need to be held valid for the full duration of the memory cycle.

The conventional static RAM's control signals furnish both state information (whether a read cycle or a write cycle is taking place) and timing data (the exact starting and stopping



1. The first 1-ns gallium arsenide static RAM passes its high speed along undiminished to the board level because its on-chip registers, single clock, and internally generated write timing overlap and synchronize its inputs and outputs (a). Lacking those circuit elements, a conventional static RAM cannot pipeline its inputs and outputs or compress its write cycle (b).

Designed for speed

The architectural considerations underlying the 12G014's 1-ns performance extend to the memory cell. For the sake of speed, it has a separate Bit Sense line, as well as a third transistor that separates the bit-sensing current from the cell's sustaining currents.

The Word Line for selecting rows goes low when active. The Bit Sense line allows the cell to sink or not sink current depending upon the data it holds. The line is biased to an appropriate voltage level by column-sensing circuitry, and the presence or absence of current drawn by the cell is easily detected.

The simplified schematic shown in Fig. A illustrates the basic read operation of the cell. The selected Word Line is first grounded, while all others stay high, and the Data Write lines, which are inactive during a read operation, are also grounded. Next, the Bit Sense line of the selected column has a positive read current source, I_R, applied to it. Its value is half of the saturated drain current of transistor Q_3.

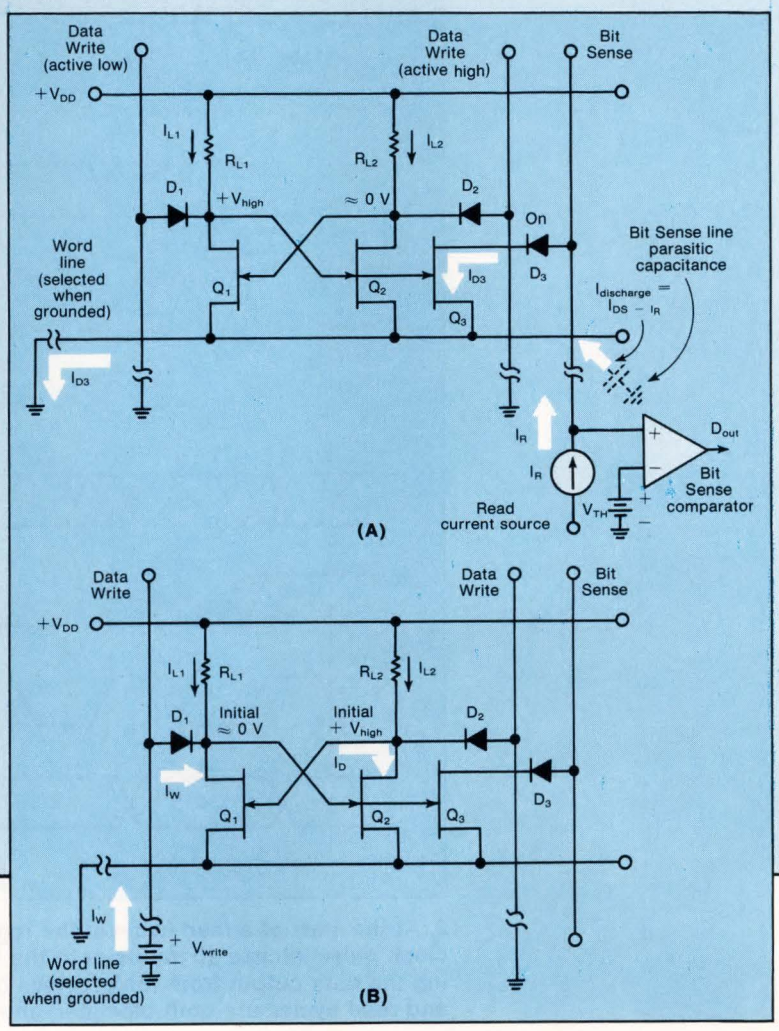
When the cell is storing a 0 (Q_1 is off, Q_2 and Q_3 are on), the Bit Sense line is quickly discharged by the current I_{D3} minus I_R, and the bit sense comparator produces a logic 0 output. Alternatively, if the cell contains a 1 (Q_1 is on, and Q_2 and Q_3 are off), then Q_3 remains off even when the selected Word Line is grounded. I_R then charges the Bit Sense line and the comparator produces a 1.

The presence of the third device, Q_3, in the memory cell allows I_{D3} to be totally independent of the cell's sustaining currents I_{L1} and I_{L2} and hence independent of the load resistance, R_L, and the static power of the memory array.

The basic memory cell also employs differential Data Write lines that are separate from the Bit Sense line. To write, one of those lines is momentarily brought high, thereby directly charging through a diode the drain of Q_1 and the gates of Q_2 and Q_3 to a high level. With Q_2 now on, the gate of Q_1 is quickly discharged to $\approx$ 0 V, completing the write. (In Fig. B, a 0 is being written to a cell that holds a 1.)

At no time during the write operation is either of the sustaining load currents used to charge nodes. The Data Write lines directly supply the high voltage level desired on the internal cell nodes. The resultant extremely short write time is totally independent of the static power dissipation of the memory cell.

Because the Bit Sense line is independent of the Data Write lines, it can continue to have the same bias during both write and read cycles. This makes for the fastest possible write followed by a read cycle. With memory cells using common Write/Sense lines, the bias used to sense the cell is totally overdriven during a write cycle. The delay that typically occurs before the read bias is reestablished (known as a write recovery time) is totally eliminated with this cell configuration.

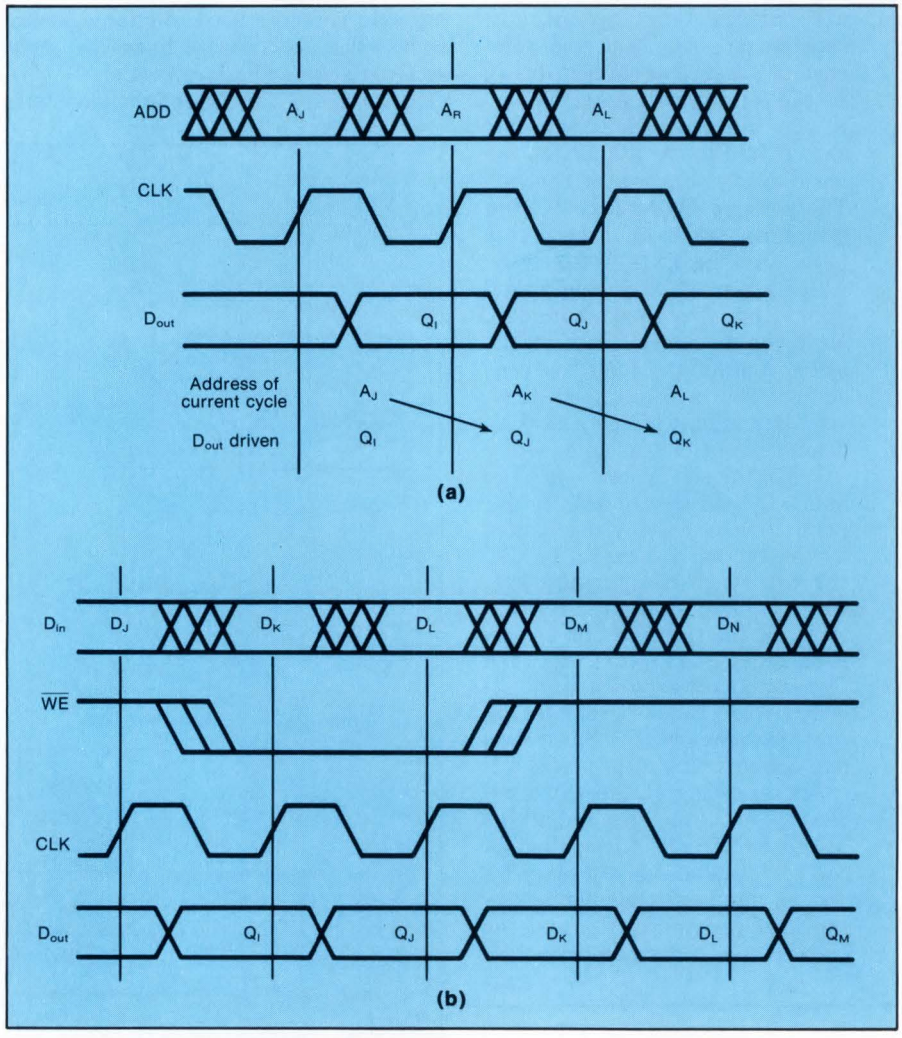


point of a cycle). Most of the timing information demands that various setup and hold conditions be met, particularly for write cycles. And the independence of all of the input signals gives rise to a host of possibilities regarding the relative timing of all edges.

Also important is the new static RAM's tremendous simplification and improvement of write cycle timing. From a user's point of view, write and read cycles of equal duration are highly desirable, but historically this has not been the case. Most systems, as a result, have had their memory cycles limited by write cycle considerations.

The length of the write cycle of a traditional static RAM is determined by adding several parameters. These are the address setup time, the rise and fall times and pulse width of write enable, the address hold time, and the address transition—the time needed to reach the next address. Therefore, it is not unusual to find systems whose write cycle runs to more than twice the duration of the read cycle.

Further, at 1-ns speeds the write pulse of conventional static memories is exceedingly narrow. Such pulses can be generated—at least in theory—but exactly where the falling or rising edge will lie is enormously uncertain. Prac-



2. At the start of a read cycle in the register mode, the rising edge of a single clock pulse latches all inputs onto the 1-ns RAM while simultaneously loading the data output from the previous cycle into the output register (a). Write and read cycles are both pipelined and are equally short (b).

tically speaking, even creating a 2-ns pulse is exceedingly difficult.

The architecture of the new GaAs chip solves both of these problems. Latching the Write Enable ($\overline{WE}$) signal at the start of the cycle and internally generating all requisite timing signals means that the timing of the write cycle is identical to that of the read cycle. Totally eliminating the write pulse, of course, obviates the problems that go hand in hand with producing very narrow pulses.

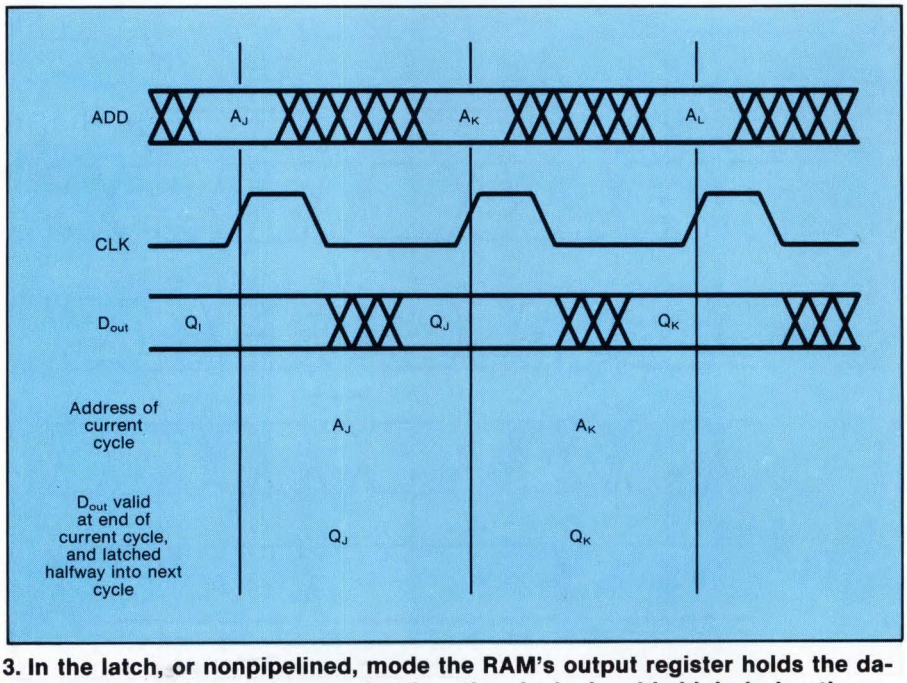
Inner workings

The internal operation of the 256-by-4-bit chip is totally self-timed. In operation, a single clock signal initiates a new memory cycle (Fig. 2a). The Address (ADD), Data Input (D_{in}), Chip Enable ($\overline{CE}$), and $\overline{WE}$ signals are all latched into on-chip registers by the rising edge of the Clock (CLK) pulse at the start of a memory cycle.

Those signals remain valid throughout the memory cycle—until the next rising edge of CLK. Because all of the inputs are latched internally, the external signals need not stay stable for the entire cycle: They can thus begin slewing during one cycle to prepare for the next.

Another set of registers, situated just before the output drivers, is latched by the same rising edge that initiates a cycle. In other words, as the output data from a given cycle is strobed into the output registers, the new addresses, input data, and control signals are loaded into the input registers to start the following cycle. Once the output data is packed into its registers, it remains valid for the entire cycle, that is, until the next rising edge of CLK.

As noted, the write cycles have exactly the same timing as the read cycles (Fig. 2b). The data input registers are loaded at the start of each cycle, whether it is a read or a write. In the first case, they are simply ignored. In the second, provided that $\overline{WE}$ is low when a cycle begins, an internal write operation proceeds for



3. In the latch, or nonpipelined, mode the RAM's output register holds the data output from the previous cycle when the clock signal is high during the first part of the new cycle. When the clock goes low, it makes the new output available for the rest of that cycle and for part of the next.

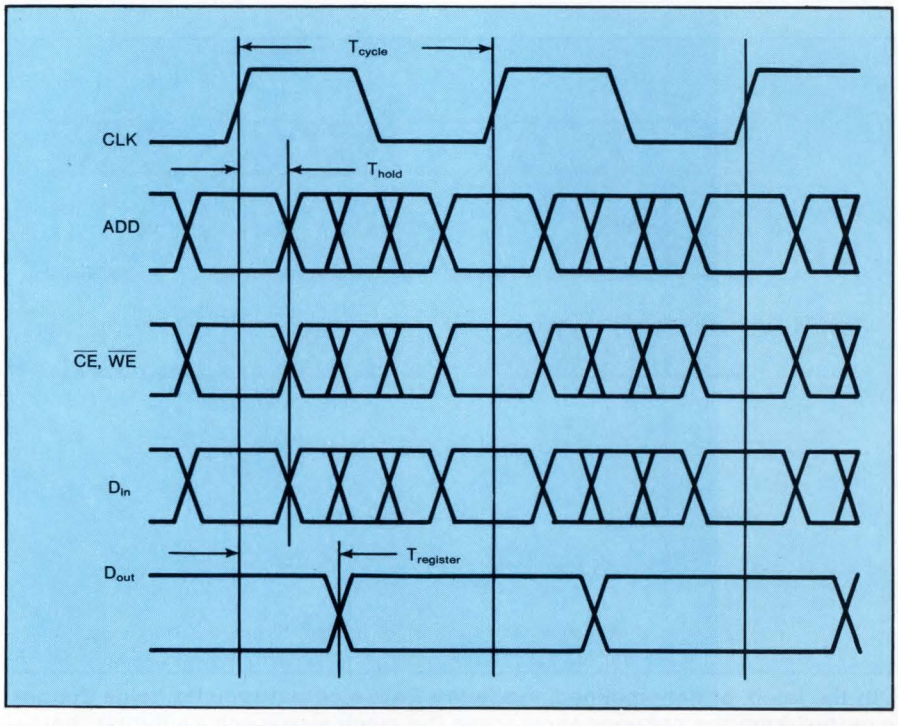
both writing data into the memory cells and then restoring internal write lines to their original condition. The output of the write cycles will exhibit the same timing as the read cycles but will reflect the new information.

In the memory chip's architecture, the control signals convey state information but not timing information. These signals, $\overline{CE}$ and $\overline{WE}$, are latched along with all the addresses and input data by the rising edge of CLK. Setup and hold times for all inputs are identical, which simplifies timing in a pipelined system. The sum of the setup and hold times (known as the required valid window) takes up only 30% of the overall cycle time—a percentage that allows the inputs to get ready for the next cycle. This ability is particularly important when the speed of the memory chips is approaching that of transition times and board-propagation delays.

The on-chip output registers work in two modes. In the register mode, the registers operate as positive-edge-triggered D flip-flops and latch the output data for the duration of the cycle. This setup yields the highest possible bit rate at the system level because the output signals have the greatest time to slew and propagate while the following cycle is being initiated. As noted earlier, in this mode the output data for a given cycle will appear at the chip outputs after the device is clocked a second time, starting the next memory cycle.

Some applications, however, cannot wait a full cycle to obtain the data from the current one. Typically, these tasks call for both a cycle time of 5 to 10 ns and an access time of 1 to 3 ns. For such situations, the latch mode exists (Fig. 3).

In it, the output register functions alternately like a single-rank latch, holding the data output when the clock is high, and when the clock goes low, like a feedthrough path leading di-



4. These two back-to-back memory cycles show the only three timing points critical for testing the 1-ns RAM—the cycle, hold, and register access times.

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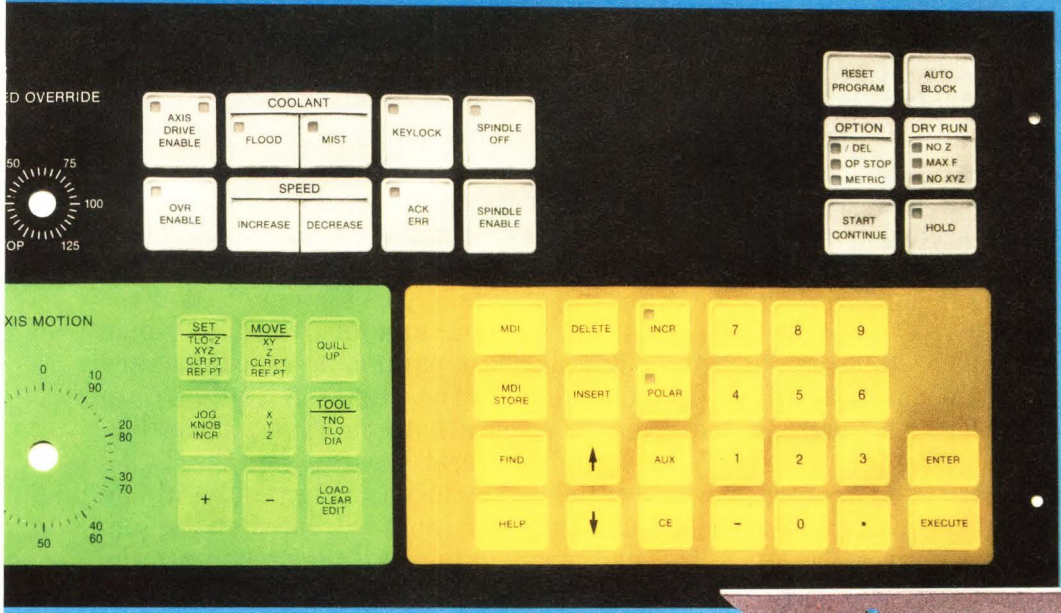

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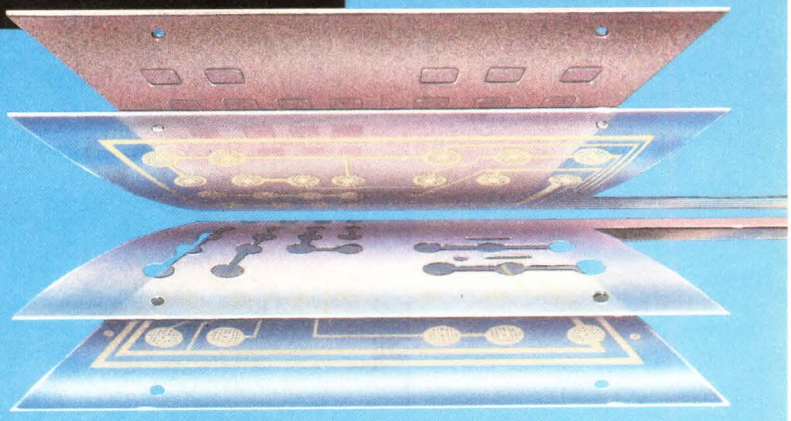

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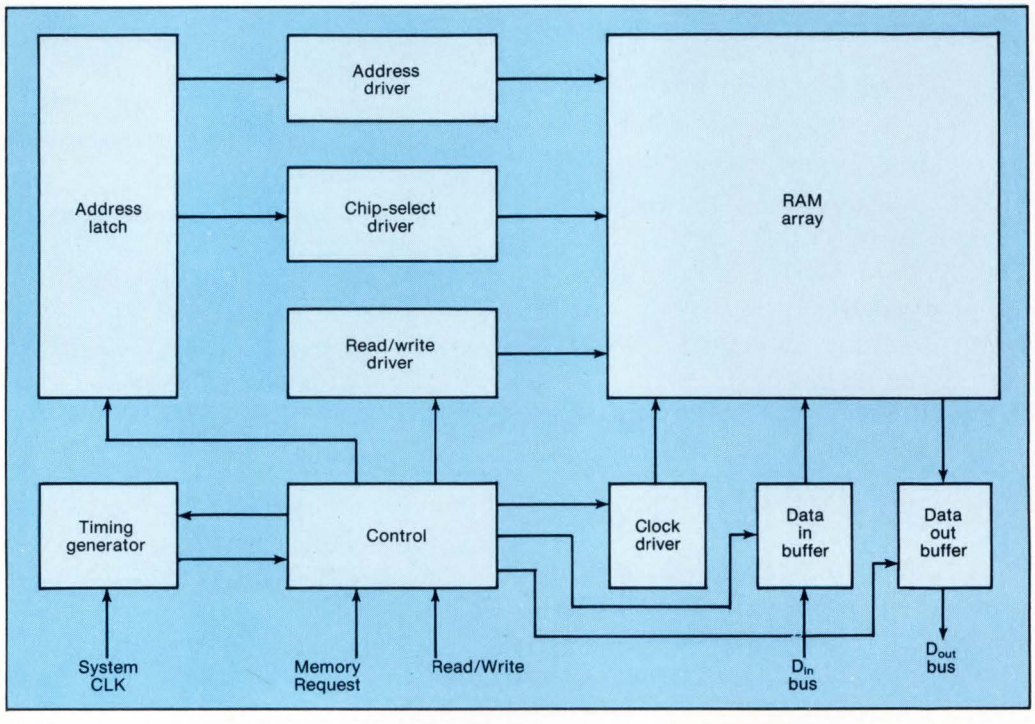
CIRCLE 78

rectly from sense amplifiers to output drivers. More specifically, the data output becomes available during the second half of the on-going cycle, while the clock is low, and is then held valid for the first half of the next cycle. In either mode, the output is held stable at least halfway into the next cycle, so that a second cycle can start before the system has sampled the data from the first cycle.

The big picture

In sum, the GaAs static RAM's architecture solves the fundamental problems of designing high-speed memory systems. The input registers give all addresses, input data, and control signals a large percentage of the cycle to slew and to propagate to all chips in an array before the clock latches them in. Likewise, the outputs have most of the cycle to slew and propagate back before being strobed out at the board edge. Consequently, cycles overlap significantly, since a new one starts before the data output from the previous one even becomes valid at the chip output—let alone at some distance away along a pc board trace. Finally, eliminating the exceedingly narrow write pulse itself yields tremendous benefits in terms of system performance by doing away with the additive parameters that formerly governed minimum cycle time.

Running at 1 ns places stringent requirements on the pinout of a memory chip. Noise and crosstalk are of paramount concern, as are package lead lengths. Hence, a leadless chip carrier with pins all around is very desirable. Viewed from above, all inputs except the clock's are located on the left and right sides of the package. The clock input is located on the top. This arrangement makes it possible to run the clock line perpendicular to all other inputs, thereby minimizing crosstalk. Since the chip's timing demands that all inputs be stable when the clock is strobed, placing the clock pin at a right angle to the rest of the inputs will prevent



5. The circuitry needed to create an interface for an array of 1-ns GaAs static RAMs is simpler than usual because it can exploit the device's self-timing capability.

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noise that results from the clock transition itself coupling onto nearby input lines.

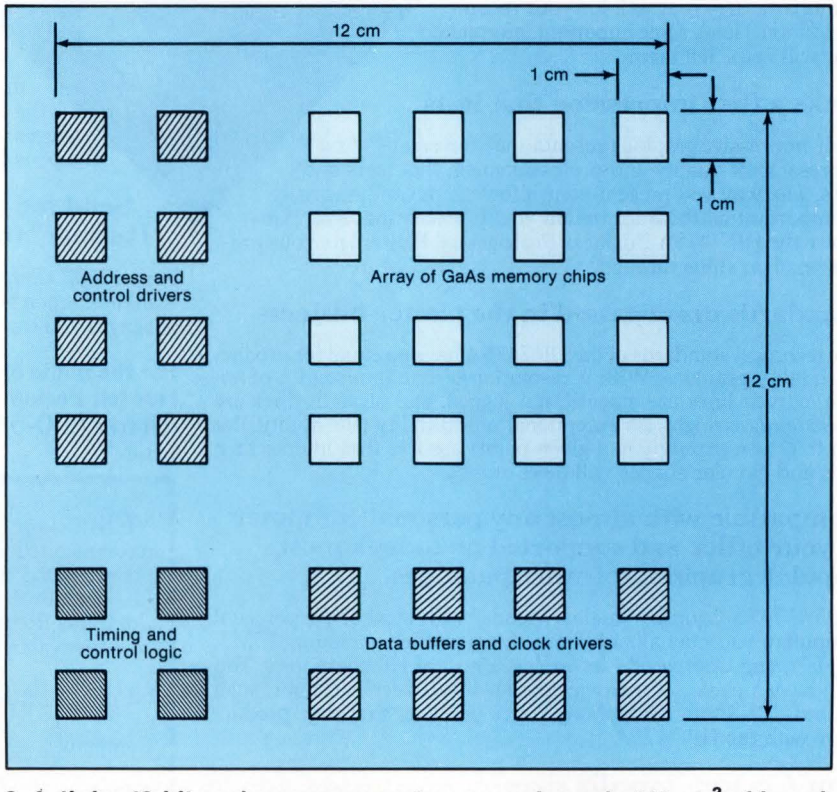
The data outputs are situated along the bottom of the package to allow for the necessary orthogonal positioning of addresses and data lines on the board. Like the inputs, the data outputs are quiet when the clock is strobed to start a new cycle.

Moving in step

All signals going to and from the memory chip are stable when the clock triggers a new cycle, and all signals then shift to their new states on that clock's rising edge. In fact, the outputs do not move until after the input hold time requirement has been satisfied, which further reduces the risk that noise coupled in from other I/O lines will mis-strobe an input. Predictable signal values and a lack of signal interaction are the consequence of the straightforward device timing. Both are enhanced by the simplicity of board layout that results from the chosen pinout.

The performance and ease of use of the memory chip is readily seen in three basic examples. In the first, the device's pipelined cycle timing dramatically eases testing a 1-ns memory. The entire chip can be checked out by ensuring that just three critical timing points are accurate to within 100 ps for independently placed edges (Fig. 4). As discussed, the rising edge of the clock controls the device. The hold requirement relative to the clock is identical for all inputs. The access time of the output register relative to the clock is the final crucial parameter. The test for the write cycle is identical—and just as easy.

In contrast, a traditional static RAM work-



6. A 1k-by-16-bit cache memory system occupies only 144 cm^2 of board space and achieves a 1-ns cycle time.

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ing at 1 ns would require placing and measuring ten 100-ps setup, pulse-width, and hold-time parameters within a 1-ns cycle—a difficult task even at the test head. And the three timing edges used to test the GaAs memory are also the three timing parameters used to implement board-level designs.

Four by four

Designing a 1k-by-16-bit GaAs cache memory board demonstrates how to realize the fastest memory arrays. Sixteen of the 256-by-4-bit chips implement a typical cache structure consisting of four 256-by-16-bit blocks of memory. Doubling up the basic 16-bit-wide design allows 32-bit words to be processed.

The interface circuitry is set up with either GaAs MSI logic or GaAs LSI devices whose memory logic is embedded within a gate array or custom foundry chip (Fig. 5). The circuitry differs from a traditional static RAM interface in only two respects. Clock drivers are added to drive the memory array, and timing generation is simplified, since only the rising edge of the memory cycle clock is critical.

At nanosecond speeds, board layout is very important (Fig. 6). Surface-mounting packages create a dense board and reduce trace lengths. The memory chip and logic interface circuits are packaged in standard 1-cm-square leadless chip carriers with 40 pads on 40-mil centers. There is room for distributing the decoupling capacitors within the array, as well as for the resistors that terminate the transmission lines at the opposite sides of the array from the interface circuitry.

The chip's pinout helps minimize the distances the traces of address and control lines must travel along each row and keeps down the length that data and clock lines must stretch along each column. A set of interface drivers is supplied for every row and column to limit fanout to only four memory chips and to keep trace lengths to about 12 cm. This arrangement holds transit times from the interface circuits along the transmission lines to the far side of the memory array to 800 ps.

The timing of the 1k-by-16-bit cache array is determined by the combined performance of the GaAs memory chips, the GaAs interface circuitry, the signal transit times, and the skews in all of these elements. GaAs interface circuitry introduces gate delays of about 400 ps with rising and falling edges of 250 ps and device skews of 200 ps. The array traces tack on 800-ps transit time delays with 200-ps skews due to minor variations in length and load.

The clock signal is delayed 300 ps with buffer gates and is routed to the input buffers and data buffers over trace lengths that are equalized to deskew the signal at the edge of the memory array. The nondelayed clock is similarly routed to the gates that pass the signal along to the array. The timing that results at each RAM in the array establishes a hold time of 300 ps for the inputs relative to the clock.

The timing will also strobe the output data buffers at the edge of the array 200 ps before the output data can start to change. At this point, memory chips have latched in the new cycle's inputs and started driving the previous cycle's outputs.

A full 800-ps transit time is allowed for the output data to travel to the edge of the memory array and for the next cycle's address to enter the array. Because of the pipelined architecture of the memory chip, 70% of the 1-ns cycle—that is, at least 700 ps—is allowed for memory array input and output transit times. Both are transparent to the RAM's operation on internally latched commands and data. This 700 ps can be subtracted from the additive cycle time components.

In this example, the total cycle time is equal to the sum of the interface propagation delay, rise times and skews, the transit times and skews, and the chip's input hold time minus the pipeline transparent time. In picoseconds that adds up to $400 + (250 + 200) + (800 + 200) + 300 - 700$, for a memory cycle of 1450 ps. The need to control only one clock edge, one hold time, and one data strobe within a memory cycle makes this nanosecond implementation practical.

A GaAs RAM built along conventional lines and dropped into the same board would not have the advantage of pipelining, thus adding at least 700 ps to the read cycle. Further, the RAM's write cycle would be stretched at least another 2000 ps to allow for a valid setup, write pulse, and hold period within the time that addresses remained valid. (The overall write pulse

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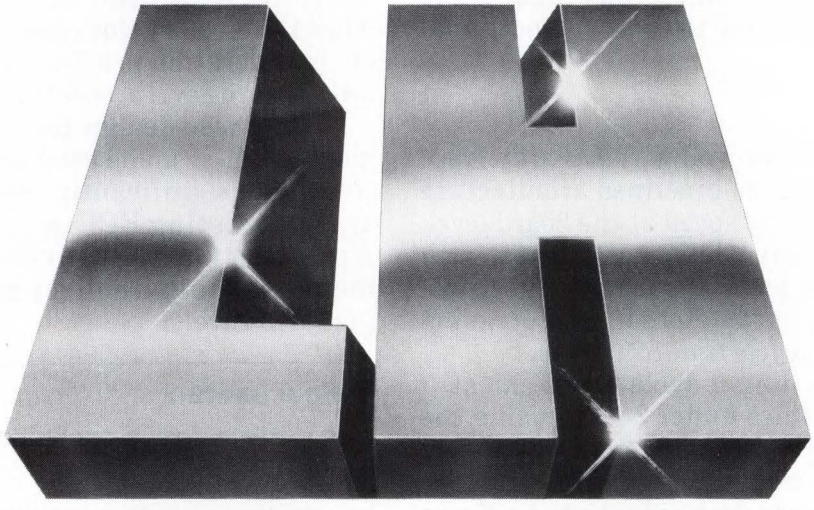

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width alone would need to be 1300 ps, which would comprise the requisite 800-ps array transit time and the 500-ps minimum per-chip write pulse called into play while all the other array interface signals were held stable for the write cycle.) That would add 2700 ps to the 1450 ps for an ideal write cycle, driving the cycle time up to 4150 ps. Practically, that figure would be nearer 5000 ps because of the need to independently set, or time out, all the edges and pulse widths necessary to control traditional static RAMs.

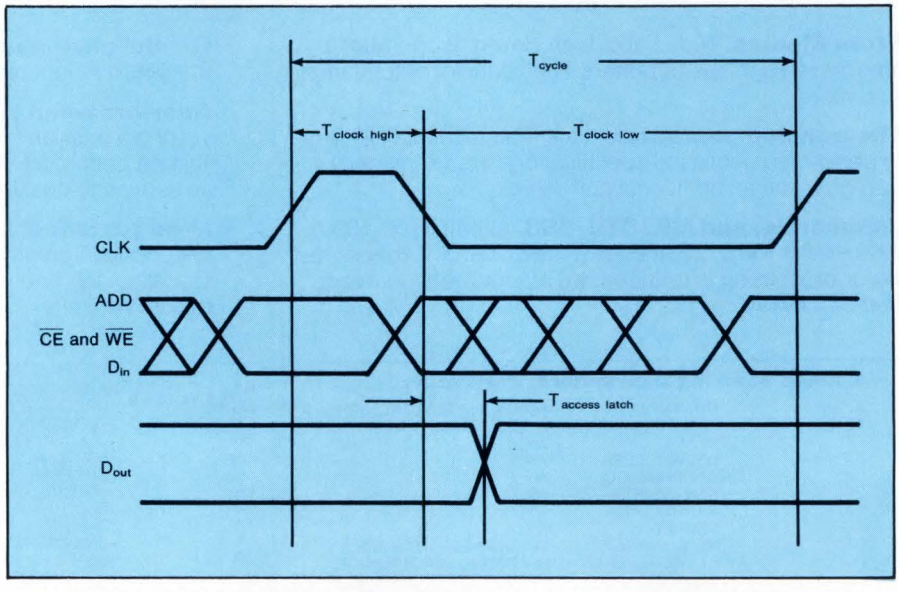
The ECL option

The memory works well with ECL interface circuits, too, since the pipelined architecture preserves most of the speed at the board level. Fast ECL gates have delays of 1500 ps, with 1500-ps rise times and 750-ps skews. Substituting these timing parameters in the foregoing board results in a cycle time of 4350 ps.

Systems with longer cycle times can still achieve access times under 2 ns by using the latch mode, in which the memory output becomes valid during the current cycle. For example, the memory clock signal can be timed asymmetrically to be high for 2 ns and low for the remainder of a 7-ns cycle. When the clock line is high, the inputs and controls are pipelined. With the output in the latch mode, the output data for the present cycle appears at the output when the memory clock goes low, rather than waiting for the next rising edge of the clock. The output data then leaves the memory array. Again, both read and write cycles are identical, with valid output data appearing when the memory clock goes low. The net result of this operation is a 7-ns memory cycle with a 4-ns board-level access time (Fig. 7).

With these design techniques, the GaAs memory chip can be used with ECL interface circuits to significantly extend the performance of existing ECL or new ECL systems. And with GaAs interface circuits, the memory chip can deliver nanosecond cache performance.□

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543



7. Memory systems with long cycle times of, say, 7 ns can still attain a 4-ns board-level access time if they use the 1-ns GaAs RAM chip in the latch mode and set the memory clock signal high for 2 ns only.

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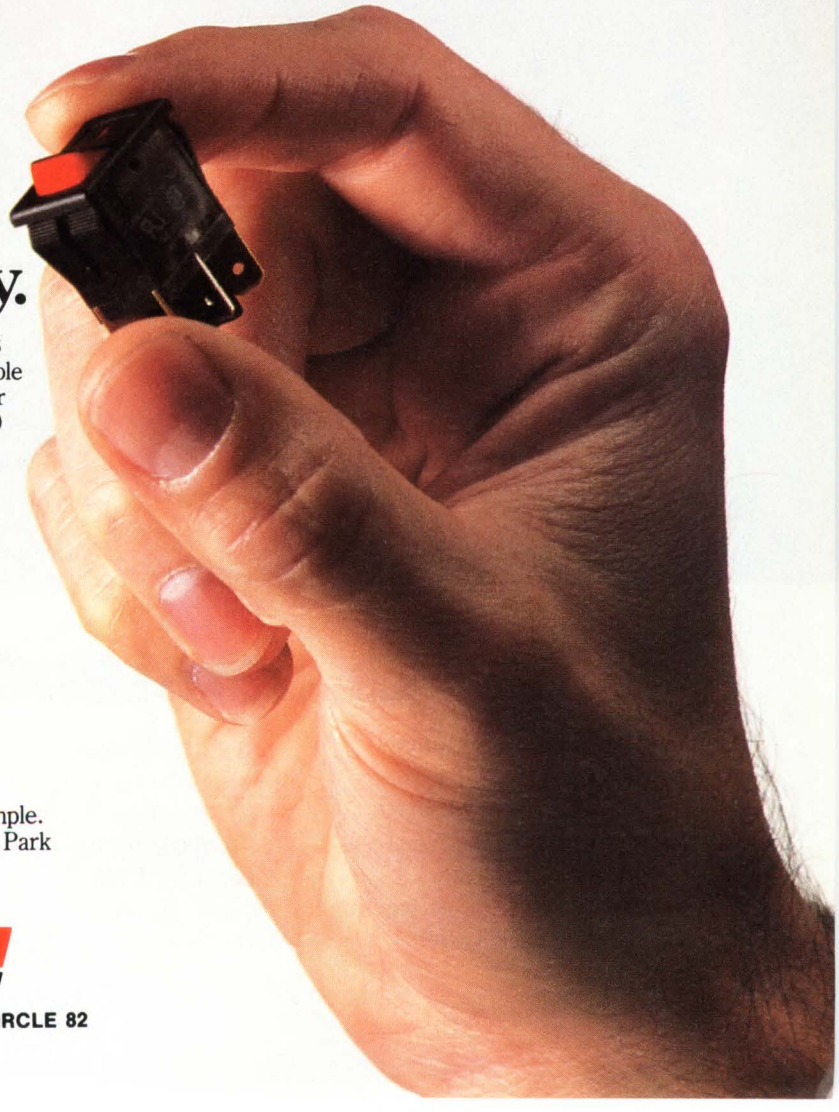

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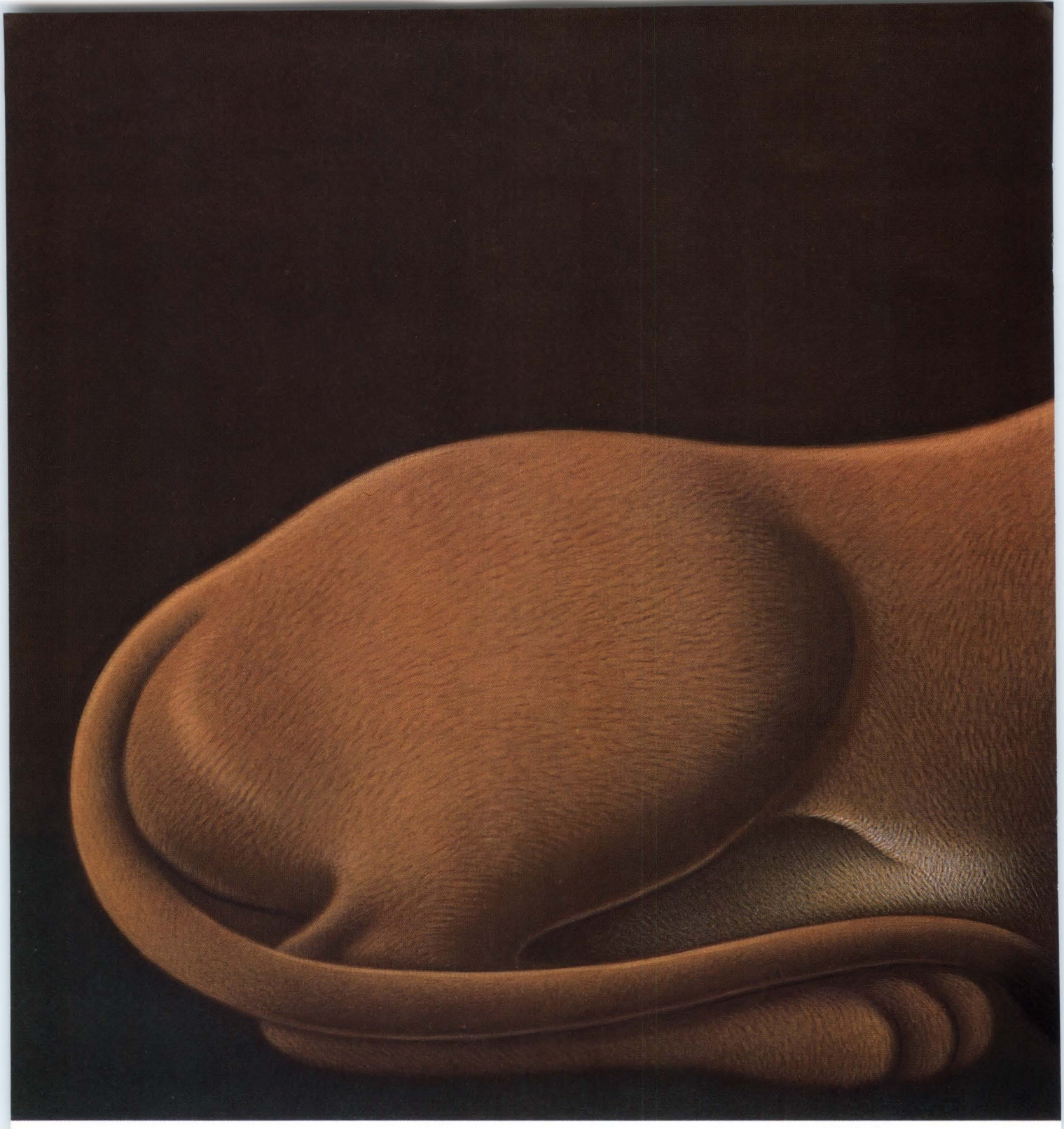

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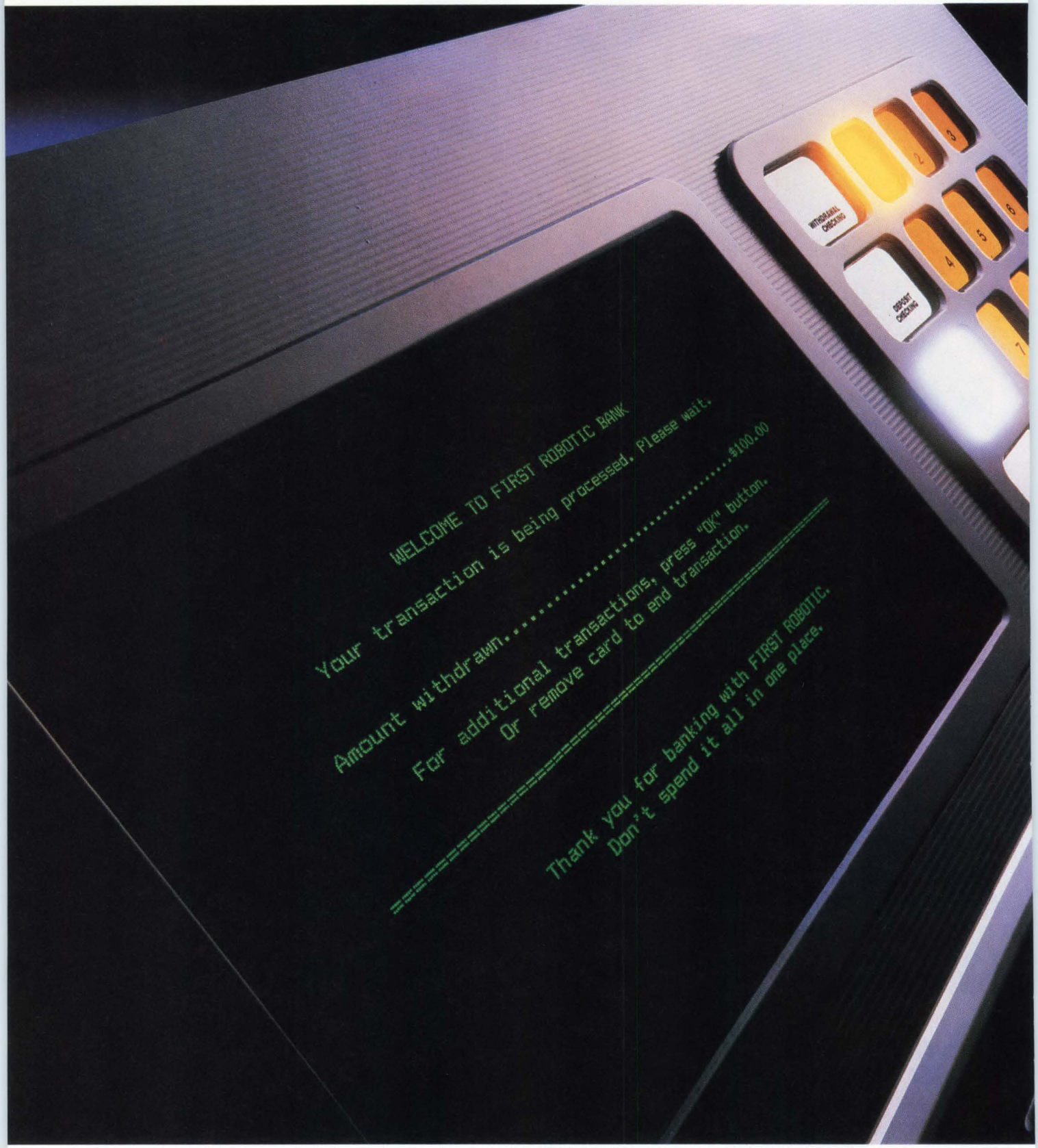

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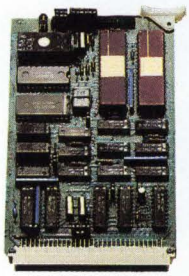

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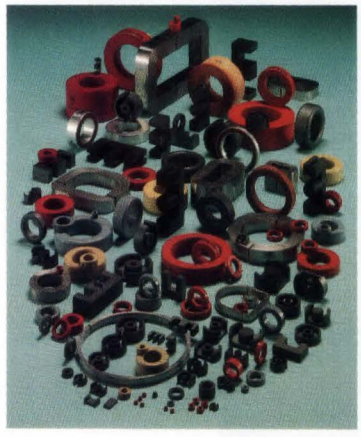

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Software tool generates test programs for GPIB in hours, not weeks

With little or no programming skill, designers can create and revise programs for bus-driven test equipment. An interactive menu tool does the trick.

Generating suitable test software for equipment sharing the General-Purpose Interface Bus (GPIB) has usually been time-consuming and difficult for the system engineer. Not too many engineers have mastered both hardware and software development. Add to this the problem of tailoring the software to the hardware (achieving universal compatibility), and the limited help of even the most promising automatic testing scheme becomes apparent.

A software development tool, however, lets the engineer with little or no programming skill create and easily revise complete test programs in only hours, rather than weeks or months, for a broad range of test instruments. Called Tek EZ-Test, the tool consists of two complementary programs in an interactive menu scheme.

The first program, the generator, creates an executable data base with the screen menus. The second program, the translator, retrieves the procedure data-base file created by the generator and converts it into a separate Basic file.

Steve Peterson, Tektronix Inc.

As manager of the Instrument Systems Integration Division's application software group at Tektronix, in Vancouver, Wash., Steve Peterson directed the design and development of Tek EZ-Test. Earlier, he also was in charge of software development for a series of IEEE-488 instruments and digitizers.

The composite test program handles the data logging and merging of test procedures.

Tek EZ-Test performs a series of discrete actions, or transactions, for each instrument setup and data-acquisition cycle. With the interactive screen menus, the user specifies up to nine operating variables for each transaction.

For the hardware description, he specifies the instrument type or model, the primary address, and the GPIB port number (for multiple-port systems). For the software portion, he includes the type of action (setup or data acquisition), failure limits for data acquisition, and two other timing parameters needed to acquire data over the bus and control the sequence of steps in the test. The designer then need only attach the required test instruments to the system controller and start the operating program.

Specifying the steps

The generator program, with its editing menu and user-definable keys on the computer keyboard, is used to define and modify the test procedure (Fig. 1). It affords options for creating and numbering each procedural step and for copying, inserting, deleting, altering, and listing any part of the step.

To generate a test setup, the user defines the step number and its type, of which there are five. They include those for completing a single instrument transaction; loop steps for single-

Test software generation

or dual-instrument stimulus or response transactions; and those for duplicating single or loop steps previously generated. Two other steps that are also useful include GOSUB, for specifying the beginning of a block of transaction steps in a subroutine, and RETURN, for defining the end of a block of transactions entered by a GOSUB statement.

Menus are accessible during program generation. The editing menu accesses the instrument selection menu, from which the user selects a test instrument for a transaction step (Fig. 2). The operating mode menu selects several transaction parameters, such as instrument messages, the pause between steps, and data acquisition from the instrument. These menus normally follow the selection of a single or loop transaction.

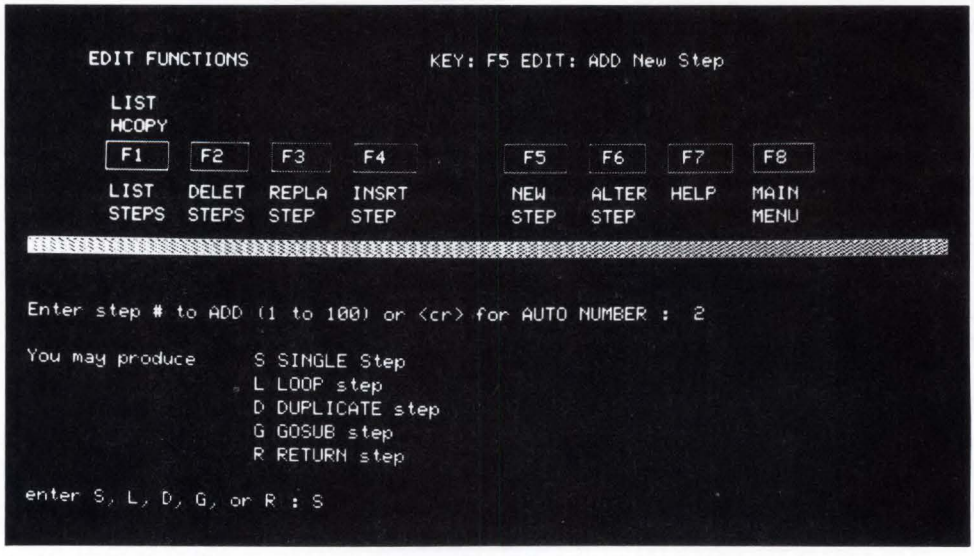
Once the instruments are selected, the user supplies the test sequence information along with the editing menu for that instrument. The test sequence may be as simple as moving to the next step in the procedure or as complex as jumping to a special battery of tests.

Options in the transaction step sequence include such standard software techniques as unconditional or conditional branching or looping.

Of particular interest to the user is the loop step, which merges stimulus setup and acquisition steps in one transaction. The driving signal (stimulus parameter) may be varied linearly or exponentially for each loop iteration. For easy analysis and graphing, stored acquisition data can be indexed to the stimulus values.

After completing the stimulus step specifications, the user may choose an instrument for the acquisition transaction and generate the rest of the step with the operating mode menu (Fig. 3). The user may request one instrument to generate the stimulus and another to acquire the response, or he can call on one instrument to perform both duties. The program then plots the output data vs the input (stimulus) signal, proving itself well-suited to plotting the frequency response of a module.

Any time after the basic operating specifications are defined, the user may execute the selected test procedure simply by invoking the test execution menu in the generator program. (Through it, the user may specify preliminary test information to instruct the system how to run the test.) The options provided by the test



1. Through the editing menu, the user can select five types of steps. In this case, step 2 of a multistep program is defined as a single-instrument transaction.

execution menu let the user run all or parts of the test sequence, step through the sequence for program debugging, and log all data or only failed data. Other options permit the plotting of data, step by step, and the graphic analysis of waveforms.

The user may employ the menu's interactive mode to override the test run if a step has failed its limits test. He may rerun the test, continue it, or abort it and return to any point in the menu.

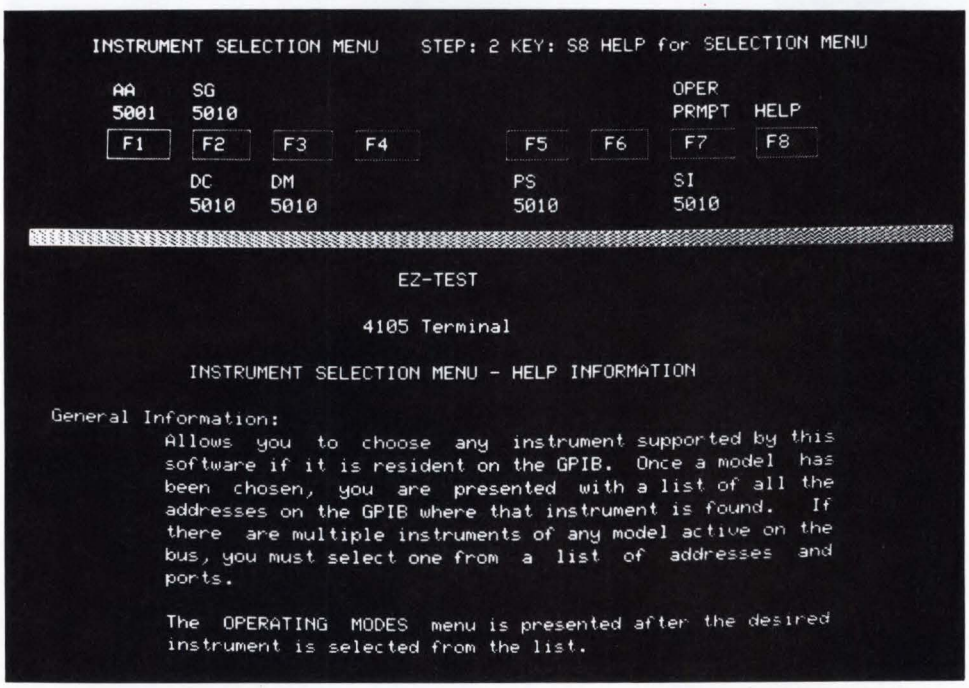
Many of the test procedures are modular in function and thus may be generated as one procedure. The test execution menu enables the user to link and execute several test procedures. Linked procedures run serially and permit the data to be logged into one data base.

After execution of each test, the acquired data can be stored in a file and displayed on a console or a line printer. The data is displayed in a table containing the user-defined test name, the step number, the stimulus values for each loop step, all acquired (output) data, the test delimiter, and indicators that denote whether a test has passed or failed.

The data base is easily modified with the editing menu, but accessing the data base in that way slows the execution of the program at run time. The translator can solve that execution problem by converting the test procedure's data base, with its instructions and test information, into an executable subprogram module.

The translator queries the user as to the file peripherals that should be used, the operator's ability to interact on failed measurements, the test procedures that should be included in the program, and the device that will serve as the operator console. Subsequently, the user enters the required parameters, and the translator automatically builds the executive and utility sections of the Basic object program. Then it sequentially translates the generator's procedure files (that is, the data base) into subprogram files. The user may then load these new programs into the system and run them to perform the tests.

To demonstrate the development tool's value, consider the testing of the audio portion of a circuit board for total harmonic distortion. The user must first define the test jig configuration for connecting the board to a programmable



2. During any step the designer may use the instrument selection menu to call one or more instruments on the GPIB—AA5001, DC5010, and so forth. Pressing the Help key brings up general information on using the development tool.

Test software generation

power supply and auxiliary equipment. In this case, an audio analyzer, signal generator, counter-timer, signal switcher, and digital multimeter are required.

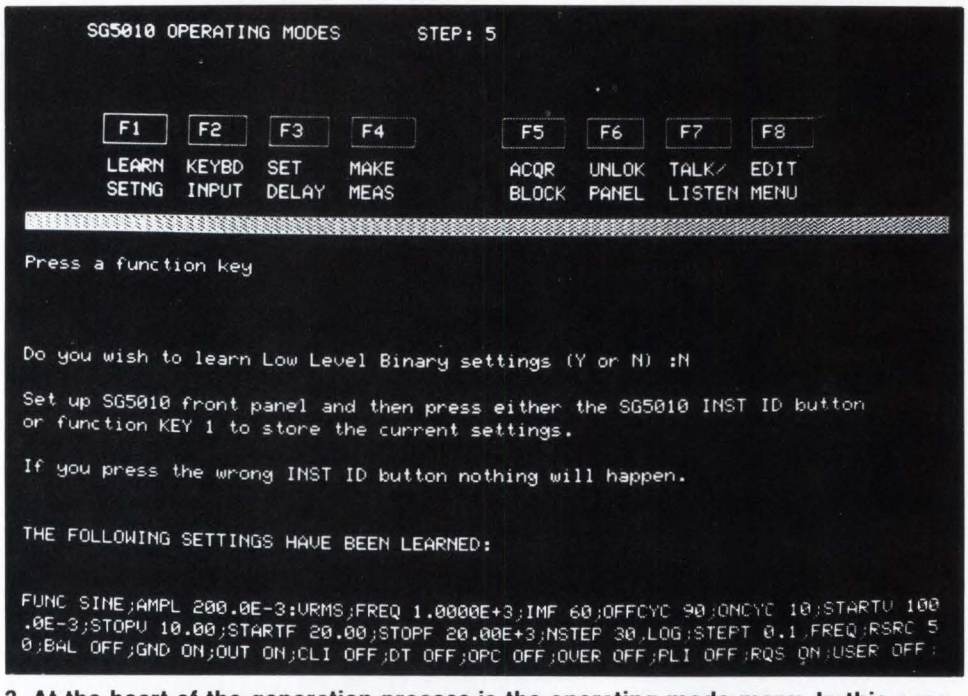
The next step

Next, a 32-step test procedure, which must be coordinated by the software, is mapped out (see "Taking the Steps to Amplifier Testing," opposite). Then the user starts generating the test by loading the generator tool and installing the test equipment at unique GPIB addresses in the test system.

When the user chooses to edit procedures through the generator's main menu, the test package indicates that it must configure the system, searching the GPIB port at every address to determine which instruments are available and which will respond to a request from the central processor. For instruments that do not respond, the system asks the user for an instrument identification string. Then the system displays the editing menu at the top of the screen, from which the user selects menu items (in this case, with a computer terminal keyboard).

The user generates the first step by pressing the NEW STEP key. The system then prompts the user to enter a step number or a carriage return to generate a number automatically. Now the user can decide which type of step to generate. If he chooses the single or loop step, the system will display the instrument selection menu. Only instruments in the development tool's predefined autoconfiguration list are presented to the user.

During the next phase of the test program, the operating mode menu appears, so that the user can set the instruments and specify appropriate action for various operating conditions. For a signal generator setup step, for instance, the user first manually sets the front-panel controls. Next he calls for the LEARN SETNG option to acquire the instrument's settings and to



3. At the heart of the generation process is the operating mode menu. In this case, an SG5010 signal generator has been selected and the LEARN SETNG **key has been pressed, leading the operator through several steps that culminate in storage of the generator's front-panel settings.**

display them on the screen; those settings become part of the procedure data base. The user can modify them through front panel and by instructing the systems to relearn them. If the user has selected an instrument from a manufacturer other than Tektronix, the program asks the user to enter an identification string so that the system can query the instrument for its settings.

Various alternatives exist for setting the instrument manually. For instance, the operating mode menu's Talk/Listen option can program the instrument through the terminal keyboard—an approach that is especially useful with signal scanners and other instruments that have no front-panel controls. It is also helpful with instrument setup commands that have no front-panel match.

Another way to learn settings is to use the Keybd input option to enter commands from the

Taking the steps to amplifier testing

Defining a complete test procedure is perhaps the most important task for the system designer working with the GPIB software tool, for it ultimately specifies the tool's entire programming task. In the case of determining an amplifier's response, the test procedure should indicate, in sequence, the software's duties for activating all test equipment, setting initial input signal levels, and providing input-signal and frequency-range increments. The 32 steps follow:

1. Disconnect the power supply from the device under test (DUT).
2. Disconnect the relay matrix from all instruments.
3. Give the operator instructions for connecting and setting the gain potentiometer.
4. Turn on the power supply and connect outputs to the test fixture.
5. Set up the signal generator.
6. Connect the relay from the signal generator and the ac voltmeter to the inputs of the device under test.
7. Measure the ac voltage of the input drive to the device under test.
8. Connect the relay from the ac voltmeter to the output of the device under test.
9. Measure the ac voltage of the output drive.
10. Give the operator instructions for setting the gain potentiometer.
11. Measure the ac voltage of the output drive, with the gain potentiometer set totally clockwise.
12. Disconnect the signal generator from the input of the device under test.
13. Measure the output noise ac voltage with no input signal.
14. Connect the signal generator to the input of the device under test.
15. Set up the ac voltmeter for reading dBm.
16. Prompt the operator to set the gain potentiometer to 10 dB (as seen on the ac voltmeter).
17. Measure the ac gain to 10 dB, ±0.2 dB, with a loop to step 16 until the gain is properly adjusted.
18. Perform the frequency response loop step and increment the stimulus frequency from 10 Hz to 100 kHz, with five steps per decade of exponential sweep and a gain measurement in decibels at each frequency.
19. Set the signal generator to −50 dBm output at 1 kHz.
20. Set the audio analyzer to measure total harmonic distortion (THD).
21. Perform the loop step for level vs harmonic distortion, using the signal generator for stimulus and the audio analyzer for acquisition; increment the input drive level from 15 dBm to −65 dBm in steps of −2.5 dBm; acquire the settled output THD reading at each level of input drive.
22. Set the signal generator for 0-dBm output.
23. Perform the loop step for frequency vs THD, using the signal generator for stimulus and the audio analyzer for acquisition; decrement the frequency from 100 kHz to 10 Hz in five steps per decade, using an exponential sweep; acquire a settled THD reading at each frequency.
24. Set the signal generator to a 10-kHz, 0-dBm square wave that drives the input of the device under test.
25. Connect the relay from the counter to the output and disconnect the audio analyzer.
26. Set the counter for automatic rise-time measurements; acquire a positive step response from the output of the device under test, measured at amplitude levels of 10% and 90%.
27. Set the counter for peak-to-peak level measurements; acquire an autotrigger measurement of the peak-to-peak voltage of the device under test's output signal.
28. Connect the digital multimeter to the output of the test device; disconnect the counter.
29. Set the digital multimeter to dc volts and acquire the dc level of the output of the test device.
30. Open all switch matrix relays so that devices are disconnected from the device under test.
31. Set the power-supply voltages to zero and disconnect outputs.
32. Print a list of test results.

terminal keyboard in the form of ASCII characters. The development tool transmits the settings to the instrument and performs a test sequence that verifies those settings. In so doing, it waits for a service request and error report from that instrument. For non-Tektronix instruments, the user must verify front-panel settings manually.

Other operating modes work with parameters like SET DELAY, which programs a pause between steps, and UNLOK PANEL, which sets the instruments to the local mode at run time. The local mode is frequently needed to make adjustments on a measuring device.

Single-point data acquisitions are handled through the MAKE MEAS option, which comes in handy for digital voltmeters, counters, and digital processing scopes, assuming that the last send data samples as a single ANSI-formatted floating-point number. The user must specify the limits, the measurement label, and the time-out parameters.

For logging large blocks of data, such as those sent from waveform digitizers, spectrum analyzers, and logic analyzers, another option acquires data blocks as large as 10 kbytes in one transaction step.

Verifying the results

When all the initial parameters have been defined, the user may invoke the editing menu's list steps to check the parameters and data for any step. For instance, the listing of the acquisition and frequency-loop operations of step 21 uses the signal generator and the audio analyzer (Fig. 4).

At any point as the 32-step program is being generated, the user can select options in the test execution menu to verify settling times or any other item of interest. In this case, only six hours elapsed in designing the test approach, generating the procedure, verifying it, and ob-

```
# 21          LOOP STIMULUS

SIGNAL GENERATOR -- ID SG5010  PORT 0  ADDRESS 10

DEVICE SETUP - NO MEASUREMENT
                            TIME DELAY: 0                PANEL MODE: LOCKOUT


PARAMETER: "freq"     UNITS: ""

INCREMENT : 10.000000 to 1.0E+5 for 21.000000 iterations.

                  -   -   -   LOOP ACQUISITION   -   -   -

         Freq Resp.

DISTORTION ANALYZER -- ID AA5001  PORT 0  ADDRESS 28

MEASUREMENT

ACQUISITION TIMEOUT:   10

MEASUREMENT UNITS:  dBm       TIME DELAY: 0                PANEL MODE: LOCKOUT


Branch to : Next Step
```

4. A listing is available for all or part of any procedure created by the generator program. In this case, the loop step is specified for measuring the amplifier's harmonic distortion vs the input level.

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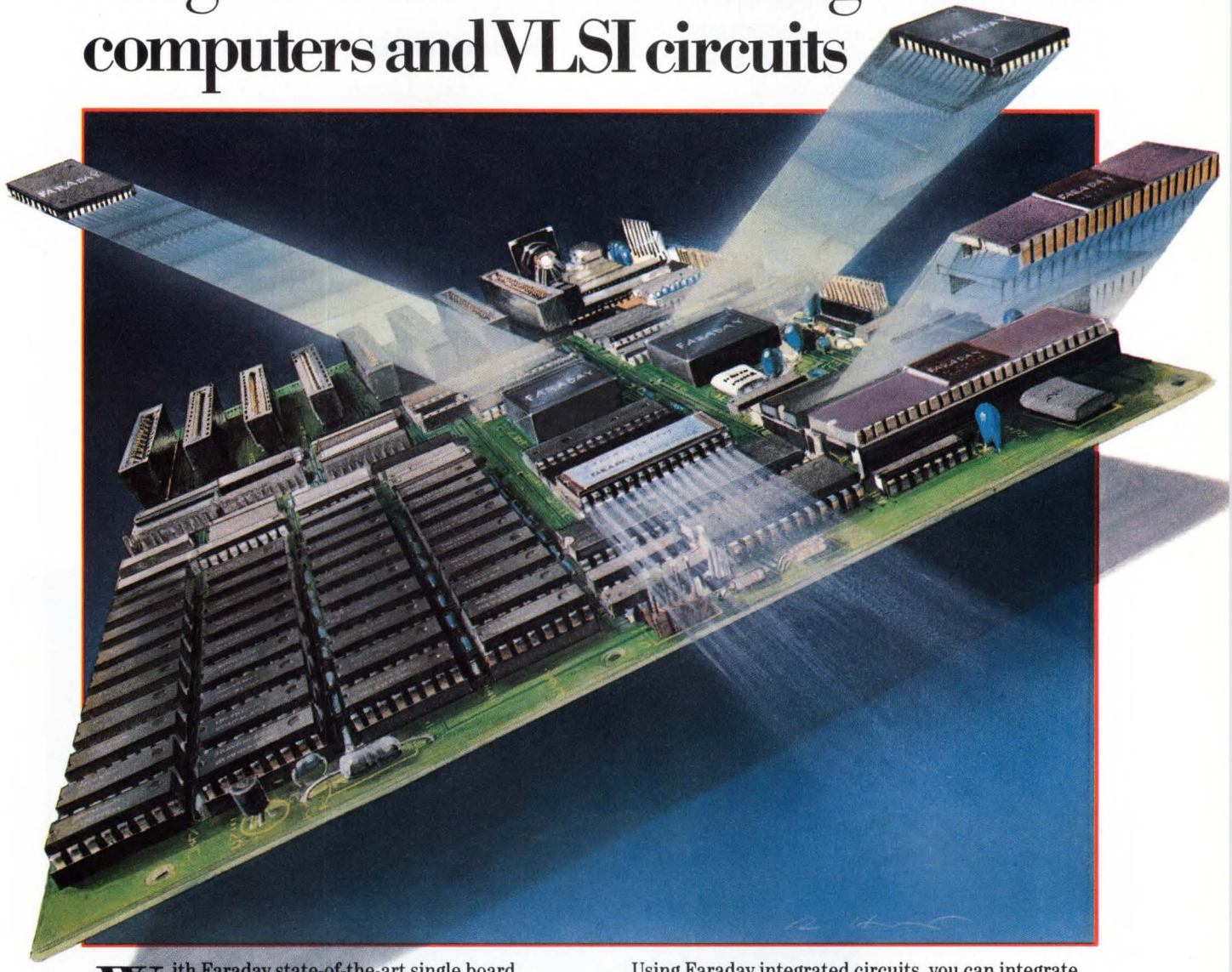

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After verifying any procedure, the user can reenter the main menu and choose the SAVE PROCD option to store the procedure on a disk. The translator program can then be loaded from the disk and run. The user's response to a series of prompts determines which peripherals will be used and which generator program procedure files will be translated.

The translation process requires 7 minutes, with most of that time spent answering prompts and queries. The volume of Basic code that is produced includes the run-time executive, data-logging utilities, instrument drivers, and the subprogram for the procedure itself. The 32-step procedure needs 1209 lines—546 for the executive and utility parts and 663 for the procedure subprograms. The translated program resides in three files: the executive, a data file containing console parameters, and the procedure subprograms.

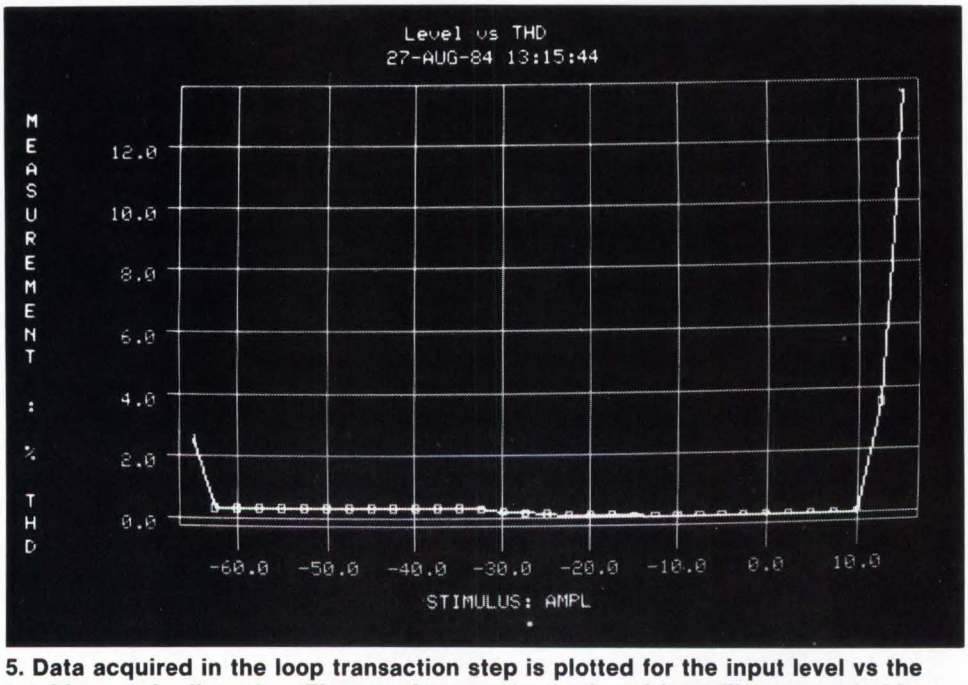
The user executes the program by running the executive file first. It reads the console parameter file and then appends the procedure subprograms. When the last subprogram is appended, the executive prompts the user for new information for the device under test and for the name of the data log file. Next the executive portion executes the procedure subprogram. Every pass produces a new file of logged information.

Translation pluses

Translated programs have several advantages over the generator-produced procedures: They carry fewer lines of code, execute two to five times faster, and are more easily enhanced. The last is a decided advantage when special algorithms must be created.

Test data stored on a disk or tape can be retrieved with the utility program's loop plot (Fig. 5). The data is normally transferred to the terminal screen, but can just as easily be sent to the printer port or placed in another data file.□

How useful?	Circle
Immediate design application	544
Within the next year	545
Not applicable	546



5. Data acquired in the loop transaction step is plotted for the input level vs the total harmonic distortion. The raw data can be retrieved from files created either by the generator program or by the Basic programs that the translator produces.

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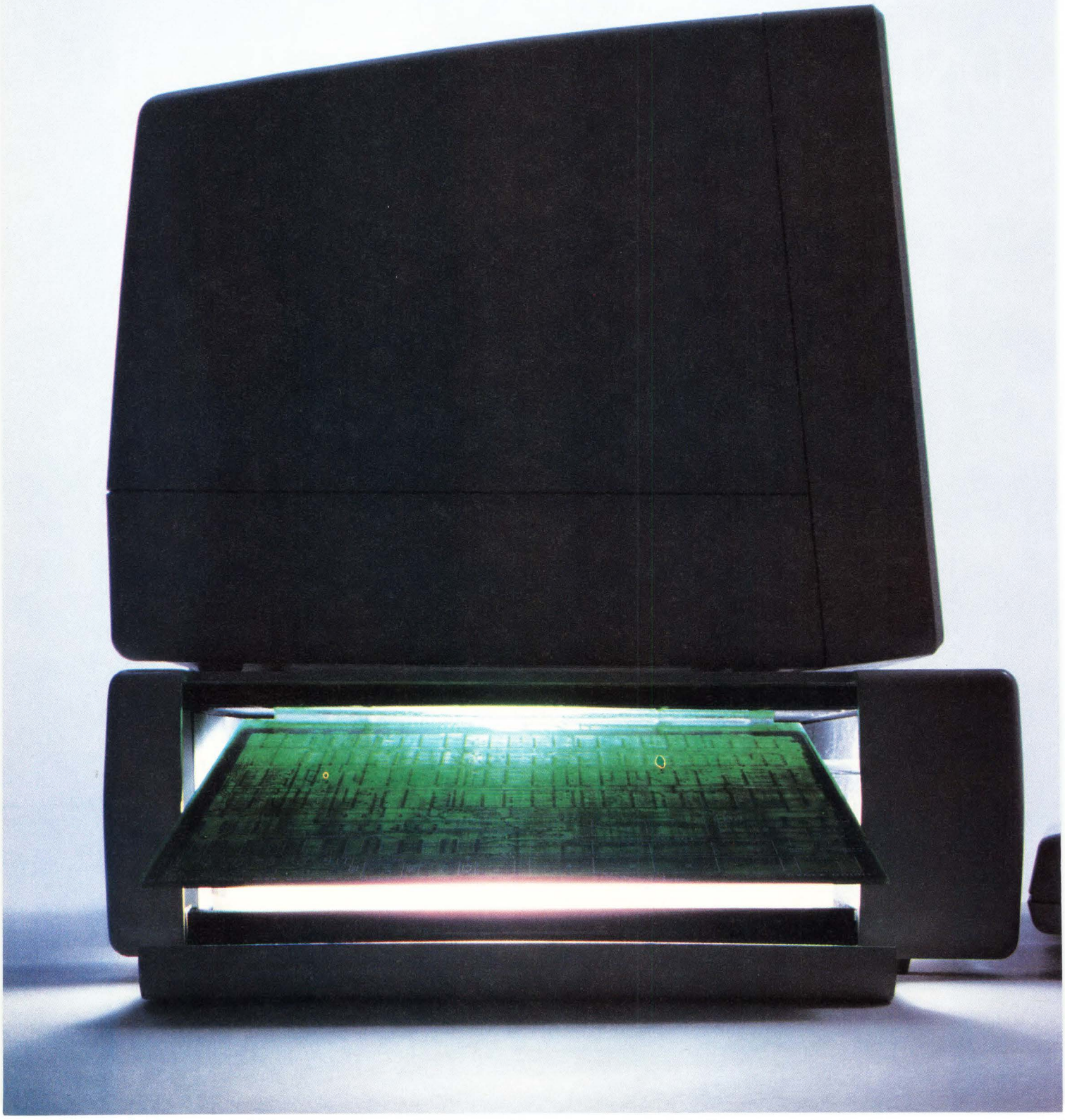

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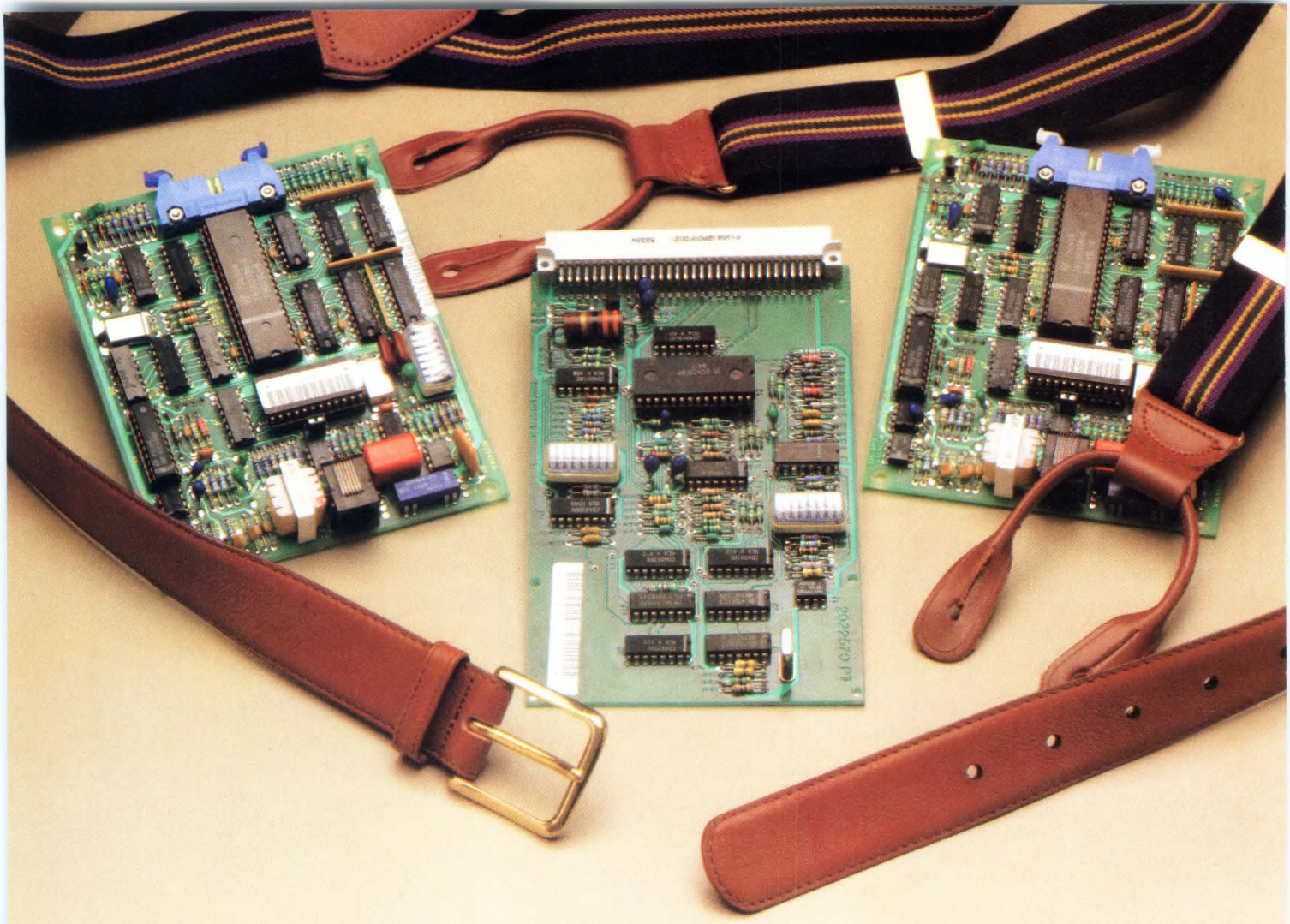

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CIRCLE 87

Workstation scores high on programmability, speed, and power

Simple support software, tightly coupled to hardware op codes, speeds the job of programming a VAX-like system with a brilliant display.

For the first time, a computer graphics workstation can combine brilliant, high resolution with tens of millions of colors and the computing power and speed required for designing large, complex ICs or even for modeling solid objects.

Three-dimensional modeling, especially with color and shading, is a computationally intensive task. The X, Y, and Z coordinates of each point defining a solid object must be translated into a two-dimensional plane of picture elements, each of which varies in color and light intensity with its purported distance from the viewer and with its position in relation to all other pixels.

As the hardware basis for such capabilities, an interactive graphics computer station—SaberStation for short—equips the application programmer with more than enough processing power for the job. Based on a National Semiconductor 32-bit chip set and running at 10 MHz under the BSD Unix operating system, the unit puts the performance of a VAX-like minicomputer on an engineer's desk. Its architecture, which employs a floating-point coprocessor and ultrafast, 32-bit-wide DMA channels, executes 1.2 million instructions a second.

More than matching that computational power is a 1200-line 19-in. CRT display that is refreshed in its entirety 60 times a second—that is, it has a 60-Hz noninterlaced refresh rate. The array of 1664 by 1248 pixels lets the user create perfect circles and slanted lines without the usual stairstep effect or the need for corrective techniques such as antialiasing. And the pixels owe their brilliance, as well as their switching speed, to a specially developed video amplifier technology, which can turn each of them on and off within 6 ns (see "Harnessing Q-SEL Technology," p. 190).

While delivering dazzling resolution, the workstation hardware does not require the application programmer to map each and every one of the more than 2 million pixels. A choice of two graphics interface software packages—one using the graphics primitives of SaberCore (based on Siggraph) and the other using those of the Graphical Kernel System—greatly simplifies graphics programming. What's more, it

Carl Held, Kevin Anderson, and **Larry Dorie**
Saber Technology Corp.

Currently software support manager at Saber Technology, Carl Held has over 20 years' experience in mainframe and minicomputer software. He holds a BS in mathematics from California Polytechnic and an MA in philosophy from San Jose State University.

Kevin Anderson, who is vice president of software development at the San Jose, Calif. company, has an MS in computer sciences from UCLA. He has been working with operating systems for over 12 years.

Larry Dorie, Saber's vice president of marketing and sales, held the same title on his last job, at Evera Co. His BSEE is from Carnegie-Mellon and his MBA is from California State University at Hayward.

eases the porting to the station of existing GKS- or Siggraph-based application packages, such as programs for laying out ICs or doing 3D modeling.

The graphics primitives are precoded subroutines that serve as a shorthand for creating graphics images, colors, and shading. They produce display lists that feed into the Virtual Device Interface. If necessary, however, the application programmer can work a stage closer to the workstation hardware, using the interface to hook into device drivers. On the SaberStation, all of the devices controlled by the software drivers are hardware versions of graphics op codes, some 120 in all. This graphics op code structure (GOPS) provides a higher basic level of functionality in hardware than does the conventional raster op code format.

Harnessing Q-SEL technology

The Quasi-Saturated Emitter Logic (Q-SEL), a proprietary circuit, is responsible for the sharp, clear pixels available on Saber's video display monitor. Because of Q-SEL technology, the video deflection amplifiers can drive more than 2 million pixels up and down over a 40-V range 60 times a second.

In essence, Q-SEL reduces Miller capacitance, which limits amplifier speed, by using very fast transistors biased to near-saturation and connected in a common emitter configuration. Biased in this manner, the transistors dissipate little power and can still produce a highly linear waveform. And because they also present an extremely low capacitance to the high-voltage transistors driving them (see the figure), the Q-SEL output transistors are capable of slewing at more than 20,000 V/μs. In addition, the Q-SEL circuit can tolerate up to 2000 V across its output, with an on-resistance of less than 1 Ω.

In the context of a 1200-line video monitor, the video deflection amplifier can slew more than 40 V within 2 ns—well within the 5.5 ns per pixel required for the resolution of 1664 by 1248 pixels. The Q-SEL circuit effectively tracks ECL logic when it is swinging 40 V and the ECL logic is swinging 1 V. Without the speed capability, the picture would appear dim and fuzzy, and the high resolution would be lost.

The workstation consists of three main subsystems—one each for applications, graphics, and images—linked to each other by high-speed buses (Fig. 1). The application subsystem includes a 32-bit 32032 processor plus a floating-point coprocessor, both backed by 1 to 12 Mbytes of RAM organized as a 16-Mbyte virtual memory space. The unit is supported by two 40-Mbyte disk drives, one for system control programs and the other for application software, and a streaming-tape cartridge for backup. Each of those peripherals includes an 8-kbyte FIFO buffer, as does the system's Ethernet controller. An RS-232-C controller and two parallel I/O channels have one such buffer, which they use in rotation for fast transfers to main memory.

The DMA controller

Inside the application subsystem is a DMA controller, which has eight dynamically relocatable channels with variable burst lengths, eight assignable priorities, and a 20-Mbyte/s transfer rate. The DMA controller links up with each of the other two subsystems. With its aid, the application subsystem can write or read any pixel in image memory and the graphics subsystem can access an image directly from disk.

The graphics subsystem translates application data into Core or GKS primitives, which are in fact calls to the Virtual Display Interface. It also performs such standard graphics functions as scalable text generation from a software-alterable font, bit alignment for image memory, and basic vector drawing. In addition, the subsystem can accommodate dedicated hardware accelerators, which speed up the jobs of filling polygons, transforming matrixes, processing arrays, generating meshes and tiles, and doing vector-to-raster conversion.

The image subsystem consists of image memory, for holding images and their updates, and a control unit. The memory can be controlled and organized in a variety of ways, including double buffering and layering. The first of these makes it possible to display some memory planes while manipulating others and to switch instantaneously between displaying those just manipulated and manipulating those just displayed. The second permits operations to be performed on two planes—for instance,

the logical ANDing of two IC metallization layers are displayed in different colors, so that their overlapping areas are highlighted in a third color.

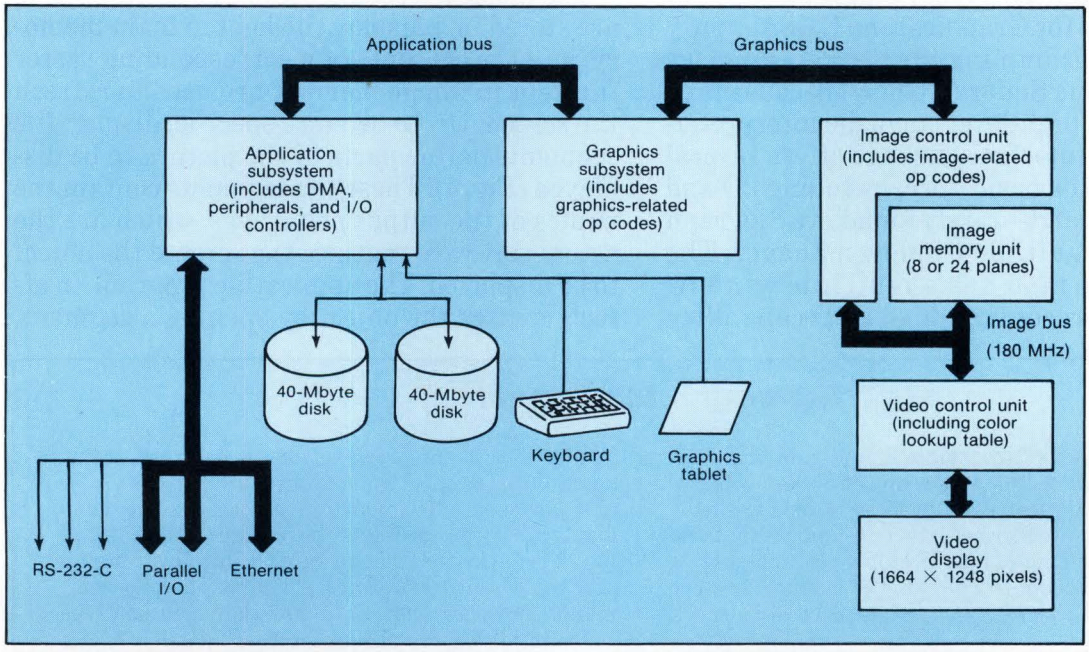
The basic image memory has up to 8 memory planes, for eight levels of gray scale, but is expandable to 24 planes, for red, blue, and green. Handling the 16 million hues yielded by 24 planes takes 6 Mbytes of memory and is perhaps used only for the most exotic graphics applications. Under ordinary circumstances, an adequate number of colors can be generated by the image control unit from a fast color lookup table situated in the video control unit.

The video control unit consists of 100K ECL components, to give it the speed to drive the video display bus at 180 MHz. That rate is essential to cope with both a 24-plane, 1664-by-1248-pixel image and pixels that may switch both on and off within 6 ns.

In operation, the DMA controller sends a block of information from the application subsystem—or even directly from disk storage—over the application bus to the graphics subsystem. That unit uses table lookup to change the real-world coordinates of the application program into graphics primitives, which call up the VDI in order to summon specific drivers for specific graphics op codes.

The graphics subsystem then passes the information to the image controller, which checks the image data and instructions for valid op codes and data structures. In the absence of a dedicated accelerator, it tackles vector-to-raster conversion. Then it groups the bits in the data stream into complete image planes before sending them across the image bus to the image memory. Finally, the memory transfers the data to the video controller, which in turn processes it through its color lookup table for presentation on the video display.

With a dedicated add-on hardware accelerator—for example, a Weitek matrix transformation processor or a polyline fill board—



1. The Saber graphics workstation includes three processing elements. An application subsystem handles I/O graphics functions and transfers application-specific screen descriptions to the graphics processor. The graphics subsystem converts these screen descriptions—using Siggraph or GKS Core primitives—into a series of display vectors, and the image processor loads the serialized image into the high-resolution display.

images are generated up to 100 times faster. The accelerator derives more complex graphics op codes from the workstation's set of 120 or so, thus using fewer of them and so increasing speed. Apart from the higher speed, the accelerator is transparent to the user.

While the hardware of the Saber graphics system has been designed to perform a computationally intensive display task, the job of actually putting the system to work belongs to the application programmer. Software packages available for the workstation are, in fact, designed to aid the programmer in transporting existing CAE/CAD software to the system or in creating new graphics application packages. These support packages include not only the Unix operating system but also C, Pascal, and Fortran-77 compilers; a library of editors, assemblers, and utilities; and, of course, the choice of two graphics interface packages.

The graphics core

The core primitives from Siggraph (Special Interest Group for Graphics) and GKS simplify the job of programming the workstation (see "Drawing a Blue Square," below) because they function like a high-level language interpreter. The Siggraph interface package offers several extensions to the basic Core, including 2D and 3D translators and—rarely found in a Siggraph structure—a multiple window manager. The GKS package also has a multiple window manager and recently added a 3D capability (ELECTRONIC DESIGN, Nov. 15, p. 47). In both, the window manager serves as the main bridge between the graphics primitives and the Virtual Device Interface software, clipping and scaling the data for viewing in each window displayed on the screen (Fig. 2).

The typical graphics application package defines an object to be displayed in terms of world coordinates (where the world is the entire picture described by the application). Before the image can be displayed, the data must be translated by a scanning or viewing operation into terms that the display device (in this case, the CRT screen) can interpret.

Scanning, which is performed by the graphics core system, can view the object in two or three dimensions, in either a perspective or parallel projection. It specifies how much of the world coordinate space is to be visible and defines a mathematical transformation between the object's world coordinates and those of the display screen (Fig. 3).

The display screen coordinates of the objects are stored in a display file kept in main memory, and the contents of a corresponding raster file kept in image memory are used to refresh the screen. Or, to be more specific, display file segments define parts of the picture to be displayed (Fig. 4). These file segments contain the names of the output primitives, which are the actual software routines that create the object to be displayed. The application program, in effect, creates the object by opening a segment,

Drawing a blue square

The application programmer will find that manipulating colors and images on the SaberStation is a fairly straightforward process. Any high-level language can access the Siggraph and Virtual Device Interface commands. If he wishes to display a blue square in one corner of the screen, he need merely enter the following lines of code in the C language:

```
1   C Open workstation
2     Call VOPNWK (workin, Devhan, workot)
3     Call VSCOLR (Devhan, 1, 0, 1000, 0)
4     Call VSECOL (Devhan, 1, workot)
5          Workot (1) = 0
6          (2) = 0
7          (3) = 20000
8          (4) = 20000
9     Call VBAR (Devhan, workot)
10    Call VCLSWK (Devhan)
```

Line 1 tells the workstation to enter the commands for graphics. Line 2 opens (accesses) a specific device handler, which in this case is the video display driver. Line 3 sets the background color and line 4 sets the foreground color. Lines 5 through 8 activate the workstation's graphics op code commands and access the data file; they also hold the information on the size and screen location of the square, such as the X-Y coordinates and the pixel positions.

Line 9 actually draws a vertical line, using the parameters given in the data file. Line 10 closes the workstation activity and shifts the action to the graphics subsystem.

When the code is processed, a bright blue square will appear on the screen.

calling out the primitives named within it, and then closing the segment.

The programmer can also specify logical input devices, which are hardware-independent. The graphics core system maps these input devices to the actual physical devices (a mouse, stylus, or joystick, for example).

Digging deeper

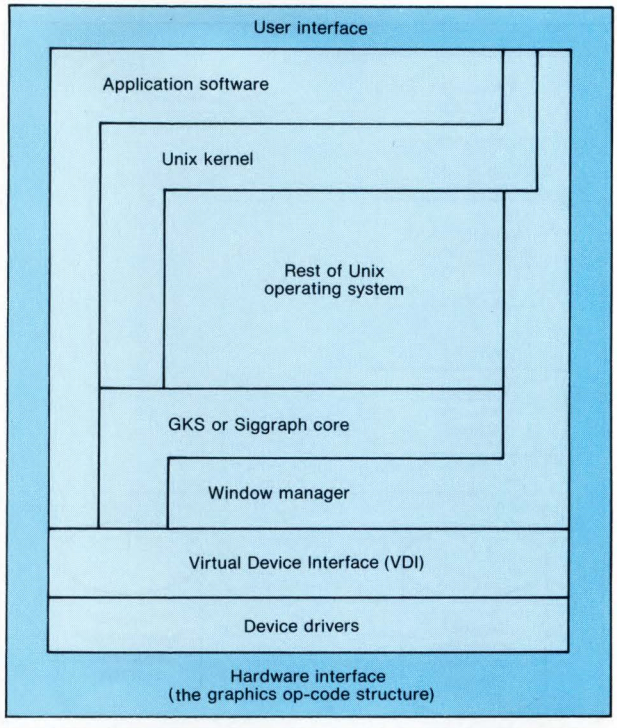
Despite the power of the GKS or Siggraph approach, the programmer who works directly with the VDI can achieve a significant improvement in performance, thanks to the close association between the interface and the graphics hardware. He or she can use any high-level language to describe VDI subroutines, which call up software drivers for the graphics op codes, which are stored in ROM.

The following Virtual Device Interface calls, written in C, will cause the system to read in the microcode streams that activate the display:

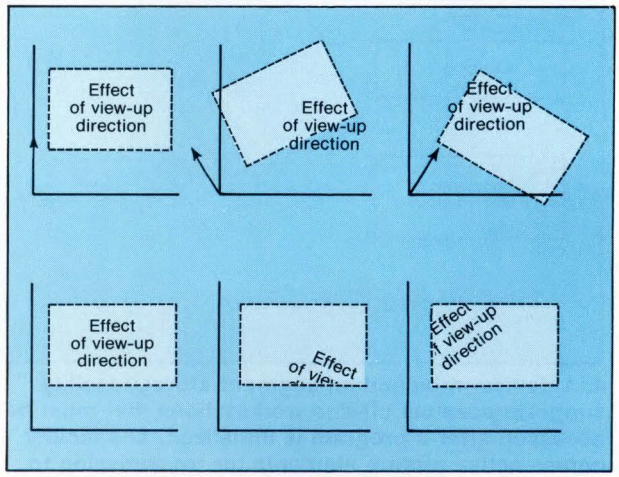
```
(Set color representation:)
Call VQ__color(dev_handler, ind_in,
  ind_out, RGB)
(Set fill color:)
Call VSF__color(dev_handler, ind_in,
  ind_out, RGB)
(Set interior style)
Call VSF__INTERIOR(dev_
  handler,style_in,style_out)
```

Alternatively, the programmer can descend below the interface to the drivers that control the graphics op codes. As an example of GOP utility, the typical software algorithm for a polyline fill breaks the polygon into rectangles and then fills each one. A simple sequence of graphics op codes is used to fill a polygon (in hexadecimal notation):

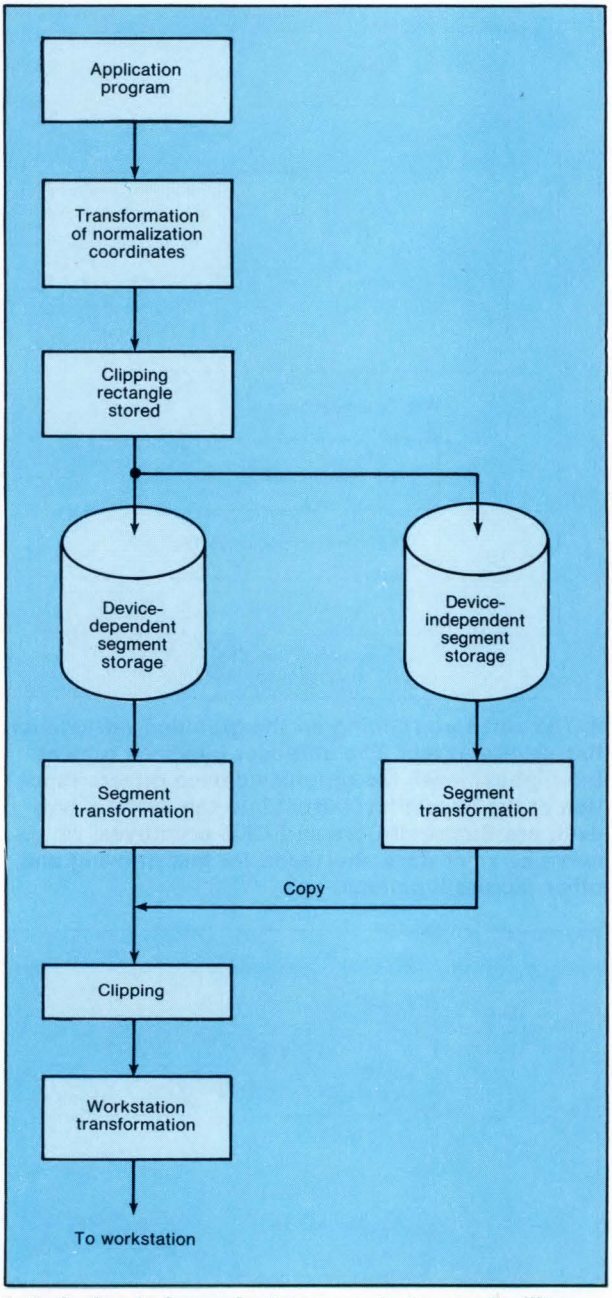
GOP	
1B	Set ICK register
12	Set right mask
20	Set and modify A register
FFFF	(Data for A register)
1A	Set foreground color
10	Set background color
19	Set height in lines
18	Set length in pixels
14	Set X starting location
15	Set Y starting location
43	Draw the rectangle



2. The software running on the graphics workstation has several levels. The end-user interface runs at the highest level; the graphics device drivers function at the lowest level. Built into the system, however, are Siggraph Core and GKS primitives, which serve as a software shorthand for line drawing and other picture functions.



3. The two-dimensional Core viewing operation provides a window that corresponds to the global world coordinate system. The screen or viewport is the display device's physical output. By moving the global window, as indicated above, it is possible to make different portions of the global space appear in the viewport.



4. A device-independent segment-storage facility supports possible off-line workstations that must be accessed after a program is initialized. The facility copies active picture elements for transmission to any device needing updating.

Each rectangle in the set will then be drawn automatically.

Other graphics op codes can perform more than one operation in a single command. For example, MOVE Plane to Planes reads from a read-enable plane, passes the data through an ALU for optional logic functions, and writes the resultant data into the selected planes at the selected addresses. In other words, it copies a set of pixels and changes their positions and their values, all in one go.

Porting an editor

To illustrate how efficiently an application program can be ported to the graphics workstation hardware through the Virtual Device Interface, an interactive color graphics editor, called KIC and developed at the University of California at Berkeley, was brought into the system. The job took less than one man-week, and the editor, which helps design masks for IC, proved visibly more responsive than when ported to workstations that lacked as tight a software-hardware interface.

KIC's porthole, or entry point, to the graphics workstation is a group of routines, called model frame buffer routines, each of which had to call the appropriate Virtual Device Interface routines. Beyond that, it was also necessary to initialize the list of frame buffer descriptors, which describe the hardware on which the editor has to run, and to set up a scroll function. KIC model frame buffer routines begin with FB, while calls to the interface routines begin with v_ (Table 1).

KIC is initialized with the call FBegin, which assigns workstation-specific values to a list of model frame buffer descriptors (Table 2) and then calls FBInitialize. In FBInitialize, the program actually opens the workstation with a Virtual Device Interface call, v-opnwk. Subsequently, FBTransfer, FBHalt and FBEnd call a single interface routine and return.

KIC uses two types of lines. FBLine assigns X-Y coordinates for each of two points in the array and calls v_pline. FBDrawLineTo does that too, but the first point is set by FBMove.

FBBox is slightly more complicated. KIC sends additional parameters of a color number, saying, "Put this in the background color or put this in the color I sent you" and "Either fill this

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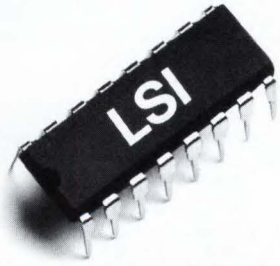

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CIRCLE 88

box or make it hollow." The first two are handled with a call to FBForeground (discussed below). If the choice was fil, a call to v_bar is made. Otherwise a box is drawn using FBLine. FBPolygon is like FBBox except that the interface call is to v_fillarea instead of v_bar.

KIC uses two coordinate systems to display text: row and column, and pixel coordinates. The first parameter in the call FBText indicates which of these coordinate system modes to use. Since v_gtext expects pixel coordinates, rows and columns are converted into them thus:

```
if (Mode == Row__Column)
(
  i = FB.fMaxY − RowOrX *
    FB.fFontHeight;
  RowOrX = (ColumnOrY − 1) *
    FB.fFontWidth;
  ColumnOrY = i;
)
```

where FB.fmaxY, FB.fFontHeight, and FB.fFontWidth were set above in FBBegin. The buffer is flushed after FBText with v_updwk. FBFlood erases the screen with v_clrwk(device).

To set a color number to a red-green-blue value, KIC uses the FBVLT call. This call has to multiply each of the RGB values by 1000 and then divide it by 999 because the Virtual Device Interface expects RGB to be between 0 and 999; only then can an interface call be made to vs_color. The KIC editor sets color numbers for primitives as either display or erase, whereas the Virtual Device Interface sets line color, fill color, and text color separately. KIC's FBForeground therefore has to call vsl_color, vsf_color, and vst_color to the color number sent as a parameter.

KIC's style identification numbers for solid fill and for hollow are the reverse of those in the Virtual Device Interface. So the first job of FBSetFillPattern is to reverse these. The next is to set the fill style using vsf_interior.

The first input routine, FBKeyboard, expects KIC to send it a pointer to a pointer in the i input buffer Type_In. The text color is then set to the color number that KIC has inserted in the variable Parameters.kpMenuTextColor and makes a call to FBForeground. The pixel location at which the keyboard input will be echoed is

Table 1. KIC editor's model frame buffer and the corresponding Virtual Device Interface routines

Control routines	
FBTransfer( )	v_updwk(device)
FBBegin(Display)	none
FBInitialize( )	v_opnwk(inarray,device,outarray)
FBHalt( ) and FBEnd	v_clswk(device)
Output routines	
FBMoveTo(X1,Y1)	none
FBDrawLineTo(X2,Y2)	v_pline(device,count,xyarray)
FBLine(X1,Y1,X2,Y2)	v_pline(device,count,xyarray)
FBBox(column,Erase?,type, style,X1,Y1,X2,Y2)	v_bar(device,xyarray)
FBFlood( )	v_clrwk(device)
FBPolygon(column,type,style, xyarray,count)	v_fillarea(device,count,xyarray)
FBText(Mode,RowOrx,ColumnOry, Text)	v_gtext(device,x,y,text) v_updwk(device)
Attribute routines	
FBVLT(ColorId,Red,Green,Blue)	vs_color(device,column,rgbin,rgbout)
FBForeground(Erase?,column)	vsl_color(device,column) vsf_color(device,column) vst_color(device,column)
FBSetFillPattern(style)	vsf_interior(device,curstyle)
Input routines	
FBKeyboard(String)	vrq_string(device,maxlen,mode, echo_xy,string)
FBPoint(X,Y,Key,Buttons)	vrq_locator(device,xy_in,ink,rband, echo_handle,xy_out,term)
Utilities	
FBPolygonClip(coord,n, window)	none
FBMore(X1,Y1,X2,Y2, Textfile)	vrq_string(device,maxlen,mode, echo_xy,string)

Table 2: One of the KIC editor's frame buffer descriptor lists

```
FB.fDisplay = Display;
FB.fMaxIntensity = 255;
FB.fButtons = True;
FB.fNumButtons = 4;
FB.fMaxX = 32767;
FB.fMaxY = 24575;
FB.fMaxP = 255;
FB.fNumColors = 126;
FB.fFontWidth = 480;
FB.fFontHeight = 720;
FB.fNumRows = FB.fMaxY/FB.fFontHeight;
FB.fNumColumns = FB.fMaxX/FB.fFontWidth;
FB.fLastCursorColumn = 74;
FB.fFilled Polygons = True;
FB.fDefinableFillPatterns = True;
FB.fNonDestructiveText = False;
buttonmask[0] = 1;
buttonmask[1] = 2;
buttonmask[2] = 3;
buttonmask[3] = 4;
FB.fButtonMask = buttonmask;
```

described as follows:

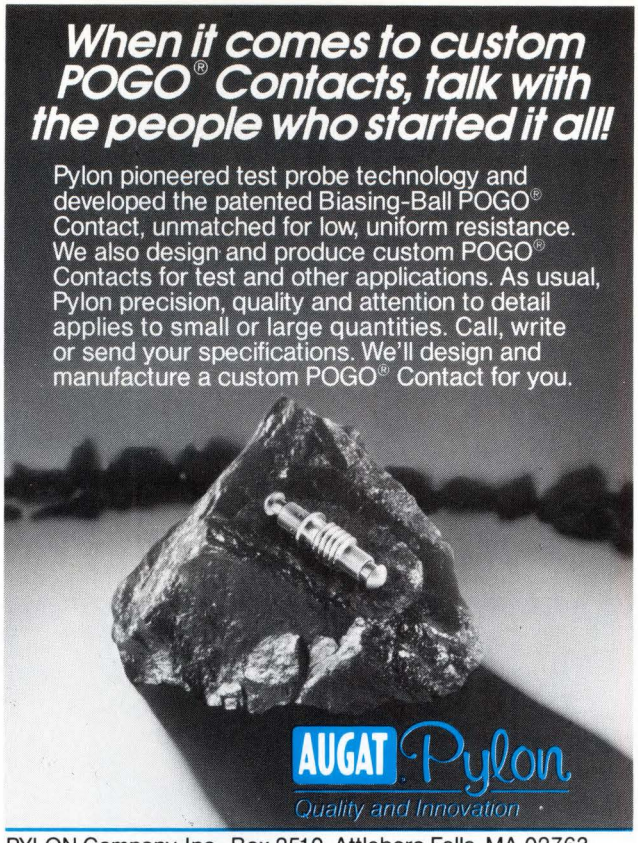
```
Y = FB.fMaxY
    -(FB.fNumRows-Parameters.
    kpNumLayerMenuRows - 1)*
    FB.fFontHeight;

X = FB.fLastCursorColumn*
    FB.fFontWidth;
```

Then an FBKeyboard(String) call is made to vrq_string, which waits for keyboard input and a carriage return. The address of the local input buffer is returned to KIC via the pointer mentioned above. The second input routine, FBPoint, expects KIC to send pointers to variables to hold the X-Y coordinates of a stylus event, the button number, or the key that was returned by a locator. The interface call vrq_locator fills those variables.

The utilities can be taken from fb.c, a sample model frame buffer. FBMore reads a file into a window on the screen and scrolls to the next page when it receives a character from the keyboard. A call to vrq_string may be used to accept the character. The KIC editor has its own window manager and its own polygon clipping (FBPolygonClip). When an application handles its own higher graphics functions, and most major applications do, it is much more efficient for them to access the drivers directly.□

How useful?	Circle
Immediate design application	550
Within the next year	551
Not applicable	552



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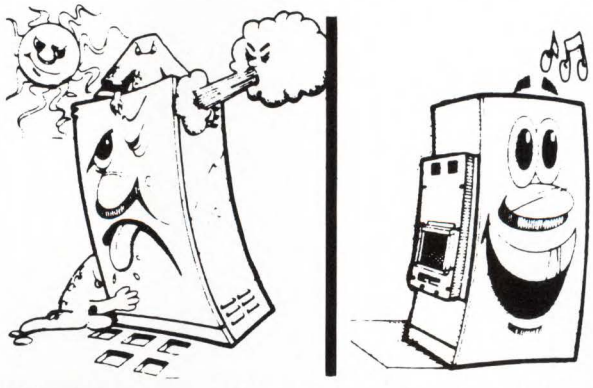

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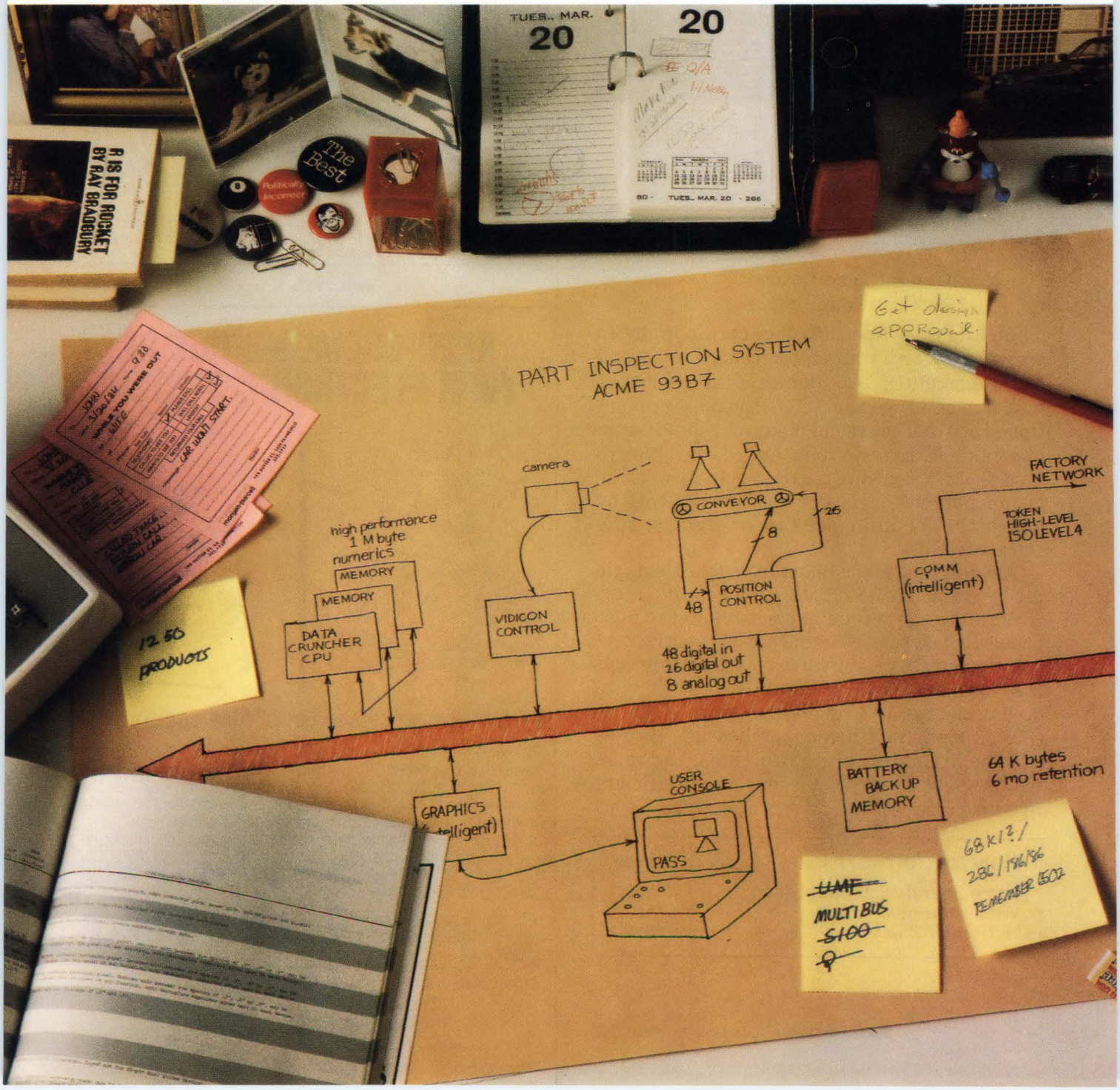

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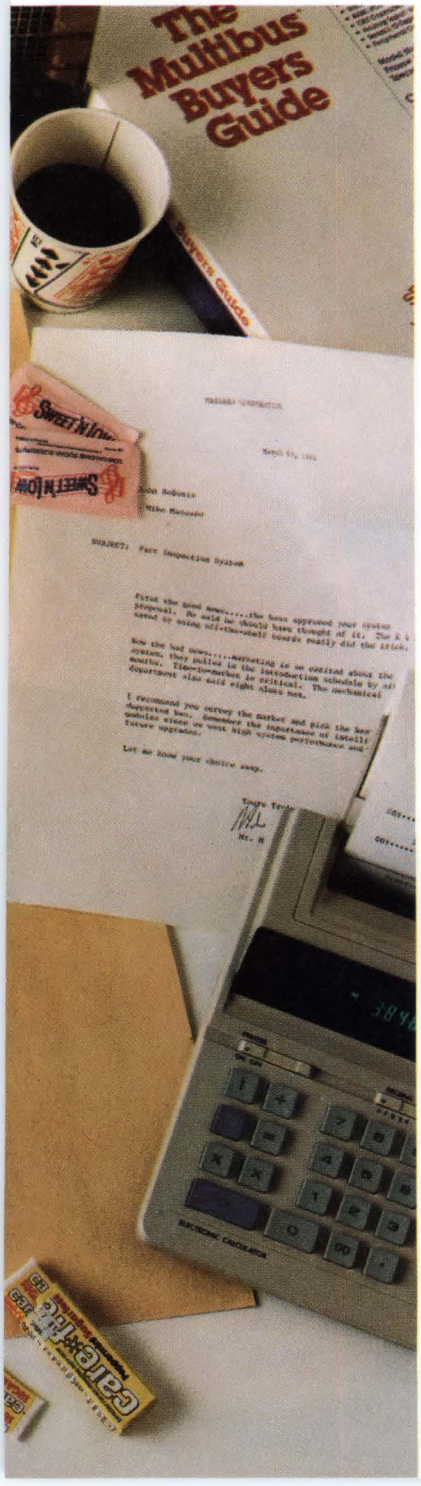

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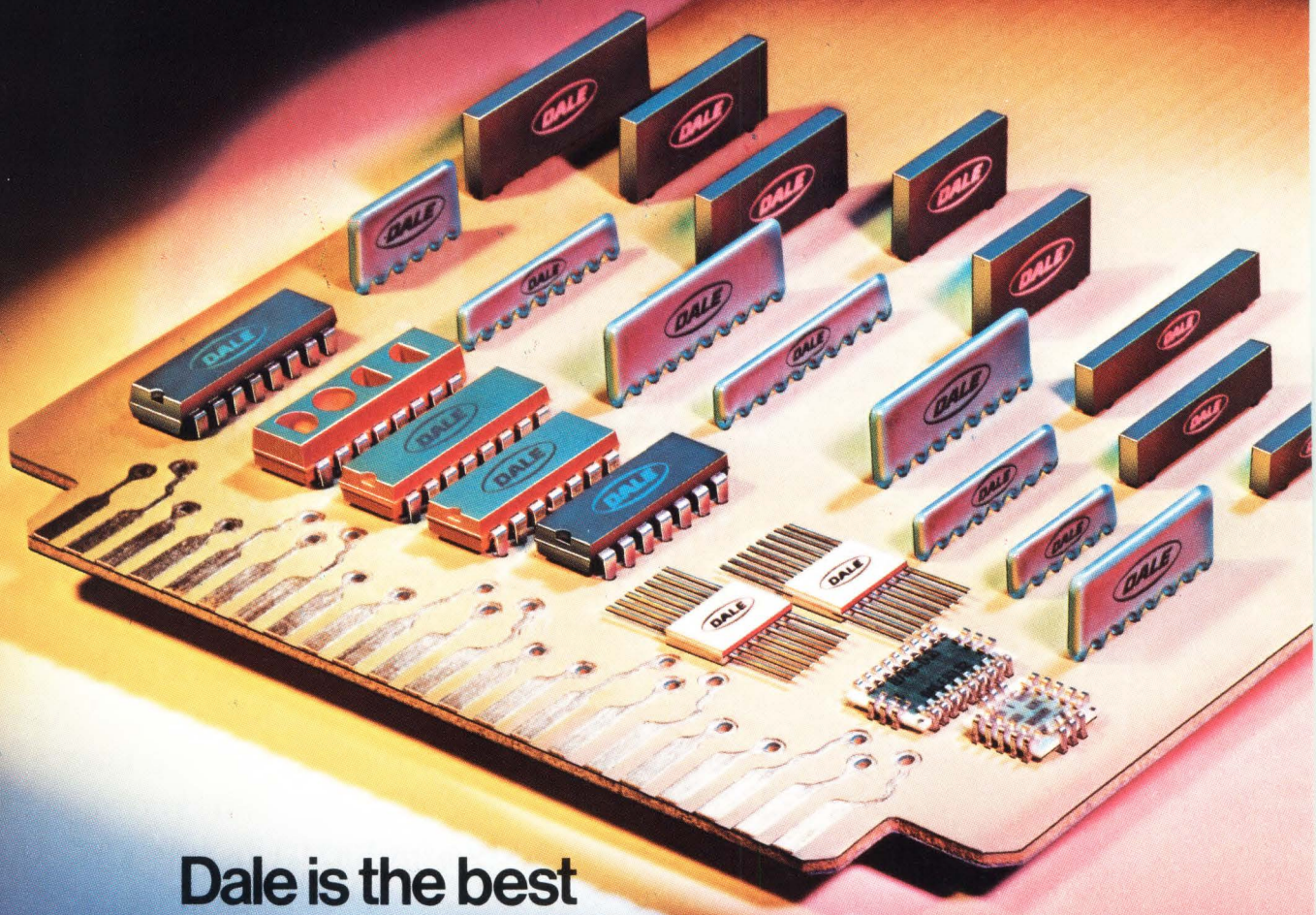

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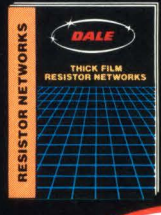

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Like logic analyzers, 1-GHz oscilloscope triggers on specific patterns

A host of triggering options lets an instrument hunt down glitches, arming it with a scope's sharp eyes and a logic analyzer's brain.

This is the fourth and final article in a series discussing the HP 54100 oscilloscope. The introductory piece appeared as the cover story of the Oct. 18 issue.

The good news is that TTL and ECL chips are steadily picking up speed, making for ever-faster systems. The bad news is that these chips' soaring switching rates and circuit complexity have opened a gap between oscilloscopes and logic analyzers, the tools on which engineers most depend to verify and troubleshoot their latest subnanosecond designs. Oscilloscopes quick enough to view nanosecond and subnanosecond pulses lack the power to trigger on important points of interest. Alternatively, logic analyzers excel at triggering but do not have a scope's ability to resolve subtle voltage and timing characteristics.

The HP 54100D, a digitizing oscilloscope with a bandwidth of 1 GHz, neatly bridges that gulf. Like a scope, it captures a waveform's vital timing and voltage features and does so with amazing speed, ease, and precision; like a logic analyzer, the instrument's sophisticated pattern recognition and triggering capture events that no ordinary scope could hope to find. Specifically, the instrument can trigger on a fault's effect, while giving designers the chance to view events long before or after that effect. And this ability is crucial to tracking down the fault's cause. In fact, the scope's pretrigger delay can stretch to 200 ms or 10 screen divisions, whichever is greater. The posttrigger delay can be set to up to 1 s or 10 screen divisions, whichever is longer.

Like the 54100A, the D version's trigger mechanism responds to signals with up to a 500-MHz repetition rate. Both scopes recognize a binary pattern across their signal and external-trigger inputs and feature a hold-off scheme that works with time or with the number of events. Unlike other scopes, both 54100s also dedicate an independently programmable comparator to each input, meaning that each input can be set for a different logic level. Further, the 54100's trigger point is fixed by digital controls and is consistently repeatable, even for pulses as narrow as 1 ns. It needs none of the fine-tuning that analog trigger circuits are infamous for.

The D version sports substantially more in the way of logic pattern recognition and triggering qualifiers than the otherwise identical A version. Its second external-trigger input, for instance, raises to four the total number of in-

Scott A. Genther, Hewlett-Packard Co.

A research and development engineer, Scott A. Genther joined HP's Colorado Springs Division in 1981. As a member of the design team for oscilloscope R&D, he has worked with high-speed logic at the IC, thick-film, circuit board, and system levels. Genther holds a BSEE and an MSEE from the University of Tennessee.

puts across which a pattern is recognized. Time-qualified pattern triggering, which requires that a pattern prevail for less (or greater) than a specified period before it is considered valid, is another of the D-version's enhancements. State triggering, which acts on a pulse edge only if the remaining inputs match a specified pattern, and event-delayed triggering, which counts events before arming the trigger circuit, are two more of its unique features. Time-delayed triggering rounds out the package: similar to event-delayed triggering, it waits a specified time—rather than a number of events—before responding.

As well equipped as it is to seek out and display subtle errors or verify critical timing margins, the scope's triggering ability is still somewhat modest compared to the latest logic state and timing analyzers. Their sophisticated triggering sequences often encompass 32 or more parallel bits. The scope truly shines, though, when its 1-GHz bandwidth, 10-ps resolution, and 100-ps timing accuracy are considered. Its choice of variable- and infinite-persistence, and averaging-display modes are equally significant. And, when necessary, the instrument can be used in conjunction with a logic analyzer to establish highly complex trigger points. Such an arrangement also serves to make up for a logic analyzer's jitter. Thus, wedding the scope to a logic analyzer gives designers and troubleshooters the most incisive views of a circuit's operation.

High road, low road

Behind the scope's ability to make complex triggering decisions is its dual-path triggering system (Fig. 1). Each input to the system feeds an adjustable-threshold comparator, the output of which is split into 500-MHz and 200-MHz paths. It is these parallel paths that give the scope's trigger its sophisticated counting and timing features without sacrificing its excellent (1-ns pulse) dynamic response. Shunting the timing and counting to the slower path ensures that they do not impair the system's fundamental trigger response, which uses the faster path.

At any time, the trigger system operates in one of five modes, which the user selects with menu-defined pushbuttons, or soft-keys. These include the aforementioned pattern, state, time-, and event-delay triggers, and an additional one called edge triggering. Particular settings can be quickly reviewed by reading, in order; the soft-key labels. These labels, which describe the function of the trigger mode and also display the current selection, combine to form a menu syntax.

Of the five modes, edge triggering is closest to the scheme found on conventional scopes, in which a single input threshold and its slope specifies the trigger point. Actually, it is a special variation on the more powerful pattern mode, which triggers the scope when a particular pattern of input signals enters or exits.

As with all modes, the trigger system's comparators determine the voltage levels that represent 0s and 1s. A specific input pattern is entered when all the inputs match the specified pattern. For example, edge-triggering on a positive-sloped signal on channel 2 is the same as setting the trigger to respond on pattern HXXX. In the scope's menu syntax, this setup would read as "Trig on Pattern HXXX When Entered."

In a sensitive state

State triggering is similar, except that one of the four inputs is assigned to be edge-sensitive. That is, the scope triggers on the rising or falling edge of the assigned input, provided that a specified pattern is present on the remaining three inputs. State- and pattern- triggering differ in that the former is activated only when an edge occurs at the selected input. In the latter, any active input can generate a trigger.

Finally, time- or event- delay modes count either intervals or events, commencing with a qualifying trigger at a selected input. The scope then ignores successive triggers, until a specified interval or number of events have passed. At that time, the trigger circuit is enabled and the scope is ready to respond to the next event.

The pattern mode allows the user to define up to 81 Boolean combinations of the scope's four inputs. Each input is assigned one of three values—H, L, or X. These stand for high, low, or don't-care logic levels, hence the 81 combinations (3^4).

The pattern HLXX, say, is true when the signal on channel 1 is high and the signal on

channel 2 is low. The pattern is false when channel 1 is low or channel 2 is high. The levels assigned to channels 3 and 4 are not considered.

With a pattern specified and the comparator thresholds for each input set, the user can pick one of four variants of pattern triggering: trigger when entered, trigger when exited, and two time-qualified schemes that trigger the scope if a pattern is present for longer or shorter than a specified interval.

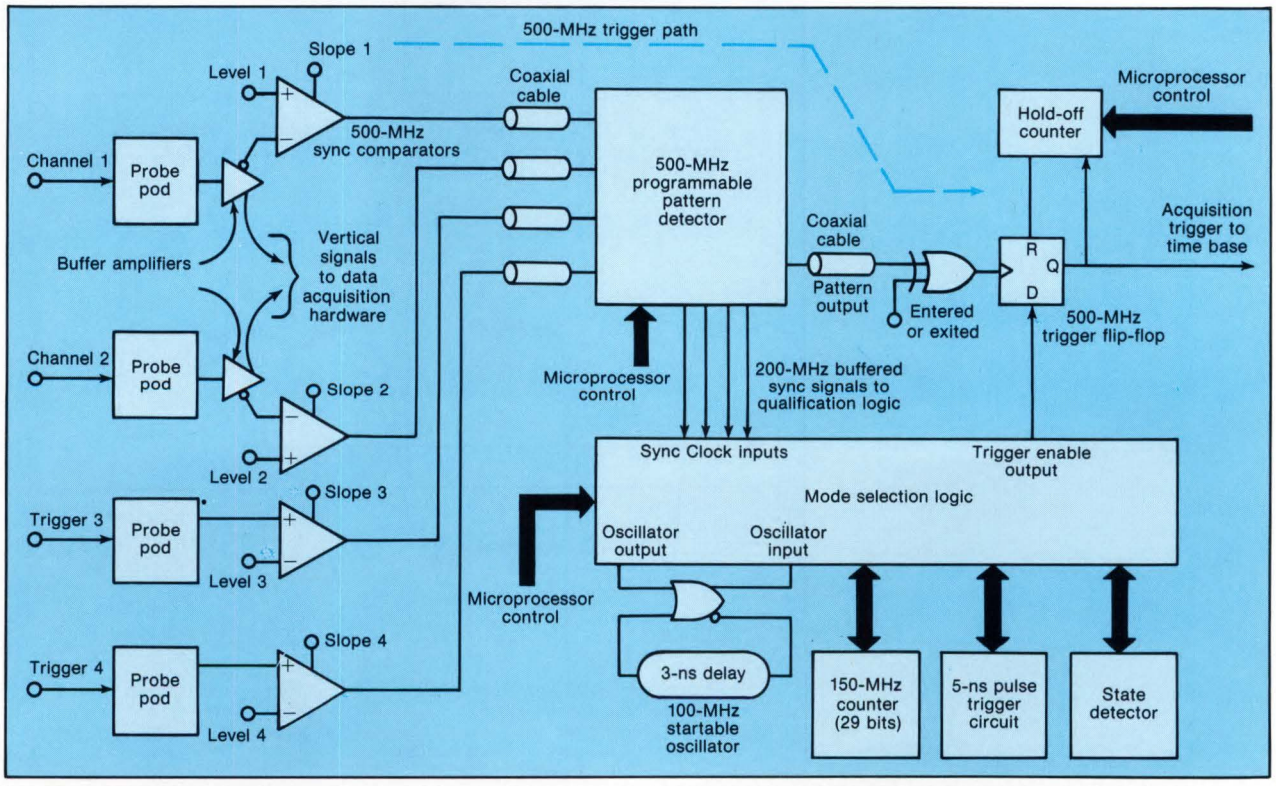
The menu syntax for the first variation is "Trigger on Pattern When Entered." Here, the trigger occurs when the pattern first becomes true. In terms of individual inputs, this happens when the last input changes to match the desired pattern. HLXX, for instance, would represent a low-to-high transition on channel 1 when channel 2 is low, or a high-to-low transition on channel 2 when channel 1 is high.

In the second subordinate mode the menu syntax reads "Trigger on Pattern When Exited." With it, a trigger is generated when a pattern goes from true to false. The input that causes the trigger is the first transition out of the specified pattern.

The last two variations qualify a pattern by the amount of time that it remains true. In one, the trigger is set to occur when a pattern exits, but only if it had been true for at least as long as the specified, or filter, time. If the pattern shifts from true to false before the filter time elapses, then there is no trigger.

Alternatively, a trigger takes place when the pattern is exited, but only if it had been true for less than the specified filter time. If it remains true longer, it does not qualify as a trigger. In all cases, the filter time can be set from 10 ns to 5 s (in 5-ns intervals from 10 ns to 2 μs) with an accuracy to within $\pm 3\%$.

Because it triggers only on pulses shorter than a specified interval, the last subordinate mode is particularly valuable in isolating infrequent glitches. First, the scope's infinite-persistence display easily reveals such glitches

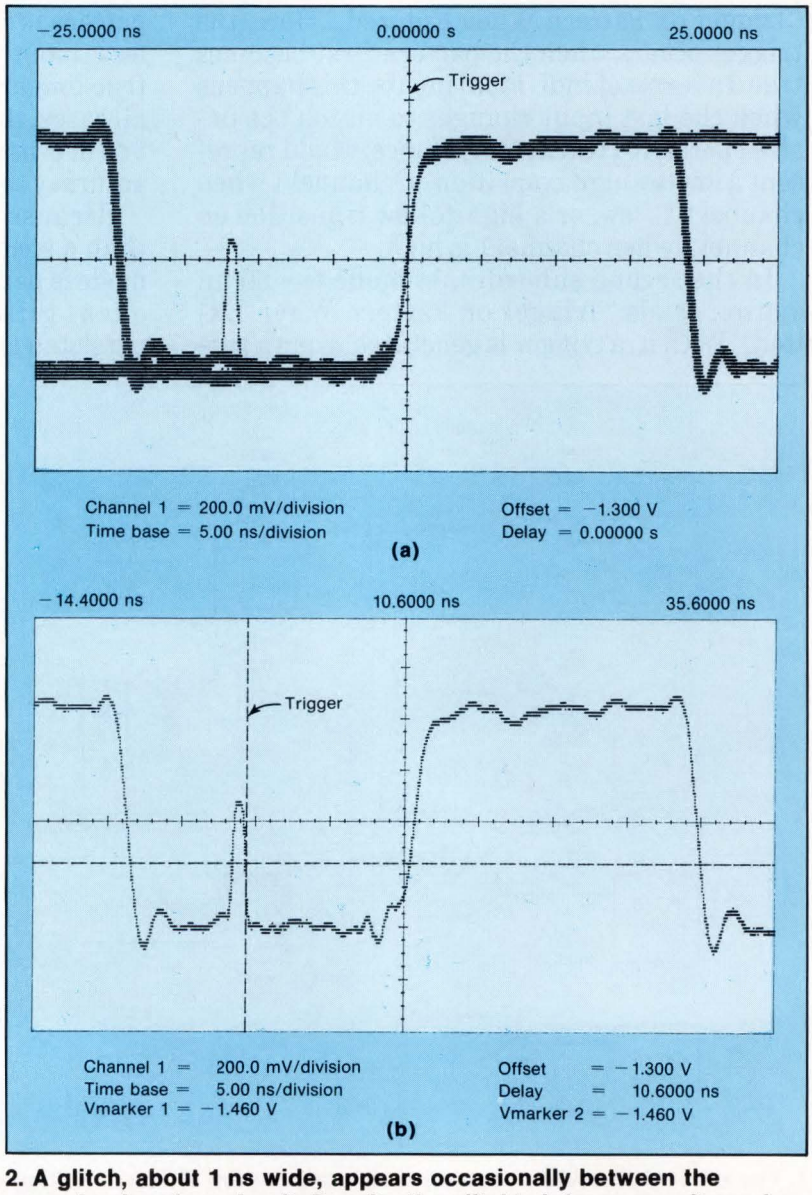


1. The HP 54100D oscilloscope owes its combination of very fast triggering and sophisticated digital pattern recognition to its having both a high-speed (500-MHz) and a low-speed (200-MHz) signal path. Further, its four inputs, two of which are also for the display, have separate comparators that allow each input to be set to a specific threshold.

among longer pulses (Fig. 2a).

Next, to trigger on the glitch alone, it is necessary to realize that it will be much narrower than the pulses surrounding it. This situation clearly suggests using the second subordinate mode to selectively trigger on the glitch by setting the pattern to HXXX with a filter time of 10 ns. The complete menu syntax for this setting would be "Trigger on Pattern HXXX When Present $<$ 10 ns." Finally, setting the trigger level so that the glitch crosses it, locks the scope onto just the glitch (Fig. 2b).

Actually, it takes more than setting a precise trigger point to capture the glitch, and the fact that the trigger system does what it does highlights not just its flexibility but its excellent pulse response and recovery time as well. The pulse response, made possible by the trigger system's 500-MHz signal path, helps it to capture the 1-ns glitch. At the same time, the



2. A glitch, about 1 ns wide, appears occasionally between the normal pulses in a circuit. Despite the glitch's infrequency, it can be easily seen thanks to the scope's infinite-persistence display (a). Moreover, the scope can trigger squarely on the glitch by being programmed to respond only to pulses less than 10 ns wide (b).

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system's 8-ns recovery time (the time needed for the filter timer to reset itself) allows it to capture all the pulses, even ones that are only 10 ns apart. Compare this capability with that of many logic analyzers, whose recovery time is as long as the programmed filter time.

Another task, flushing out timing anomalies in an asynchronous handshaking protocol, showcases the scope's ability to cut troubleshooting time. This job combines time-qualified pattern triggering and the scope's ability to view events that happened long before the trigger itself.

Asynchronous handshaking is a technique to minimize the transfer time between digital subsystems. Bus cycles are initiated by a controller, like a microprocessor, and are not deemed complete until an accessed peripheral, like a DMA controller, signals that a task is done.

The simplest version of asynchronous handshaking involves only a request (REQ) and an acknowledge (ACK) signal. The first is generated by the controller; the second, by the peripheral. In a typical handshaking sequence, the controller sends REQ high, indicating to the peripheral that the data on the bus is valid and it should start working. The peripheral responds by forcing ACK high when it is ready to return data. When the controller senses that ACK is high, it accepts the data and pulls the REQ line low. The peripheral completes the cycle by pulling ACK to its original low state.

Keep in step

The handshaking mechanism requires special circuits to operate asynchronously alongside a typical system's synchronous clock. If designed improperly, these circuits can cause timing violations and, as a result, occasional intolerably long bus cycles. Fortunately, the scope's time-qualified pattern trigger helps to pinpoint these anomalies and track down their sources.

When the scope is hooked into the relevant circuit points, it shows a REQ (upper channel) and ACK (lower channel) sequence (Fig. 3a). Triggering on the low-to-high transition of the REQ line, the instrument reveals a double trace on both channels, indicating that sometimes the peripheral takes very long to respond to REQ. As in the foregoing example, the scope's infinite-persistence display keeps the infrequent anomaly in view.

To trigger only on the longer cycles, the pattern-mode is set, in menu syntax, to "Trig On Pattern HLXX When Present > 80 ns." This results in a trigger when the response time (from REQ = 1 to ACK = 1) is greater than 80 ns, which filters out the normal, shorter cycles.

Looking back in time

Once it is verified that the trigger is capturing only the longer cycles, the pretrigger delay allows the troubleshooter to view events before the start of the handshake (Fig. 3b). To free the scope's vertical channels and permit probing of other points in the circuit, the handshaking signals and their trigger settings can be easily moved to the scope's two external trigger inputs.

Often, digital signals, like those found in a serial data link or at the output of a disk drive, occur repeatedly but unpredictably. Some analog signals, like the composite video voltage associated with a test pattern, behave similarly. Three problems can limit a conventional scope's ability to observe these signals: a repetition rate too low to produce a visible display; timebase jitter inherent in the instrument itself; and system jitter between the signal and the synchronizing pulse (particularly when a mechanical device generates the clock reference). All three can spell trouble, even when the system under test supplies an external trigger pulse to synchronize a scope's display.

The new scope addresses each of these limitations, respectively, with its infinite-persistence display, ultrastable time base, and delayed triggering capability. The first eliminates the problem of low repetition rate, since the display will not fade between a signal's occurrences. Next, the scope's time base is crystal-controlled consequently exhibiting very little jitter—even over delays of thousands of screen diameters. In fact, the specified rms value of jitter is 50 ps + 0.5 ppm of the delay setting. Finally, the trigger system's delay can overcome the problem of system-induced jitter by using one input as a qualifying source and another as the actual trigger.

Consider, for example, the 218th pulse in a

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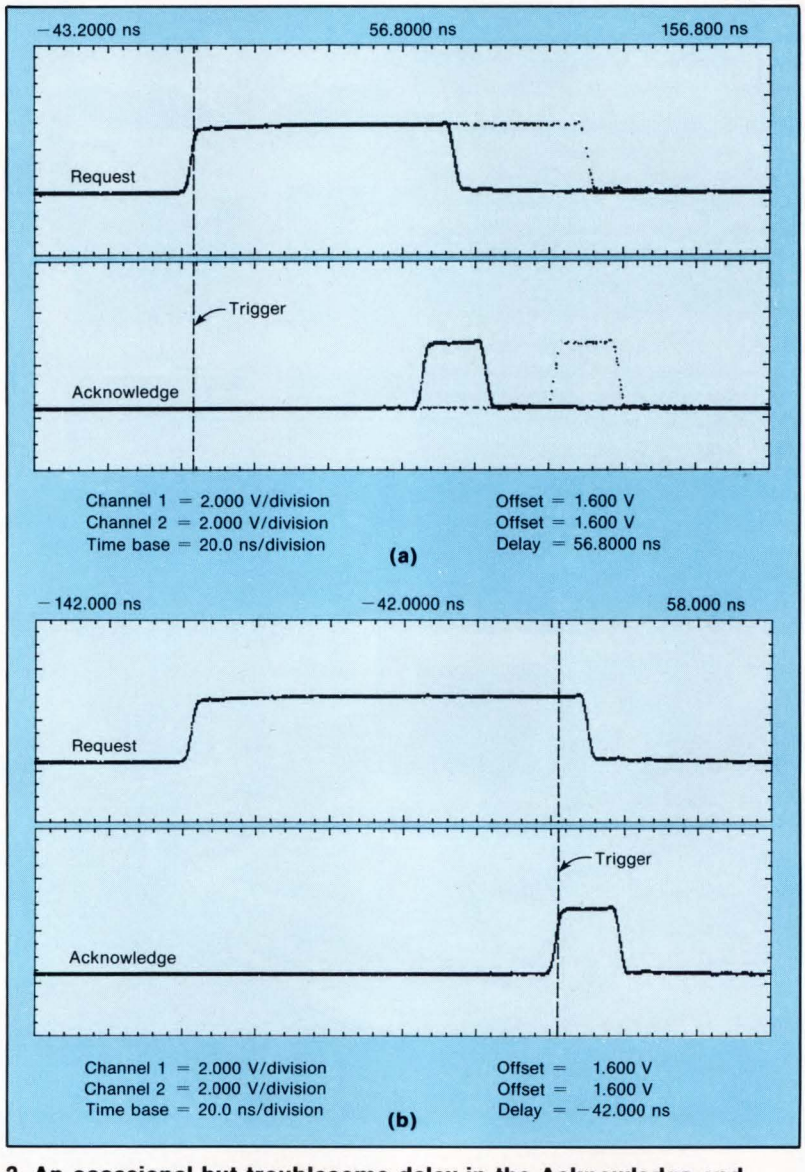
Digital oscilloscope

string, which shows jitter with respect to a pulse used to synchronize the scope (Fig. 4a). To view the event without jitter, the actual triggering point is shifted to the 218th edge by using the event-delayed trigger. After a qualifying edge like the system's sync pulse triggers the delay counter the scope counts a predefined number of events and then triggers on the last, in this case the 218th. The menu syntax for this setup reads "After Positive Edge On Chan 2 Trigger On 218 Events Of Positive Edge On Chan 1," which lets the triggering system produce a jitterless display (Fig. 4b). The range of the event-delay count is from 1 to 99,999,999 events. It works for repetition rates of over 150 MHz and is ready to go less than 2 ns after the qualifying event.

The same approach is also very useful for viewing composite video signals of almost any format. If the input comparators is set so that



3. An occasional but troublesome delay in the Acknowledge and Request handshaking protocol appears as a double trace on the upper and lower displays (a). To activate on the longer cycles, the trigger is set for patterns that are longer than 80 ns in duration (b).

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IMAGE CAPTIONS

Top:

- *Left back corner: 2-D FFT processed in 2 minutes with LIPS Plus.*
- *Four 1024^2 medical images: multimodality, split screen display.*
- *Face: CT scans in 3-D modeling, plastic surgery at Mallinckrodt.*
- *Mountains: LIPS assists fast graphics hardware and large memory matrices with GKS-based Auxiliary Graphics Processor. Courtesy S.A.I.*
- *Pseudo-colored flowers: shows LUT manipulations. Note graphic load display plus intensity reference scale.*
- *Same 1024^2 flowers: shows color cut and paste in 1 frame time.*
- *Jars and pens: Synthetic image like #4, courtesy Pacific Data Images. Photo by Jim Weil.*

Bottom:

- *Two corners: LIPS driver supports 1024^2 LANDSAT imagery, courtesy NASA-Ames Research.*
- *Top bas relief: Matrix filter, the basis of classification and recognition. LIPS allows kernels of any shape and size and executes at video rates.*
- *Histogram: line or pixel analysis under LIPS.*
- *Spheres: fast Z-buffer merge, courtesy Rensselear.*
- *Cake and strawberries: 1024^2 looks good enough to eat.*
- *Bottom: mesh algorithm, courtesy Lunar & Planetary.*
- *Weather satellite: shows graphics overlay, courtesy MacDonald Dettwiler.*

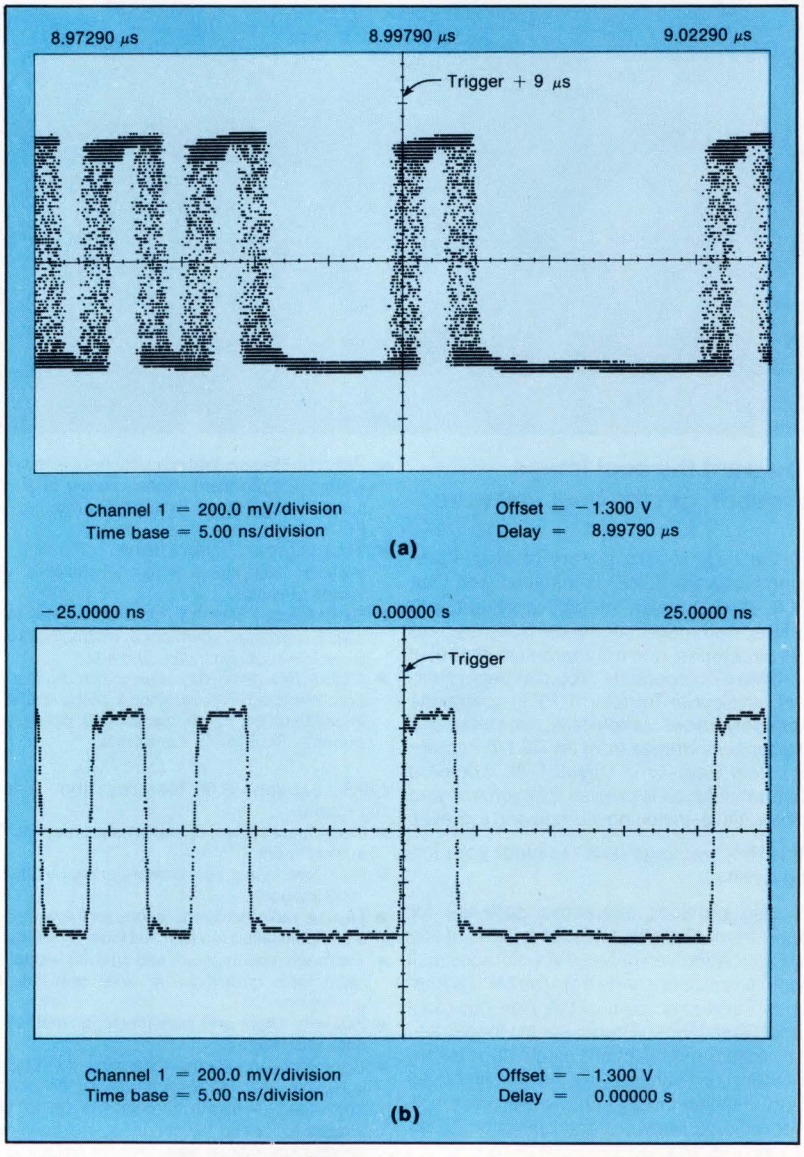
CIRCLE 94

GOULD
Electronics

only the vertical and horizontal sync pulses cross the comparator's threshold, the sync-pulse edges are the only ones seen by the delay counter. Thus simply setting the counter to the proper (and easily calculated) number of sync pulses locates any horizontal scan line and, ultimately, any pixel of the video display.

The time-delay trigger is similar to its event-delay counterpart and is generally applicable in the same situations. In some cases, such as when events between a sync pulse and a signal occur intermittently, the time interval is needed to ignore any intervening events.

More specifically, after a qualifying event, a specified amount of time goes by, after which the next event generates a display trigger. The delay can be set from 20 ns to 5 s with an accuracy to within ±3%. Because the trigger event



4. Jitter appears on the 218th pulse in a string when it is triggered on an external sync signal (a). To eliminate it, one scope channel is set to start the event-delay counter; which is programmed to count 218 events before triggering. The resulting display on the second channel is free of any jitter present between the sync pulse of the system under test and the observed pulse (b).

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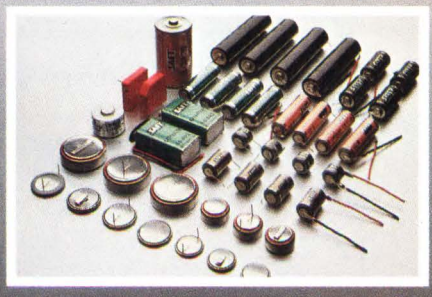

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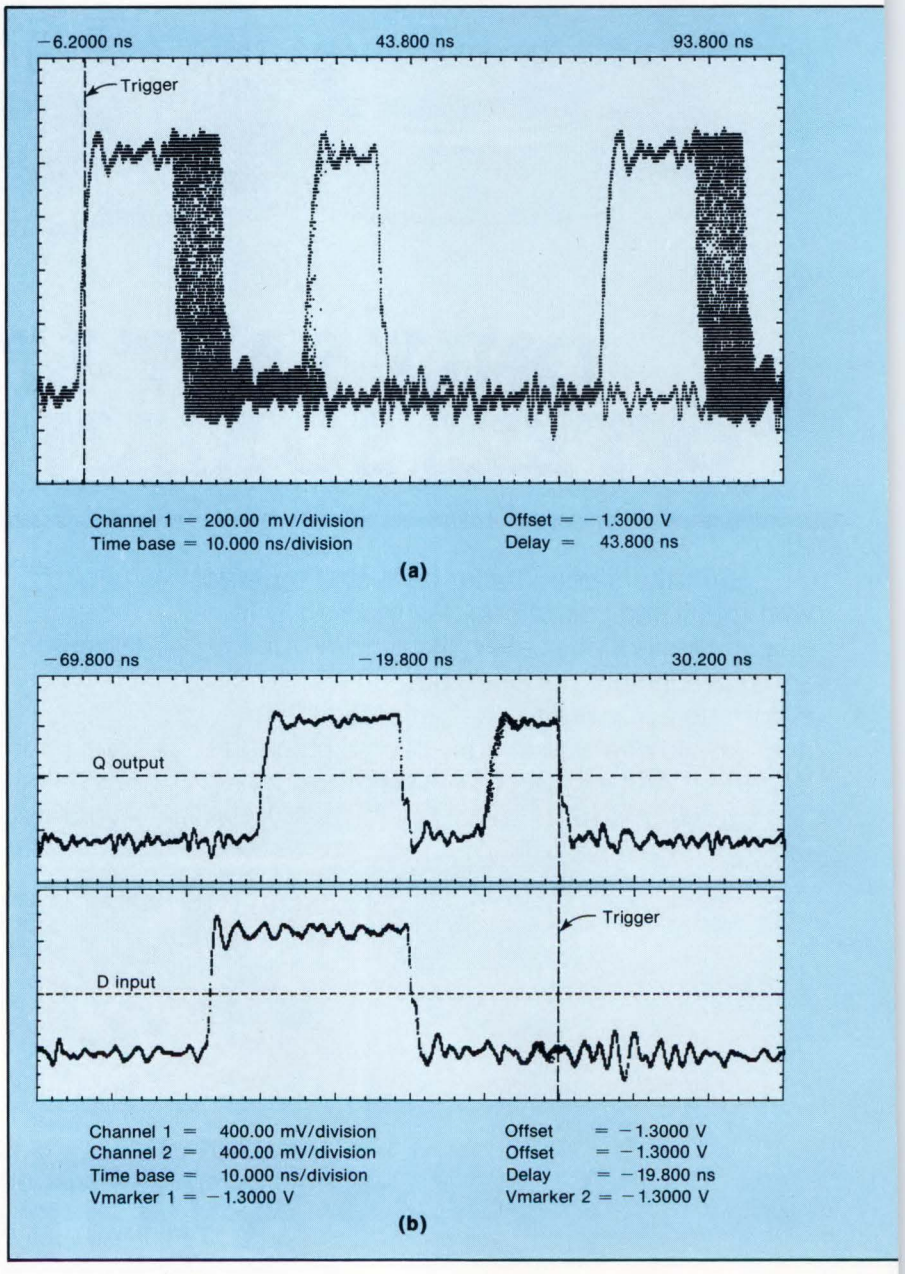
Digital oscilloscope

is carried along the trigger system's high-speed path, events as short as 1 ns will produce a display. Finally, in both delay modes, the qualifying trigger can be as short as 5 ns.

Despite the scope's extensive logic triggering capability, it is possible that only the sophisticated triggering algorithms and wide bit-path of an advanced logic analyzer will locate a particular event of interest. In such cases, though, the scope can still equip the analyzer with the advantages of pre- and post-trigger viewing, high accuracy and resolution, and infinite persistence. In addition,the instrument's delayed trigger eliminates the effects of jitter that usually exist between a logic analyzer's sync output and clock.

To couple the two instruments, the logic analyzer's trigger output becomes the scope's qualifying source and is connected to one of the latter's inputs. The signal of interest (or one that is synchronous with it) is connected to another of the scope's inputs. That input is chosen

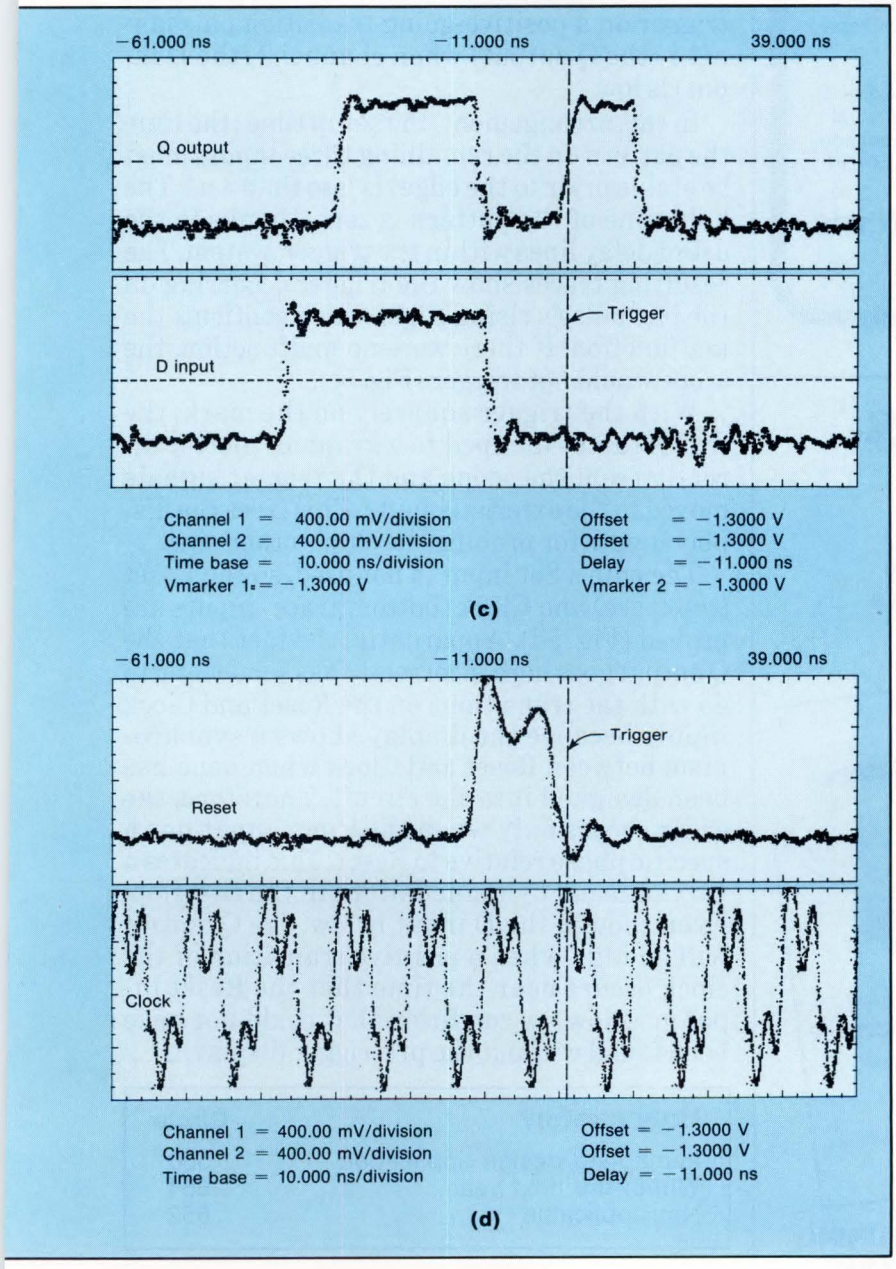


5. A narrow pulse on the output of a D-type ECL flip-flop appears to cause a circuit to malfunction (a). Triggering on the narrow pulse only and displaying the Q output and D input shows that the glitch violates the flip-flop's logic (b). Then, triggering on the pulses' rising edge confirms the abnormal operation (c), and switching the display to the Reset and Clock pulses, without changing the trigger, shows the nature of the flip flop's malfunction (d).

as the trigger source. With the scope's event-delayed trigger active and the number of events set to one, the vertical trigger will occur on an event that is synchronized to the signal of interest. As before, both trigger inputs (the qualifying and actual display trigger) can be the viewed signals or else moved to the scope's trigger inputs to free the vertical inputs for probing points in a circuit.

With or without the help of a logic analyzer, the scope's triggering and pretrigger delay abilities are powerful tools that stand to save the weeks often spent diagnosing a problem. Consider, for instance, the output of an ECL D-type flip-flop in a malfunctioning asynchronous circuit (Fig. 5a).

The correct output consists of a series of pulses of varying widths separated by about 70 ns. Occasionally, though, a premature pulse comes through. Because the normal pulses are always more than 10 ns wide and the aberrant pulse is less, the scope's time-qualified trigger-



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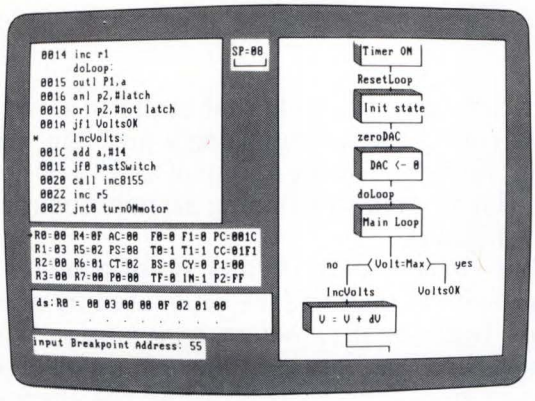

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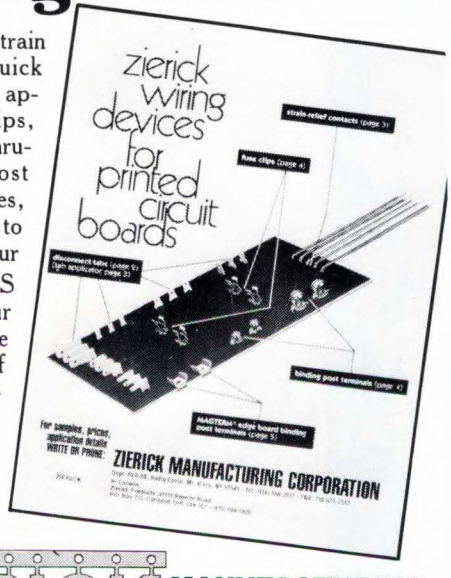

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CIRCLE 97

DESIGN ENTRY

Digital Oscilloscope

ing can lock onto the shorter pulse (Fig. 5b). Moreover, comparing the flip-flop's Q output (upper trace) to its D input (lower trace) and using the scope's pretrigger delay reveals that the output is going high while the input is low—an apparent malfunction of the flip-flop.

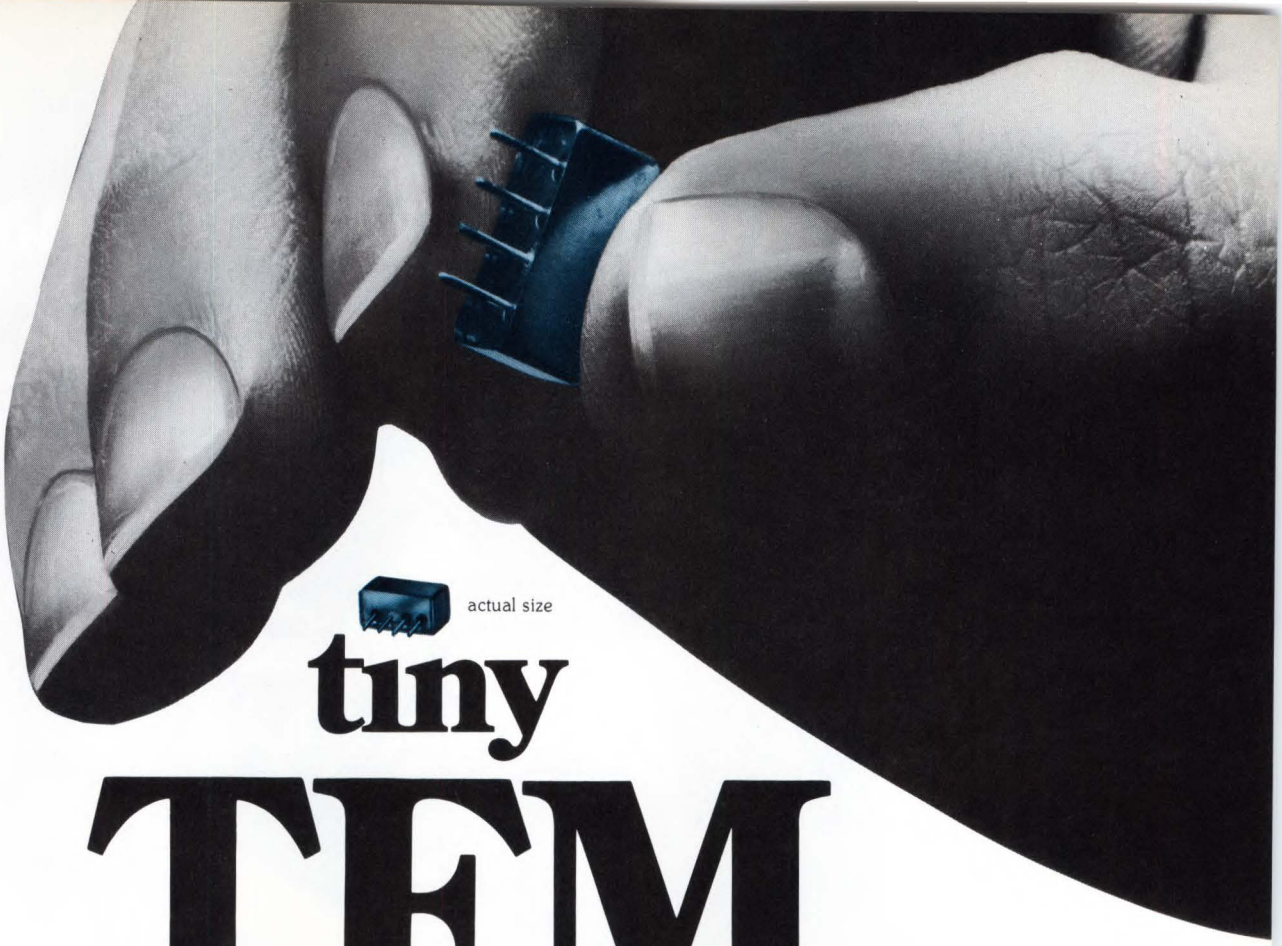
Using state triggering, which assigns one of the inputs to be edge-sensitive, the user activates the scope precisely on the unwanted output transition. The menu syntax for this setting is "Trigger On Positive Edge On Chan 1 When Pattern —LXX Is Present." In other words, trigger on a positive-going transition on channel 1 (the Q output) when channel 2 (the D input) is low.

In this arrangement, the setup time (the time the pattern on the remaining three inputs must be stable prior to the edge) is less than 4 ns. The hold time of the pattern is zero, thanks to the use of delay lines within the trigger system. The resulting traces show the trigger occurring on the bad pulse's rising edge, which confirms the malfunction. If there were no malfunction, the scope would not trigger (Fig. 5c).

With the trigger squarely on the mark, the traces can be dumped to a graphics plotter directly from the scope and the trigger signals moved to the external inputs. This frees the display inputs for probing the chip's other pins.

The chip's Set input is not used, so the Reset (top trace) and Clock (bottom trace) inputs are probed (Fig. 5d). Apparently, the fact that the Q output goes high incorrectly has something to do with the transitions on the Reset and Clock inputs because the display shows a synchronism between Reset and Clock when none has been designed into the circuit. Therefore, the error occurs only when the Clock input has a specific phase relative to Reset. This indicates a very unusual dynamic failure in the flip-flop. Even though the D input is low, the Q output will go high when a positive transition of the clock occurs near the time that the Reset input goes low—a condition that could not have been found without the pretrigger display. □

How useful?	Circle
Immediate design application	550
Within the next year	551
Not applicable	552



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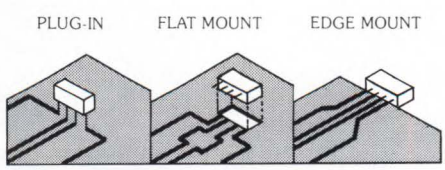

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			1 Octave from Band Edge	Total Range	Lower Band Edge		Mid Range		Upper Band Edge		$	
	LO/RF	IF			LO-RF	LO-IF	LO-RF	LO-IF	LO-RF	LO-IF	EA.	QTY.
TFM-2	1-1000	DC-1000	6.0	7.0	50	45	40	35	30	25	11.95	(1-49)
TFM-3	.04-400	DC-400	5.3	6.0	60	55	50	45	35	35	19.95	(5-49)
TFM-4	5-1250	DC-1250	6.0	7.5	50	45	40	35	30	25	21.95	(5-49)
•••TFM-11	1-2000	5-600	7.0	7.5	50	45	35	27	25	25	39.95	(1-24)
•••TFM-12	800-1250	50-90	—	6.0	35	30	35	30	35	30	39. 95	(1-24)
▪▪TFM-15	10-3000	10-800	6.3	6.5	35	30	35	30	35	30	49.95	(1-9)
▪▪TFM-150	10-2000	DC-1000	6.0	6.5	32	33	35	30	35	30	39.95	(1-9)

•••If Port is not DC coupled
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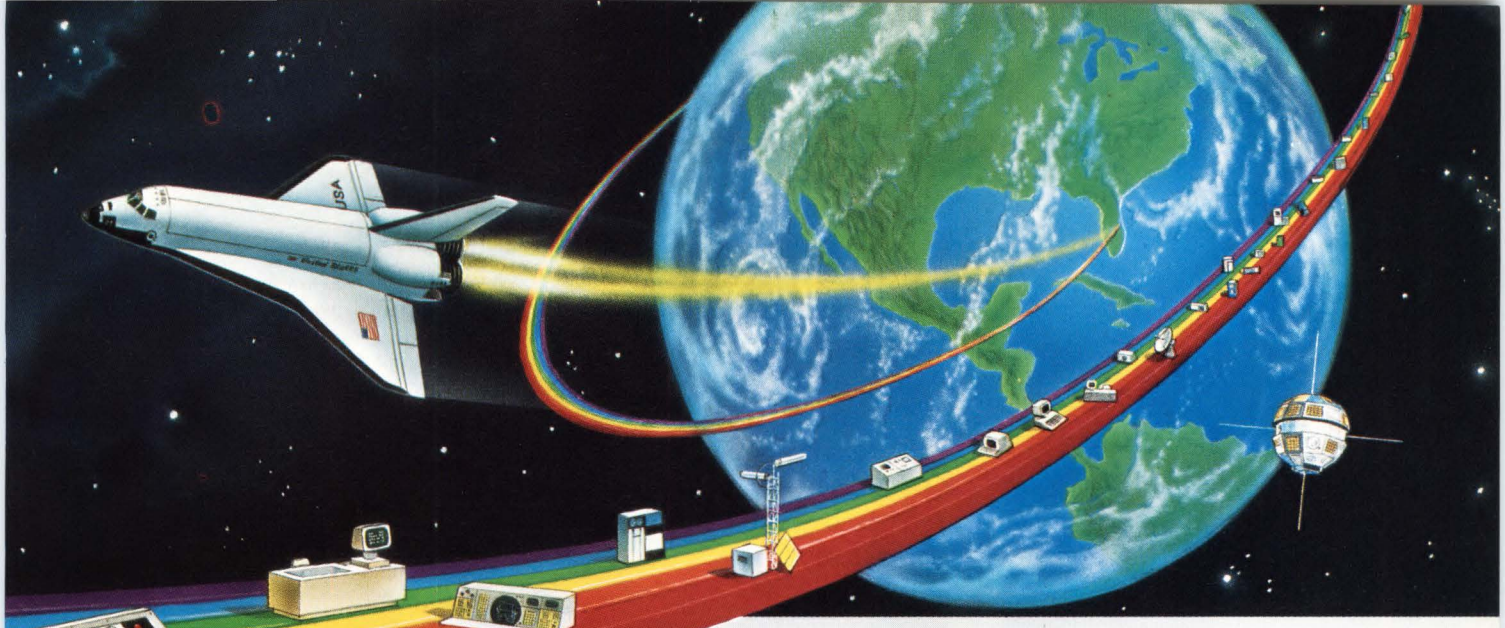

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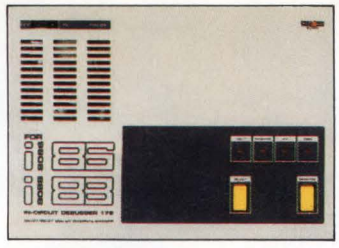

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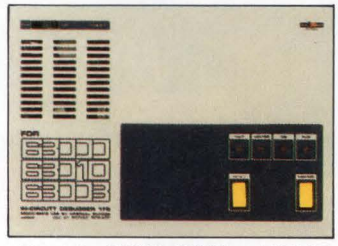

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- 68008

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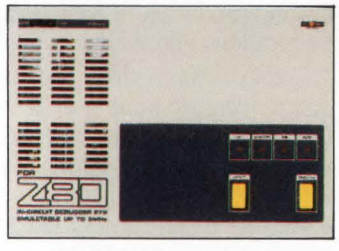

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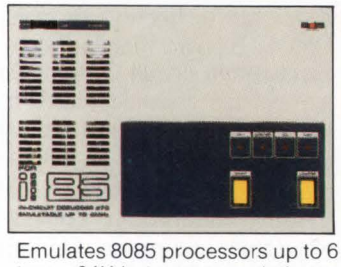

i8085

- i8085A
- i8085A-1
- i8085A-2

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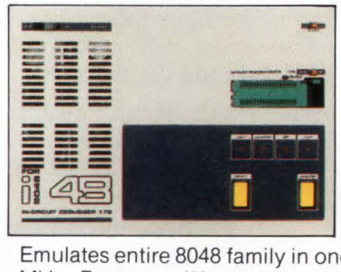

i8048

- i8048
- i8049
- i8050
- i8748
- i8749
- i8039
- i8035
- i8040

Emulates entire 8048 family in one unit to 11 MHz. Features; 4K emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands. 8748 and 8749 units feature a built-in EPROM programmer.

CIRCLE 100

DESIGN SOLUTION

Mastering the fine points of a programming language spells better software

Developing efficient code requires a familiarity with the internal workings of a programming language. Here PL/M-86 is put to work for the iAPX 86 microprocessors.

Knowing how to take advantage of a high-level programming language's subtler features can help a software developer squeeze the most performance out of a microprocessor-based system. The advanced capabilities of the popular PL/M-86, a structured modular language, gives developers several avenues for refining program code.

To be as effective as it is, a PL/M-86 compiler exploits the underlying microprocessor architectures of the iAPX 86 family, including the 8086, 8088, 80186, and 80188, as well as the 80286 when the latter is working with real addresses rather than protected virtual addresses. As a result, the language can optimize its machine code output for fast execution and minimum memory.

In all, there are at least four ways that a programmer can get the most from the PL/M-86 compiler—through the built-in procedures, code optimization, memory models, and subsystems. Although little or nothing can be done to compensate for poor programming or inadequate hardware, a well-planned and well-executed microprocessor system can benefit substantially if the programmer masters those four areas.

Built-in procedures and functions are like reserved words, because the compiler recognizes them automatically. However, unlike reserved words, the names of built-in procedures can be redeclared as ordinary variable names, but the built-in functions are relinquished. If the name is not redeclared, the compiler automatically invokes the predefined operation whenever the procedure is called. For example, MOVE is a built-in procedure that shifts a string of bytes for which the programmer has specified the source, destination, and quantity.

Like built-in functions, procedures draw on the various hardware features of the iAPX 86 architecture. The MOVE procedure, for example, uses the hardware's string operations. Unfortunately, any source code that depends on that or any other built-in procedure will not execute as efficiently on a microprocessor that does not incorporate them in its instruction set.

On the other hand, a built-in procedure frequently avoids the need for a branching sequence and in doing so improves a system's performance. In general, branching degrades a

Dan Lau and **Ujjal Kohli,** Intel Corp.

A senior software engineer with Intel's development systems operation in Santa Clara, Calif., Dan Lau concentrates on compilers and operating systems. He holds a BS in electronics engineering and computer science from the University of California at Berkeley.

Ujjal Kohli, now going for his MBA at Harvard Business School, was formerly a software product manager and engineer at Intel, where he developed the basic software for the iAPX 86 microprocessor family. He holds an MS in computer engineering from the University of Rochester.

system's speed, because it interrupts the instruction prefetch queue in the microprocessor's architecture. Other built-in functions help trim the time needed to scan strings, words, and bytes.

Easy initialization

Consider the SETB procedure, which sets all the elements of an array to one value, simplifying such tasks as initialization with statements like:

```
CALL SETB (0, @BUFFER, LENGTH (BUFFER));
```

In calling SETB, a programmer need only specify the string's new value, its location (using a pointer), and the number of bytes (or words, using SETW). If that same operation were coded with a loop (a form of branching), as in:

```
DECLARE I WORD;
    DO I = 0 TO LAST (BUFFER);
    BUFFER (I) = 0
END;
```

it would not execute as quickly as the previous one.

Another procedure, XLAT, translates a block of bytes using a table. The programmer specifies the array's source and destination and the location of the translation table:

```
CALL XLAT (@SOURCE, @DEST, LENGTH
          (SOURCE), @TRANSLATION);
```

The XLAT procedure could be applied to a communication system, translating character-encoding schemes like ASCII and EBCDIC. As with SETB, XLAT alone is far more efficient than would be the loop typically used for translating a string of bytes:

```
DO I = 0 TO LAST (SOURCE);
    DEST (I) = TRANSLATION (SOURCE (I));
END;
```

Not all PL/M-86 built-in procedures are callable. Some, like FINDB and its converse, SKIPB, are functions that return values or locations. FINDB searches a string of bytes (or words, with FINDW) for a specified value, called the target (Program 1a). On finding it, it points to that value's memory location. FINDB proves valuable when, say, a certain keystroke must initiate some action.

The execution time for FINDB depends on the time it takes to simply scan the string of bytes. On the other hand, the code performing the same function would contain a series of IF . . . THEN . . . ELSE comparisons and execute in considerably more time (Program 1b).

The function SKIPB searches for a byte that does not match a particular default value. One application is in a program, like a compiler, that must scan a string of input characters but ignore all blanks.

Besides using the built-in operations, a programmer can create fast and compact code by taking advantage of the compiler's optimization techniques. Where possible these techniques automatically reduce the amount of machine code without changing the code's semantics; knowing what kind of code these

Program 1. Searching for characters

```
DECLARE SEQUENCE (*) BYTE INITIAL ('AEI . . . Z');
DECLARE ORDER WORD;
ORDER = FINDB (@SEQUENCE, LETTER, LENGTH
  (SEQUENCE));
IF ORDER <> OFFFFH THEN
    DO CASE ORDER;
    /* DO 'A' ACTION */
    /* DO 'E' ACTION */
    /* DO 'I' ACTION */
    . . .
    /* DO 'Z' ACTION */
    END;
ELSE
    /* NOT A VALID LETTER */
```

(a)

```
IF LETTER = 'A' THEN
    /* DO 'A' ACTION */
ELSE IF LETTER = 'E' THEN
    /* DO 'E' ACTION */
ELSE IF LETTER = 'I' THEN
    /* DO 'I' ACTION */
ELSE IF . . .
    . . .
ELSE IF LETTER = 'Z' THEN
    /* DO 'Z' ACTION */
ELSE
    /* NOT A VALID LETTER */
```

(b)

techniques compress is to the programmer's benefit.

The optimization techniques lengthen somewhat the time required to compile code. Therefore, the programmer has the option of setting one of four degrees of increasing optimization, letting the programmer strike a balance between speed of compilation and economy of code.

A bag of techniques

The level chosen determines the use of techniques—for instance, constant folding; strength reduction; the elimination of common subexpressions (portions of an expression), superfluous branches, and unreachable code; and the optimization of indeterminate memory and register allocations.

During compilation at optimization level 0, for instance, the process of constant folding recognizes operations that are superfluous and can be removed or that can be combined with others, thereby saving memory space. Level 1 adds strength reduction, which substitutes equivalent but faster operations for longer ones, like shifting to the left to multiply by two.

Also at level 1, Boolean expressions are "short-circuited"; in other words, resolved without the compiler having to evaluate every term. For instance, the expression A>B AND I>J is always false if the term A>B is false. In that case the full expression can be considered false without resolving the issue of whether or not I is greater than J.

Finally at level 1, identical subexpressions are eliminated. To do that, the compiler looks at two operands at a time and reorders them to detect identical ones. Even though a subexpression may appear several times, the compiler generates the code that is needed to calculate the subexpressions only once.

When similar expressions contain more than two operands, a programmer must write those expressions in a consistent order. For example, the compiler, which groups two operands at a time, recognizes that the subexpressions (I+J) and (J+I) are identical, as are (J+I+K) and (I+J+K). However, it does not recognize that the expression (K+I+J) is also the same as the last two because it now sees K as the first operand. Therefore a programmer should write the same subexpressions in the same order (see the table, below).

Wherever possible, common subexpressions should be grouped together and not separated by calls, thereby avoiding any recalculations. Since the compiler does not carry the contents of registers across calls, the stored values of previously calculated subexpressions may be lost. By keeping common expressions together, the programmer avoids the need for recalculating or reloading register values that may help resolve similar expressions.

When mixing unsigned variables of different widths (like bytes, words, and double words), programmers should work from the wider value to the narrower one—a good tip for managing subexpressions. For example, if B and W are byte and word variables respectively, the assignment W = B will produce more instruc-

Eliminating common subexpressions

Expression	1	2	3
Original order	(I+J+K)	(J+I+K)	(K+I+J)
Grouping by two	((I+J)+K)	((J+I)+K)	((K+I)+J)
Preferred reordering	((I+J)+K)	((I+J)+K)	((I+K)+J)

tions than B = W; in the latter, the smaller width is expanded by adding zeros and then stored, involving extra instructions. On the other hand, going from wider to narrow variables involves only truncation.

What if?

In optimizing code at level 1, the compiler can recognize subexpressions that were used in the IF and THEN portions but not in the ELSE portion of a Boolean expression. Therefore it is better to structure the condition of an IF statement in such a way that the THEN portion can use the IF statement's evaluation. This is also a way for the programmer to benefit from the short-circuiting of Boolean expressions. Structuring expressions in this manner may require IF tests to be reordered.

Program 2. Putting expressions in order

```
/* Unoptimized */
DO CASE X;
    DO; /* CASE 0 */
        I = 0;
        J = 1;
        K = 5;
    END;
    DO; /* CASE 1*/
        K = 9;
        J = 1;
        I = 0;
    END;
    DO; /* CASE 2 */
        J = 1;
        K = 7;
        I = 3;
    END;
END;
```

```
/* Optimized */
DO CASE X;
    DO; /* CASE 0 */
        K = 5;
        I = 0;
        J = 1;
    END;
    DO; /* CASE 1 */
        K = 9;
        I = 0;
        J = 1;
    END;
    DO; /* CASE 2 */
        K = 7;
        I = 3;
        J = 1;
    END;
END;
```

In iAPX 86 processors, most arithmetic operations automatically set flag registers to indicate the operation's results, such as a zero, a carry, and so on. If unaltered by a subsequent operation, the flags set by a subexpression can be used immediately by a conditional statement that uses the same subexpression, without requiring additional code to reset the flags. Therefore the programmer should avoid situations that will alter the flag's registers between the evaluation of the common subexpression and the test.

Reducing redundant code

Finally, at optimization levels 2 and 3, the compiler can detect common code sequences by looking for paths to the same point in a set of instructions. If two paths to the same point have identical code, the compiler deletes the code from one path and inserts a branch to the identical path. To help the compiler find identical code sequences, the programmer should always write sequences of statements in the same order (Program 2).

Besides optimization, the PL/M-86 compiler also benefits from the segmented memory found in the iAPX 86. That segmentation allows a program to make short (16-bit) efficient references to local data items and procedures. However, it can still access the full 1-Mbyte address space when necessary.

The iAPX 86 architecture features four so-called segmentation models: small, compact, medium, and large, each offering a different trade-off of performance and program size. Specifically, performance generally improves by going from large to small models, and within each model a programmer can still maximize performance by following certain guidelines—for instance, declaring a procedure to be public, eliminating external data references in large models, and carefully using address pointers.

For insight into these guidelines, consider why small and compact models execute better than medium and large ones: In the latter pair, each source module forms a separate code segment, so that the compiler views any call to a procedure or function in another module as an external long (32-bit) call. In other words, the

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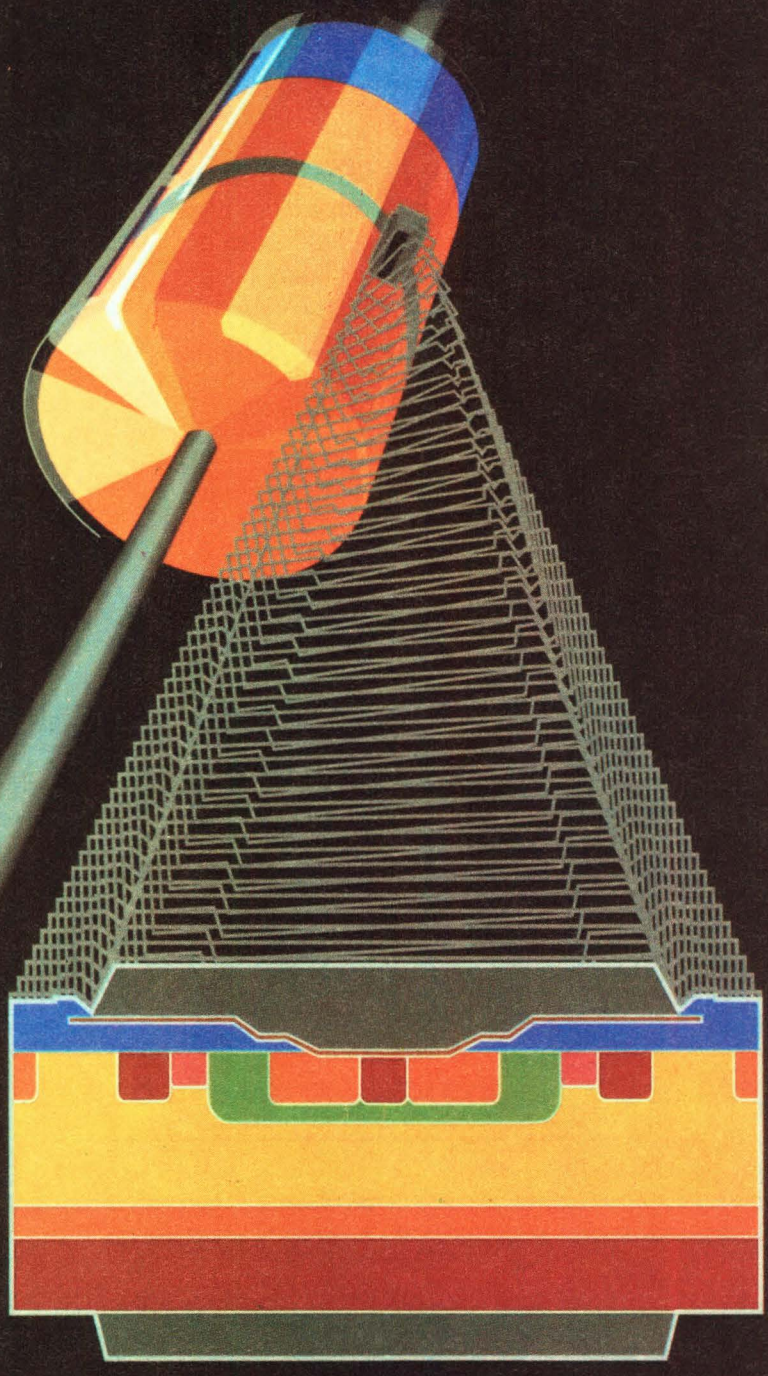

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CIRCLE 101

call instruction must switch to another code segment. It must save the contents of both the code-segment and instruction-pointer registers and later reload them. Short calls, on the other hand, require saving and reloading only the instruction-pointer register.

Going public

Regardless of the segmentation model, a procedure can be called from within its own module using only short calls. That does not hold true for a procedure that has been assigned a public attribute, meaning it can be called from outside a module. If a symbol is given a public attribute (for a medium or large model), it is automatically accessed only with a long call, even if that call is actually made from within the same module. In contrast, if a procedure cannot be reached from outside a module—in other words, it is not declared public—the compiler knows that only short calls are necessary and codes the procedure accordingly.

Thus, the first guideline of segmentation is to avoid making procedures public, unless absolutely necessary. That goal can be met by putting all related procedures in the same module and declaring as public only those that must interface with other modules having the same attributes (Program 3a).

In a large model, referring to a data item in an external module is less efficient than if the data item were local. That inefficiency is the same for intermodule procedure calls in medium and large models: The compiler must generate instructions to switch a segment register (Program 3b). On the other hand, if a data item in a large model is found within the module being compiled, a more efficient short reference suffices. In small, compact, and medium models all data items from all modules are in the same segment; thus there is never a need to switch segments.

A judicious use of pointers (indirect addresses to data items) is yet another way to ensure efficient coding. For all but the small RAM model, which itself is a subset of the small model, the compiler works with either a 32-bit pointer or a 16-bit offset word. The pointer is more powerful and allows the programmer to address the complete address space of the iAPX 86 architecture. However, because the pointer occupies 32 bits, it can be manipulated only through two 16-bit registers, an inefficient arrangement.

The offset-word pointer, although limiting a programmer to a 64-kbyte segment, is manipulated with only one 16-bit register. By storing an offset value, the word pointer can only be used with a segment register, which provides the address base. The compiler always assumes that the data-segment register stores the base value.

Ideally, pointers should refer to data objects in the current data segment, since a full pointer

Program 3. When variables and procedures are local

```
/* Less optimal */
PROCEDURE P PUBLIC;
  ...
END P;
...
CALL P; /* Long call */
```

```
/* More optimal */
PROCEDURE P;
  ...
END P;
...
CALL P; /* Short call */
```

(a)

```
/* Less optimal */
DECLARE B BYTE EXTERNAL;
...
... B ... /* Long ref */
```

```
/* More optimal */
DECLARE B BYTE;
...
... B ... /* Short ref */
```

(b)

```
/* Less optimal */
DECLARE T (100) WORD;
DECLARE P POINTER;
DECLARE S (1) BASED P,
WORD;
...
P = @T;

DO WHILE S (0) <> 0;
  ...
  P = @S (1);
END;
```

```
/* More optimal */
DECLARE T (100) WORD;
DECLARE W WORD;
DECLARE S BASED W,
WORD;
...
W = .T; /* Safe if T is
local */
DO WHILE S <> 0;
  ...
  W = W + SIZE (S);
END;
```

(c)

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is not required or even desirable in the instance. Instead a word-offset pointer is preferable (Program 3c).

Programmers can help the compiler produce efficient code through subsystems, which in effect are extended segmentation models. A subsystem comprises a group of tightly related modules.

Best of both worlds

Medium and large segmentation models have the important advantage of multiple code and data segments. With subsystems, a programmer can retain the advantage of those models without relinquishing the positive features of small and compact models.

Just as performance benefits arise with references to procedures and variables within the same module, procedures and variables within the same subsystem also help the compiler generate optimal code. In addition, symbols can also be exported from subsystems, in the same fashion that they can be declared public. In fact, exported symbols are really superpublic symbols, since they can be accessed from outside the subsystem.

Program 4. Breaking up is easy

```
$COMPACT (DRIVER HAS ROOT, DATA, IO, UTILS,
  SYMBOL_TABLE, . . .)
$COMPACT (SCANNER HAS READER, TOKENIZER,
  LISTER, PARSER, . . .)
$COMPACT (SEMANTICS HAS DECLARATIONS,
  STATEMENTS, . . .)
$COMPACT (GLOBAL_OPTIMIZER HAS DATA_FLOW,
  CONTROL_FLOW, . . .)
$COMPACT (CODE_GENERATOR HAS,
  REGISTER_ALLOC, INSTR_SELECTOR, . . .)
$COMPACT (LOCAL_OPTIMIZER HAS PEEPHOLE, . . .)
$COMPACT (OBJECT_WRITER HAS DATA_REF,
  PUB_DCL, EXT_REF, . . .)
$COMPACT (CROSS_REF HAS SORT_DCL, SORT_REF,
  PRINT_LIST, . . .)
```

Program 5. A mix of large and small models

```
$LARGE (CEL87 EXPORTS mgerSIN, mgerCOS, mgerTAN)
. . .
mgerSIN: PROCEDURE (X) REAL EXTERNAL;
    DECLARE X REAL;
END mgerSIN;
mgerCOS: PROCEDURE (X) REAL EXTERNAL;
    DECLARE X REAL;
END mgerCOS;
mgerTAN: PROCEDURE (X) REAL EXTERNAL;
    DECLARE X REAL;
END mgerTAN;
. . .
```

Two kinds of subsystems exist: An open subsystem is almost the same as a normal segmentation model, except that it can export names. A closed subsystem resembles a large model, with the exported names exactly like the public names.

The subsystem concept is essentially a logical extension of the regular models of segmentation and lets a programmer restructure a model for the best performance. For example, if a small-model program grows too large for one segment (i.e., bigger than 64 kbytes), a programmer can either switch to a medium model, which is less efficient for procedure calls between modules, or identify a tightly coupled subset of modules.

With the latter approach, modules A, B, and C could form a closed subset of their own, leaving the remaining modules as an open subset. Neither source code nor data structures need be changed, since all data variables remain within the same segment. Moreover, all procedures still use short call and return mechanisms, except those that have been moved to the closed subsystem.

For example, a small-model program can be transformed into one using small subsystems with the definition:

```
$SMALL (Foo HAS A,B,C,; EXPORTS This, That)
```

In that definition, all modules except A, B, and C implicitly belong to the small open subsystem. References to public procedures and variables within the same subsystem are short ones, because the compiler knows that the references are in the same physical segment when the program is executed. However, references from outside the Foo subsystem to the exported names This and That will be long.

Similarly, any application program that uses a large model of segmentation can probably be improved by changing it to a compact-model subsystem. Most programs need more than one module to perform some closely related function: Subsystems enable the programmer to group these modules into the efficient packages

of a smaller model.

For example, consider a compiler consisting of eight major phases: a driver, scanner, semantics processor, global optimizer, code generator, local optimizer, object module writer, and cross-reference lister. The many modules in each phase communicate with one another through public procedures and variables that are declared in the driver. Moreover, each phase is invoked by the driver, using a procedure call.

If the compiler uses a large model, all the intermodule references will be inefficient, even those within the same phase. However, by defining a compact-model subsystem for each phase, the whole system's performance improves (Program 4).

Normally, all modules of a PL/M-86 program must be compiled with the same segmentation model. However, the compiler can mix small subsystems with compact and large ones. For example, consider a large-model package, called the common elementary functions library, that supports the 8087 math coprocessor. Without subsystems, any module that refers to a procedure in the library must also be compiled as a large model, despite that model's inherent inefficiency.

With subsystems, however, the library can be accessed through a more efficient small model, with the library procedures defined as exported from a closed large subsystem. Therefore, to access the sine, cosine, and tangent functions of the library, the programmer need only declare those library procedures as exported (Program 5). The compiler then knows that it must generate long calls to these procedures no matter what model of segmentation is being used for the current module.□

How useful?	Circle
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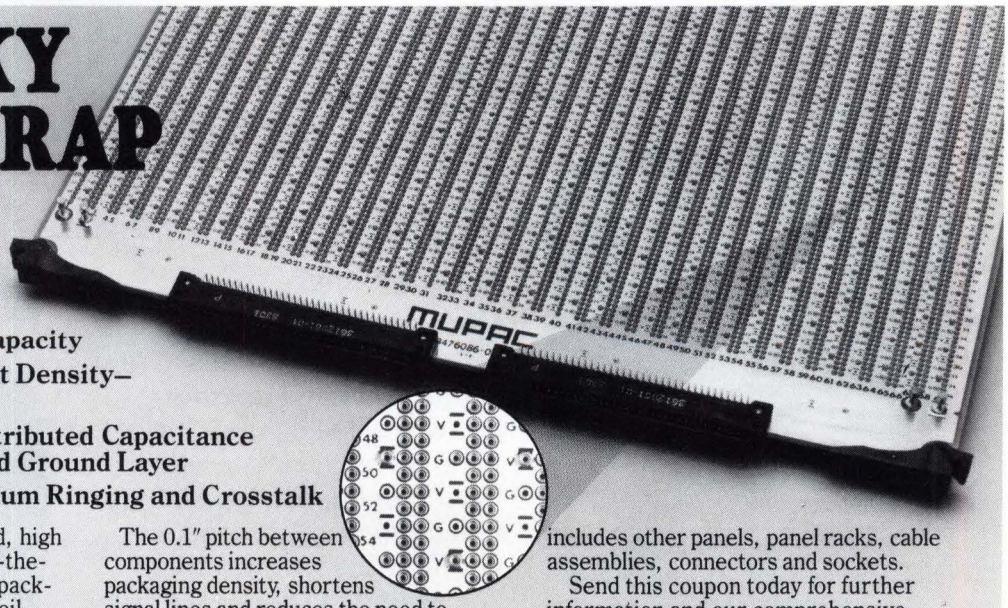

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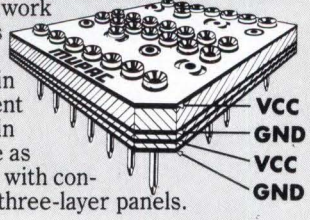

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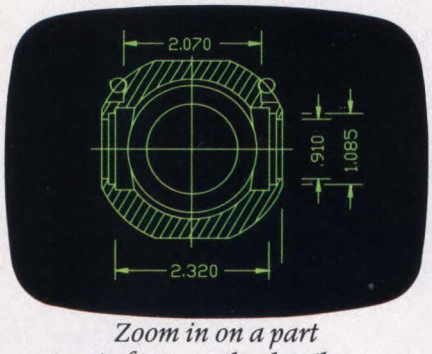

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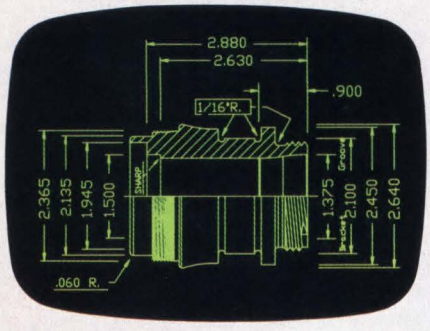

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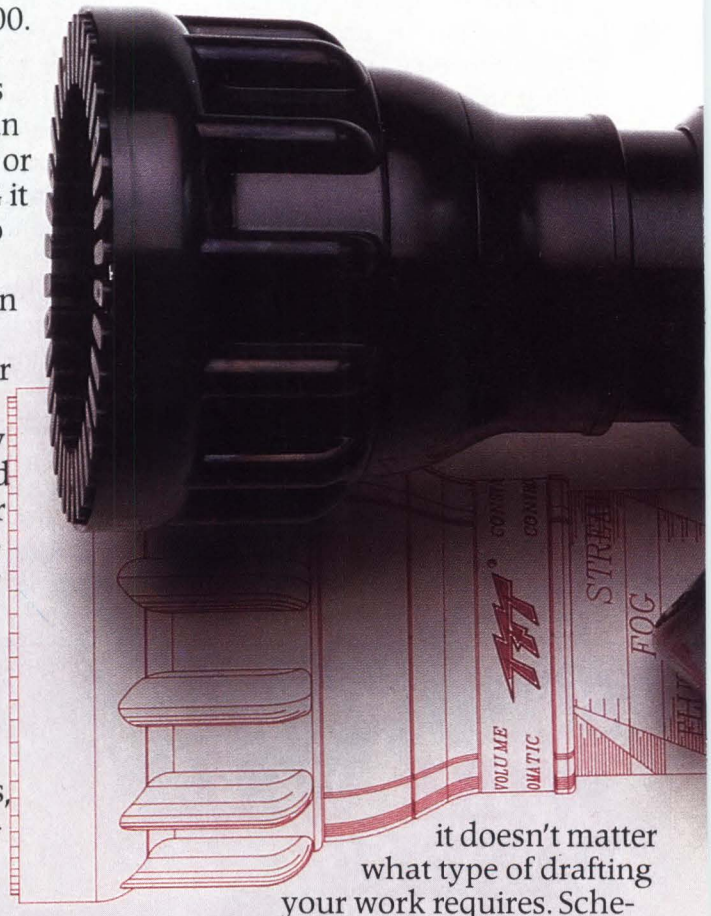

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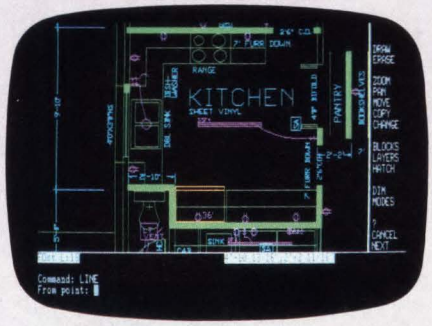

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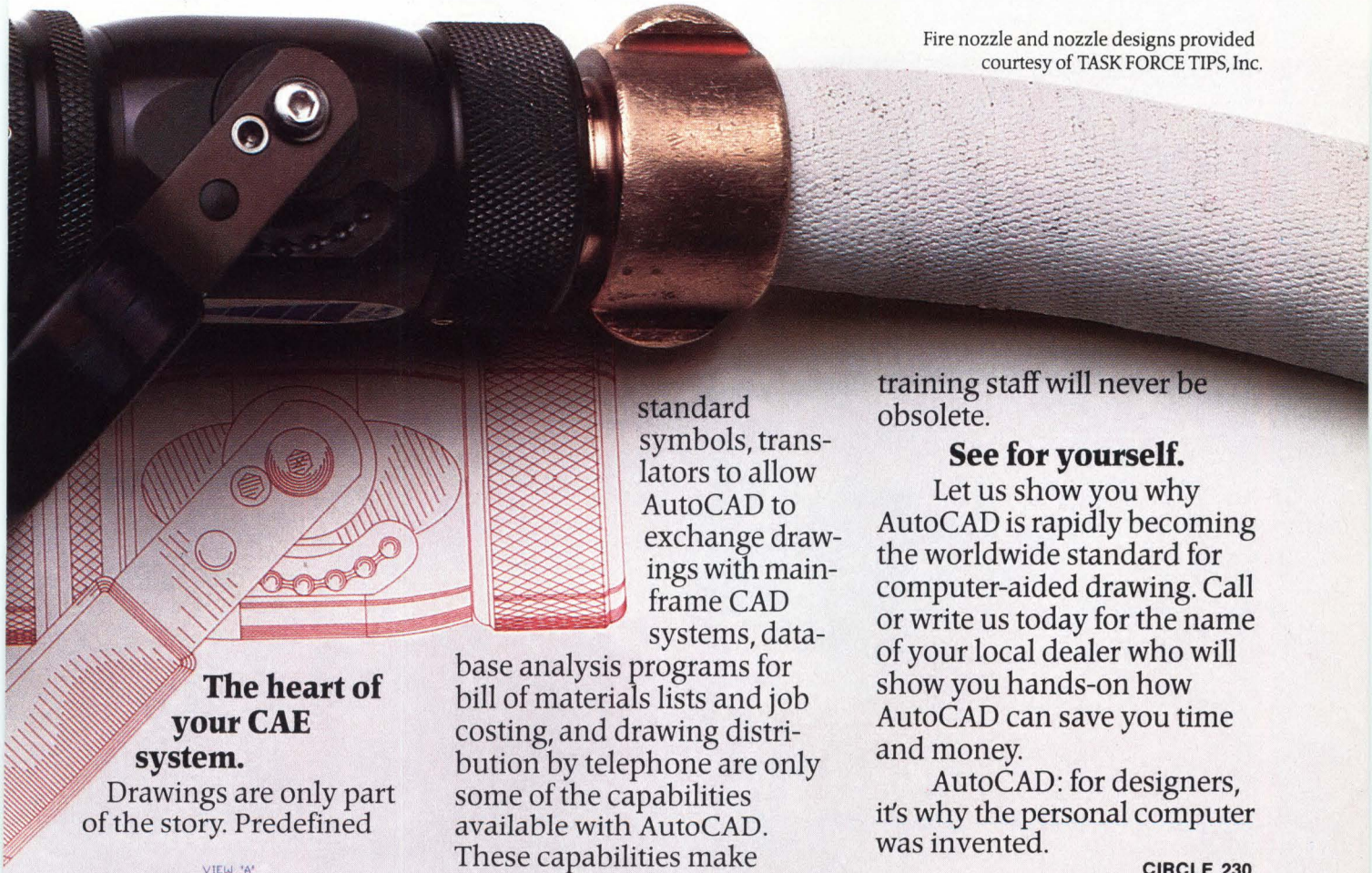

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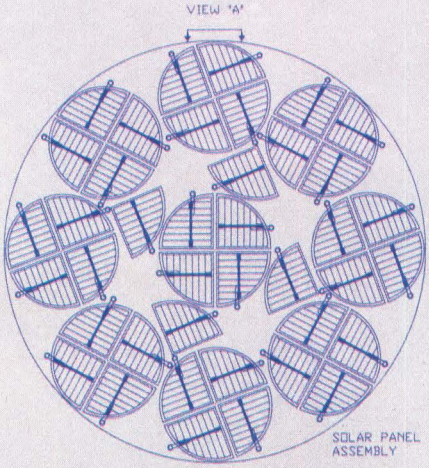

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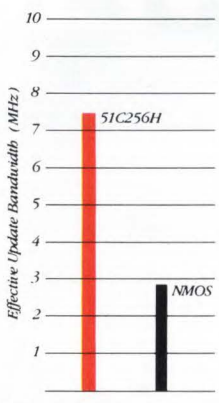

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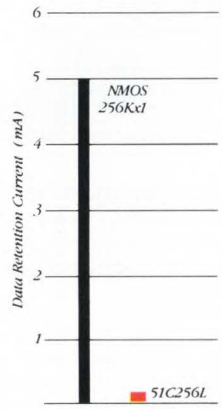

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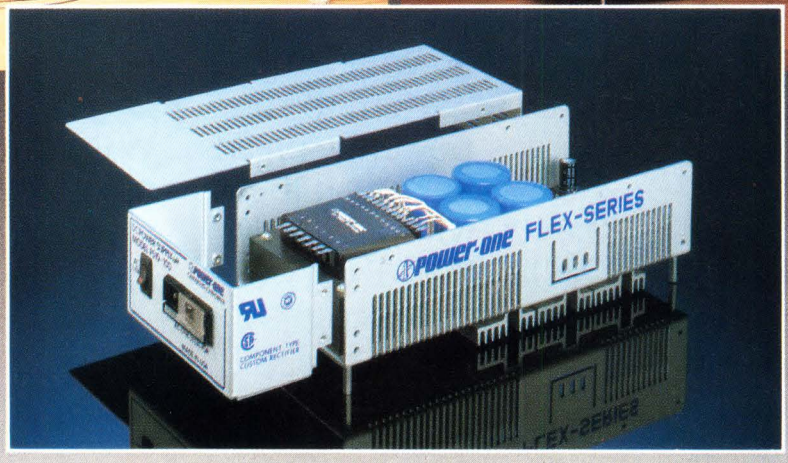

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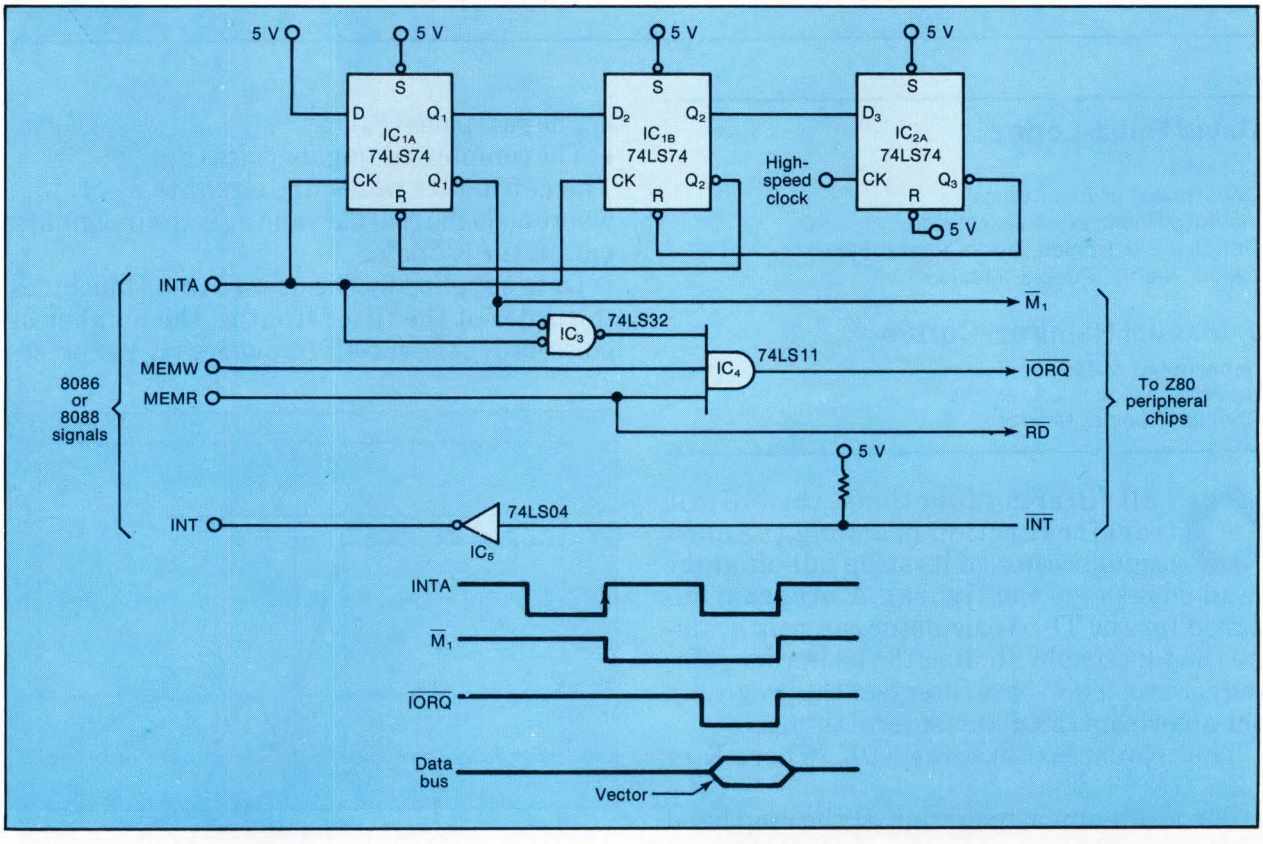

Five chips can handle interrupts between an 8086- or 8088-based processor system and peripheral chips designed for the Z80 processor. Data is transferred during the second of two interrupt acknowledgement cycles.

stable condition in the Z80's daisy-chained interrupt priority structure, the circuit has been designed so that an interrupt status signal cannot change when the Machine Cycle 1 line, $\overline{M_1}$, is low.)

An active-low interrupt request signal ($\overline{INT}$) from the support chip is sent to the CPU system through IC_5, an inverter, to indicate the start of the cycle. The interrupt acknowledge line (INTA) from the 8086 or 8088 system is connected to the clock inputs of dual flip-flops IC_{1A} and IC_{1B}, as well as to an OR gate, IC_3. Therefore, when the first INTA pulse ends, $\overline{M_1}$ goes low. At the start of the second pulse, the I/O Request line ($\overline{IORQ}$) also goes low. The requesting device with the highest priority is allowed to place its interrupt vector on the data bus and set an internal latch that indicates the interrupt is under service.

At the end of the second pulse, the Q_2 output from flip-flop IC_{1B} goes low, resetting IC_{1A}, as well as $\overline{M_1}$ and $\overline{IORQ}$. A third flip-flop, IC_{2A}, samples the Q_2 output from IC_{1B} and resets the latter device at the end of the cycle. The length of the reset pulse is determined by the frequency of the clock used by IC_{2A}.

TI-59 program finds elliptic transfer function for low-pass filters

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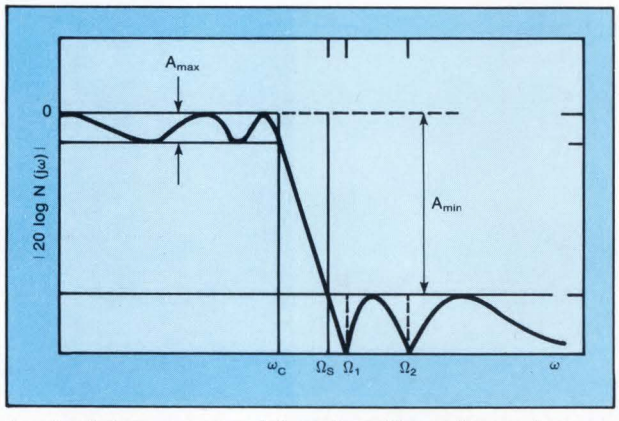
Of all filtering functions, the elliptic transfer function is among the most useful because of its steep fall-off at the band edges (see the figure). A program designed for the TI-59 calculator can help evaluate the function by finding the odd-order poles and zeros of a low-pass filter (see the program). The algorithm calculates several things:

- The transmission zeros—ΩK, where $K = 1, 2, \ldots, (N-1)/2$;
- The minimum attenuation at the stop band with respect to the maximum value at the pass band A_{min} expressed in dB;
- The real poles (P_0);
- The complex-conjugate poles (P_K)

The conjugate poles are equal to $\alpha_K + j\beta_K$, where α_K is the real part and β_K is the imaginary part of the Kth pole.

Data supplied by the user (Table 1) includes the order of the filter (that is, the number of poles, or N); the cut-off frequency (ω_C), express-



A calculator program determines the poles and zeros of an elliptic transfer-function filter, one characterized by its steep fall-off at the band edges.

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ed in radians/s; the stop-band frequency (Ω_S), expressed in radians/s; and either the reflection coefficient (ρ), shown as a percentage, or the maximum attenuation of the pass-band ripple in dB (A_{max}).

The last two of those parameters are related to each other by the formula:

$$A_{max} = -10 \log\left[1 + \left(\frac{\rho}{100}\right)^2\right]$$

Once the poles and the zeros have been found, the transfer function, $H_{(S)}$, is found with the help of the formula:

$$H_{(S)} = \frac{(S^2+\Omega_1^2)(S^2+\Omega_1^2)\ldots(S^2+\Omega^2_{(N-1)/2})}{(S+P_0)(S+P_1)(S+P_1^*)\ldots(S+P_{(N-1)/2})(S+P^*_{(N-1)/2})}$$

The results obtained with the calculator program for a normalized low-pass filter—that is, one with a ω_C of 1—compare favorably with those found in other filter tables (Table 2). Values other than unity can be used. The program, which can be recorded on a magnetic card, can evaluate the elliptic transfer filtering function up to the 21st order.

*S. Darlington, "Simple Algorithms for Elliptic Filters and Generalizations Thereof," *IEEE Transactions on Circuits and Systems*, Vol. CAS-25, No. 12, pp. 975-980, 1978.

Table 1. User instructions for low-pass elliptic transfer function

Step	Procedure	Enter	Press			Display
1	Filter order	n	A			n
2	Pass-band cut-off frequency (rad/s)	ω_c	B			ω_c
3	Stop-band frequency (rad/s)	Ω_s	C			Ω_s
4a	Either reflection coefficient (%)	ρ	D			0
	or					
4b	passband ripple (dB)	A_{max}	E			0
5	Compute transmission zeros, Ω_k $k = 1,2,\ldots,(n-1)/2$		R/S			Ω_k
	Repeat step 5 for each value of k until 0 appears in the display.					
6	Compute stop-band attenuation, A_{min}		2nd	C′		A_{min}
7	Compute real pole, P_o	0	2nd	D′		P_o
8a	Compute k^{th} pole, real part	k	2nd	D′		Re (P_k)
8b	Compute k^{th} pole, imaginary part		2nd	E′		Im (P_k)
	Repeat steps 8a and 8b for each value of k					
	$k = 1,\ldots,(n-1)/2$					

Table 2. Results of calculation for a low-pass filter

Input	Output	
	Zeros	Real and complex poles
$n = 5$	$\Omega_1 = 1.465436966$	
$\omega_c = 1$	$\Omega_2 = 1.656220908$	
$\Omega_s = 1.414213562$	$\Omega_3 = 2.165997414$	$P_o = -0.3186089933$
$\rho = 50\%$	$\Omega_4 = 3.944466518$	$P_1 = -0.2095320012 + J\ 0.6875524703$
	$A_{min} = 51.4064495$ dB	$P_2 = -0.0582836518 + J\ 0.991367843$

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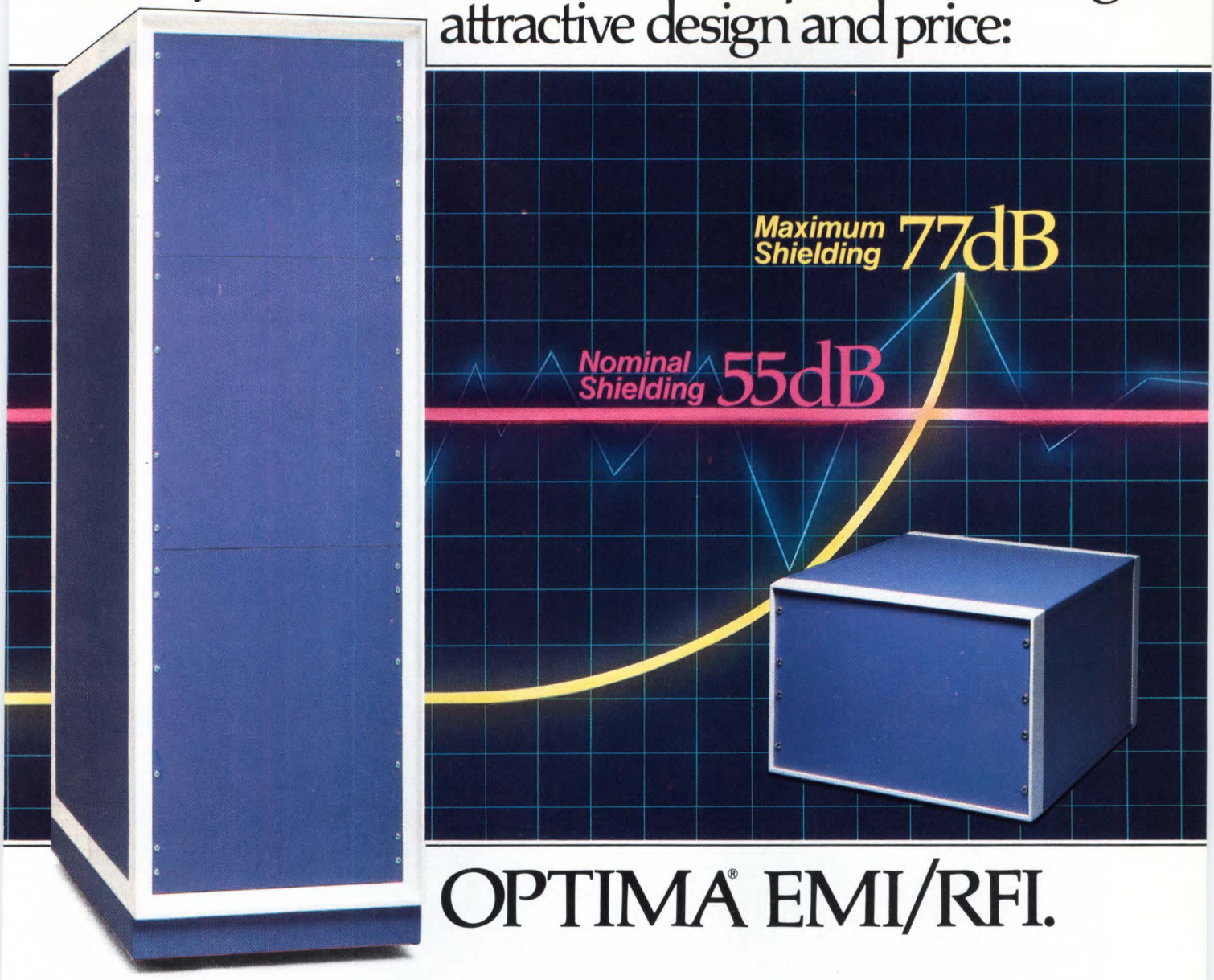

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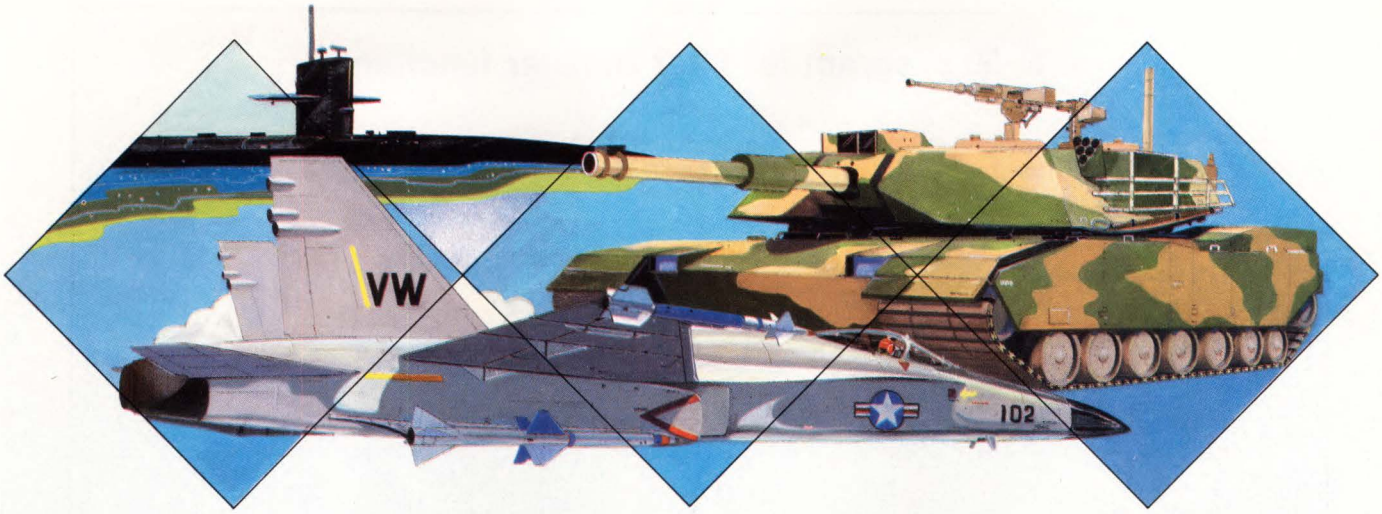
CIRCLE 107

TI-59 program for filter transfer function

```
000  76 LBL    065  43 RCL    130  95  =     195  04  4     260  95  =
001  11  A     066  08  08    131  39 COS    196  04  4     261  34 ΓX
002  42 STO    067  91 R/S    132  55  ÷     197  42 STO    262  85  +
003  10  10    068  76 LBL    133  43 RCL    198  54  54    263  43 RCL
004  04  4     069  14  D     134  15  15    199  04  4     264  01  01
005  42 STO    070  55  ÷     135  95  =     200  42 STO    265  35 1/X
006  02  02    071  01  1     136  35 1/X    201  02  02    266  95  =
007  01  1     072  00  0     137  76 LBL    202  02  2     267  65  ×
008  02  2     073  00  0     138  34 ΓX     203  45 Y^x    268  43 RCL
009  42 STO    074  95  =     139  71 SBR    204  53  (     269  46  46
010  59  59    075  33 X²     140  61 GTO    205  43 RCL    270  95  =
011  43 RCL    076  94 +/-    141  97 DSZ    206  10  10    271  71 SBR
012  10  10    077  85  +     142  02  02    207  75  -     272  24 CE
013  91 R/S    078  01  1     143  34 ΓX     208  01  1     273  65  ×
014  76 LBL    079  95  =     144  72 ST*    209  54  )     274  43 RCL
015  12  B     080  28 LOG    145  56  56    210  65  ×     275  45  45
016  42 STO    081  65  ×     146  35 1/X    211  43 RCL    276  95  =
017  07  07    082  01  1     147  65  ×     212  15  15    277  71 SBR
018  91 R/S    083  00  0     148  43 RCL    213  45 Y^x    278  24 CE
019  76 LBL    084  95  =     149  09  09    214  43 RCL    279  65  ×
020  13  C     085  94 +/-    150  95  =     215  10  10    280  43 RCL
021  42 STO    086  76 LBL    151  01  1     216  95  =     281  44  44
022  08  08    087  15  E     152  44 SUM    217  42 STO    282  65  ×
023  55  ÷     088  55  ÷     153  57  57    218  43  43    283  02  2
024  43 RCL    089  01  1     154  01  1     219  76 LBL    284  95  =
025  07  07    090  00  0     155  44 SUM    220  22 INV    285  55  ÷
026  95  =     091  95  =     156  56  56    221  71 SBR    286  43 RCL
027  34 ΓX     092  22 INV    157  43 RCL    222  75  -     287  43  43
028  42 STO    093  28 LOG    158  57  57    223  72 ST*    288  95  =
029  11  11    094  75  -     159  32 X:T    224  54  54    289  35 1/X
030  43 RCL    095  01  1     160  43 RCL    225  32 X:T    290  71 SBR
031  08  08    096  95  =     161  10  10    226  01  1     291  24 CE
032  65  ×     097  34 ΓX     162  22 INV    227  44 SUM    292  45 Y^x
033  43 RCL    098  42 STO    163  67  EQ     228  54  54    293  43 RCL
034  07  07    099  01  01    164  35 1/X    229  32 X:T    294  10  10
035  95  =     100  00  0     165  00  0     230  97 DSZ    295  35 1/X
036  34 ΓX     101  70 RAD    166  91 R/S    231  02  02    296  95  =
037  42 STO    102  01  1     167  76 LBL    232  22 INV    297  42 STO
038  09  09    103  06  6     168  17 B'     233  43 RCL    298  53  53
039  43 RCL    104  42 STO    169  43 RCL    234  01  01    299  43 RCL
040  11  11    105  56  56    170  10  10    235  33 X²     300  06  06
041  76 LBL    106  00  0     171  42 STO    236  65  ×     301  91 R/S
042  85  +     107  42 STO    172  03  03    237  43 RCL    302  76 LBL
043  33 X²     108  57  57    173  01  1     238  47  47    303  19 D'
044  42 STO    109  76 LBL    174  07  7     239  45 Y^x    304  65  ×
045  58  58    110  35 1/X    175  42 STO    240  04  4     305  89  π
046  33 X²     111  04  4     176  56  56    241  95  =     306  95  =
047  75  -     112  42 STO    177  76 LBL    242  85  +     307  55  ÷
048  01  1     113  02  02    178  45 Y^x    243  01  1     308  43 RCL
049  95  =     114  01  1     179  73 RC*    244  95  =     309  10  10
050  34 ΓX     115  04  4     180  56  56    245  35 1/X    310  95  =
051  85  +     116  42 STO    181  65  ×     246  28 LOG    311  42 STO
052  43 RCL    117  48  48    182  43 RCL    247  65  ×     312  02  02
053  58  58    118  43 RCL    183  09  09    248  01  1     313  00  0
054  95  =     119  57  57    184  95  =     249  00  0     314  42 STO
055  72 ST*    120  65  ×     185  91 R/S    250  95  =     315  01  01
056  59  59    121  89  π     186  02  2     251  94 +/-    316  36 PGM
057  32 X:T    122  95  =     187  44 SUM    252  42 STO    317  05  05
058  01  1     123  55  ÷     188  56  56    253  06  06    318  17 B'
059  44 SUM    124  53  (     189  97 DSZ    254  43 RCL    319  65  ×
060  59  59    125  02  2     190  03  03    255  01  01    320  43 RCL
061  32 X:T    126  65  ×     191  45 Y^x    256  33 X²     321  53  53
062  97 DSZ    127  43 RCL    192  91 R/S    257  35 1/X    322  95  =
063  02  02    128  10  10    193  76 LBL    258  85  +     323  42 STO
064  85  +     129  54  )     194  18 C'     259  01  1     324  50  50
```

(continued on p. 240)

Standard MIL-SPEC DC/DC CONVERTERS



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5/12/15/24/28 VDC @
30/12.5/10/6.3/5.3A†
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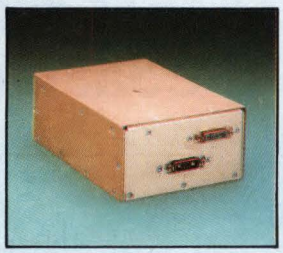
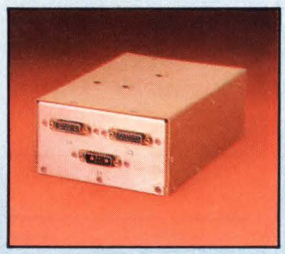


300W Single
5/12/15/24/28 VDC @
60/25/20/12.5/10.7A†
7″L x 5″W x 2.625″H

180W Dual
±12/15/24/28 VDC @
7.5/6/3.8/3.2A†
7″L x 4.5″W x 2.625″H



175W Triple
5 VDC @ 20A &
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(continued from p. 238)

TI-59 program for filter transfer function

```
325  32 X:T    353  76 LBL    381  85  +     409  42 STO    437  22 INV
326  65  ×     354  10 E'     382  01  1     410  04  04    438  44 SUM
327  43 RCL    355  43 RCL    383  95  =     411  36 PGM    439  52  52
328  53  53    356  51  51    384  34 ΓX     412  04  04    440  92 RTN
329  95  =     357  65  ×     385  85  +     413  10 E'     441  76 LBL
330  42 STO    358  43 RCL    386  43 RCL    414  36 PGM    442  61 GTO
331  51  51    359  11  11    387  05  05    415  04  04    443  42 STO
332  05  5     360  95  =     388  95  =     416  17 B'     444  49  49
333  42 STO    361  91 R/S    389  92 RTN    417  73 RC*    445  35 1/X
334  00  00    362  76 LBL    390  76 LBL    418  52  52    446  85  +
335  01  1     363  75  -     391  54  )     419  65  ×     447  43 RCL
336  05  5     364  42 STO    392  43 RCL    420  02  2     448  49  49
337  42 STO    365  55  55    393  50  50    421  95  =     449  95  =
338  52  52    366  35 1/X    394  42 STO    422  35 1/X    450  55  ÷
339  76 LBL    367  85  +     395  01  01    423  42 STO    451  02  2
340  53  (     368  43 RCL    396  43 RCL    424  03  03    452  95  =
341  71 SBR    369  55  55    397  51  51    425  00  0     453  55  ÷
342  54  )     370  95  =     398  42 STO    426  42 STO    454  73 RC*
343  97 DSZ    371  55  ÷     399  02  02    427  04  04    455  48  48
344  00  00    372  02  2     400  36 PGM    428  36 PGM    456  95  =
345  53  (     373  95  =     401  05  05    429  04  04    457  32 X:T
346  43 RCL    374  34 ΓX     402  15  E     430  13  C     458  01  1
347  50  50    375  92 RTN    403  43 RCL    431  42 STO    459  22 INV
348  65  ×     376  76 LBL    404  50  50    432  50  50    460  44 SUM
349  43 RCL    377  24 CE     405  42 STO    433  32 X:T    461  48  48
350  11  11    378  42 STO    406  03  03    434  42 STO    462  32 X:T
351  95  =     379  05  05    407  43 RCL    435  51  51    463  92 RTN
352  91 R/S    380  33 X²     408  51  51    436  01  1
```

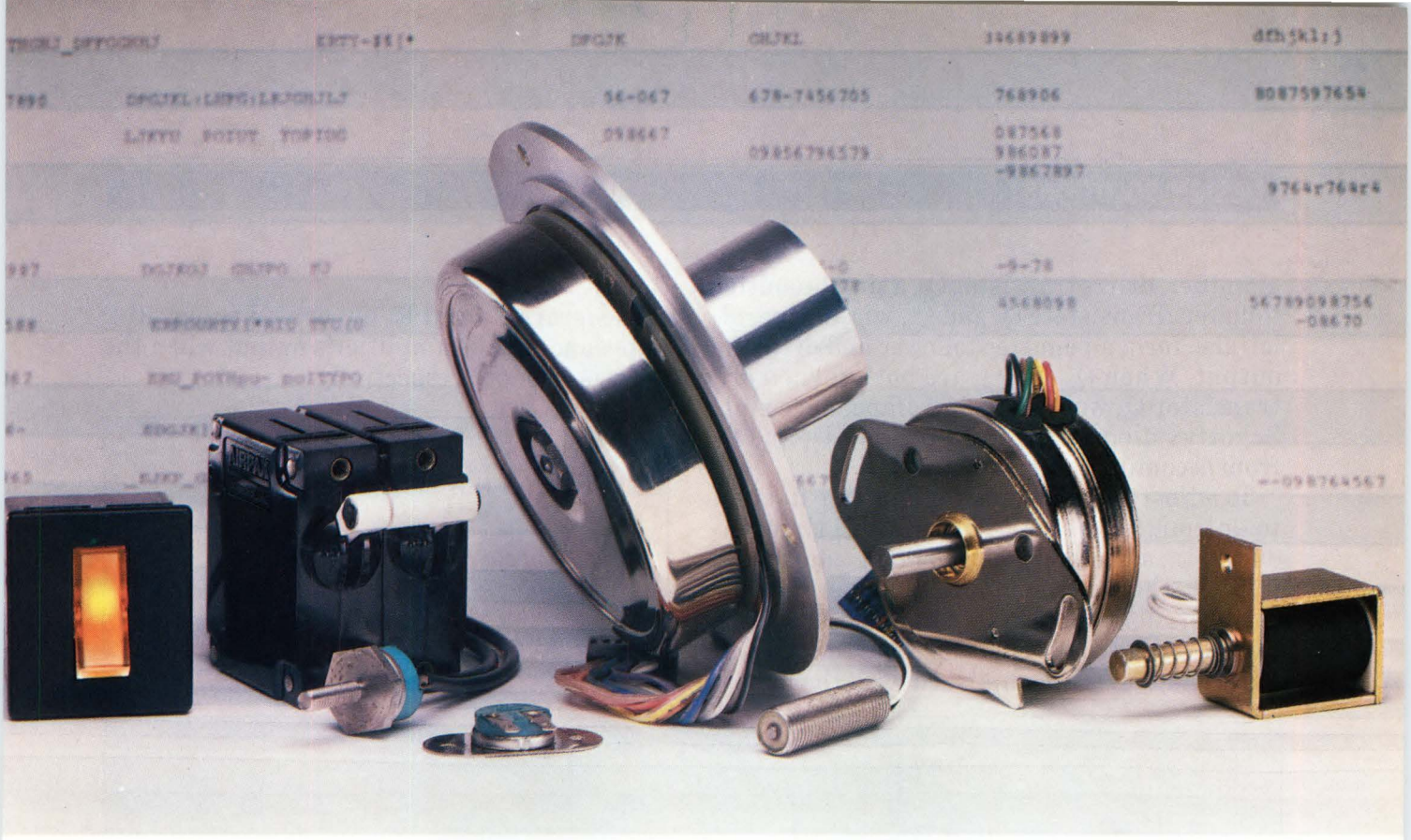
Five-transistor amplifier boosts fast pulses into 50-Ω coaxial cable

M.U. Khan
Manager of Research and Development
Systronics
89-02, Naroda Industrial Area, Naroda-382 330,
Ahmedabad District, India

A simple five-transistor pulse amplifier delivers 5-V pulses into a 50-Ω load, with rise times of just 2.6 ns and fall times of 3.5 ns, matching the performance of more costly circuits containing more parts. Simply by varying the supply voltage over a range of 6 to 14 V and adjusting the circuit's off-board attenuator, the pulse amplitude can be reduced to as little as 100 mV.

The circuit (see the figure) works from dc to 50 MHz and will deliver pulses as short as 10 ns. It is driven by a TTL signal through a 740S00 quad Schottky NAND gate, IC_A through IC_D. If, however, only an ECL-level signal is available, a level translator, such as the MC10125, can be substituted for the 74S00.

Transistor Q_1, wired as a common-emitter



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amplifier, drives transistor Q_2, a simple emitter follower. Transistors Q_3 and Q_4, wired in parallel, also form an emitter follower and drive the output. When Q_3 and Q_4 are both turned off, transistor Q_5 works as a low-impedance sink. Schottky diodes D_1 and D_2 prevent Q_1 and Q_5 from becoming saturated.

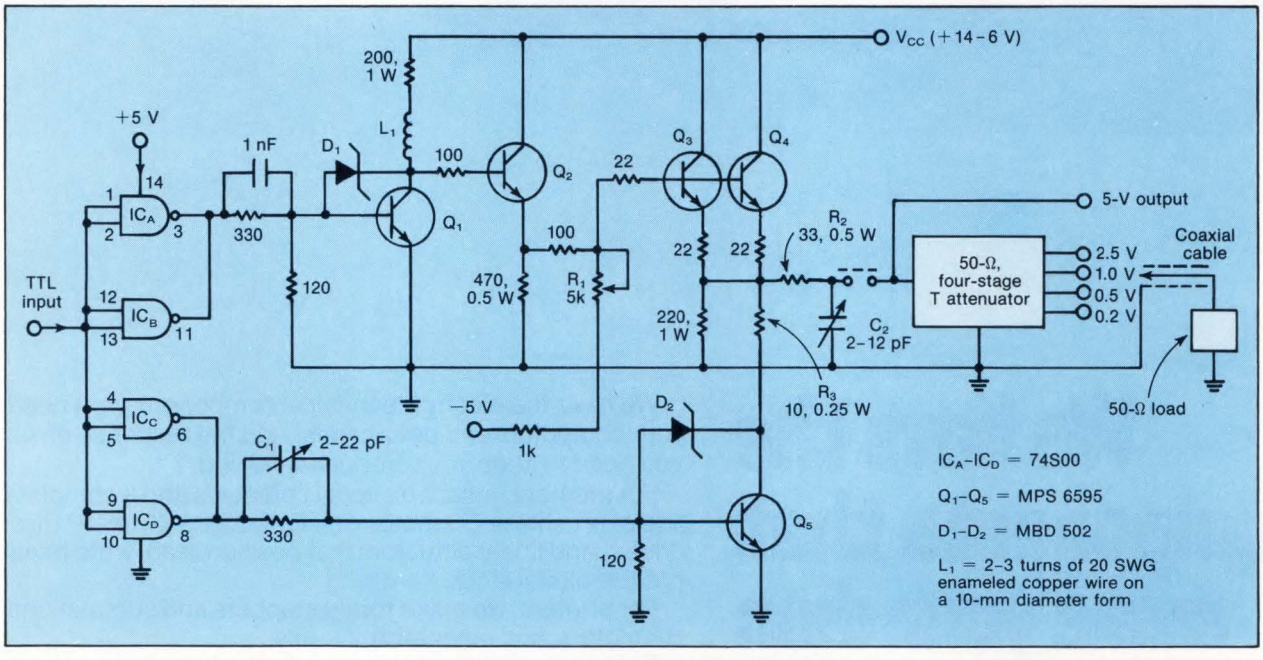
To adjust the circuit, potentiometer R_1 is set to optimize the output pulse's fall time. Inductor L_1, a peaking coil, should be adjusted to improve the rise time to within a permissible 5% overshoot. Likewise, capacitor C_1 can be varied to control preshooting. Further output pulse shaping is accomplished with the help of capacitor C_2.

Resistors R_2 and R_3 ensure a proper 50-Ω impedance at the amplifier's output when the pulse is on or off, respectively.

Winner for November 15, 1984

Pseudo-sine-wave circuit generates FSK tones without discontinuities

Mike Huddleston, Senior Project Engineer, Scientific-Atlanta Inc., MS ATL 5-A, PO Box 105038, Atlanta, Ga.



Transistors Q_3 and Q_4, connected in parallel, form the output emitter follower of a simple yet fast pulse amplifier. The circuit handles repetition rates as high as 50 MHz and transition times of about 3 ns.

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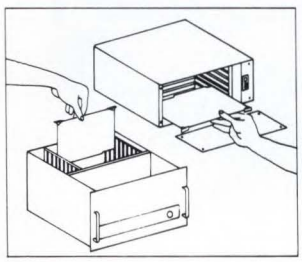

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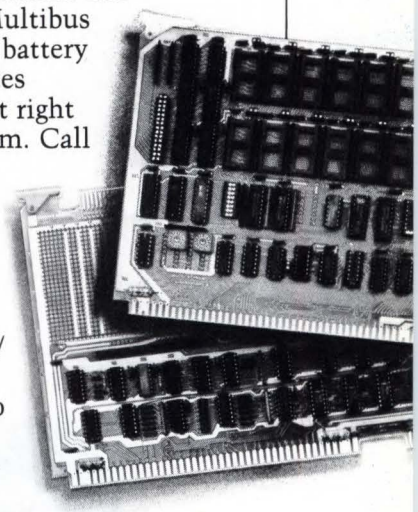

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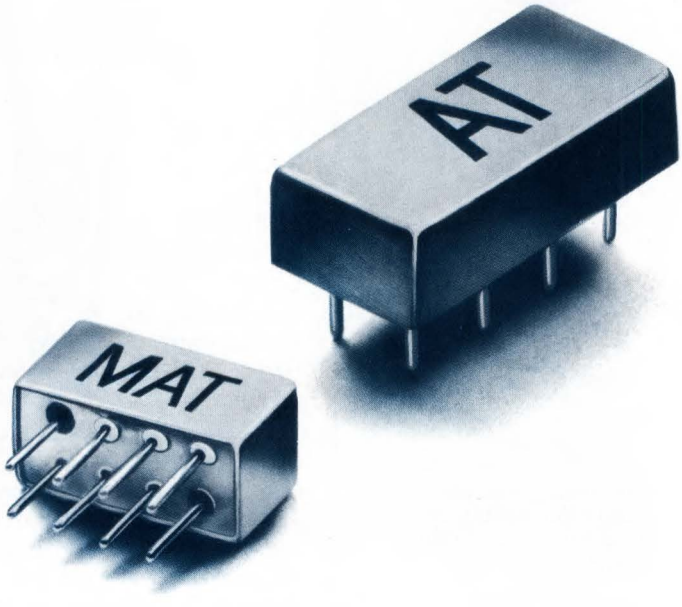

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AT-6	MAT-6	6
—	MAT-9	9
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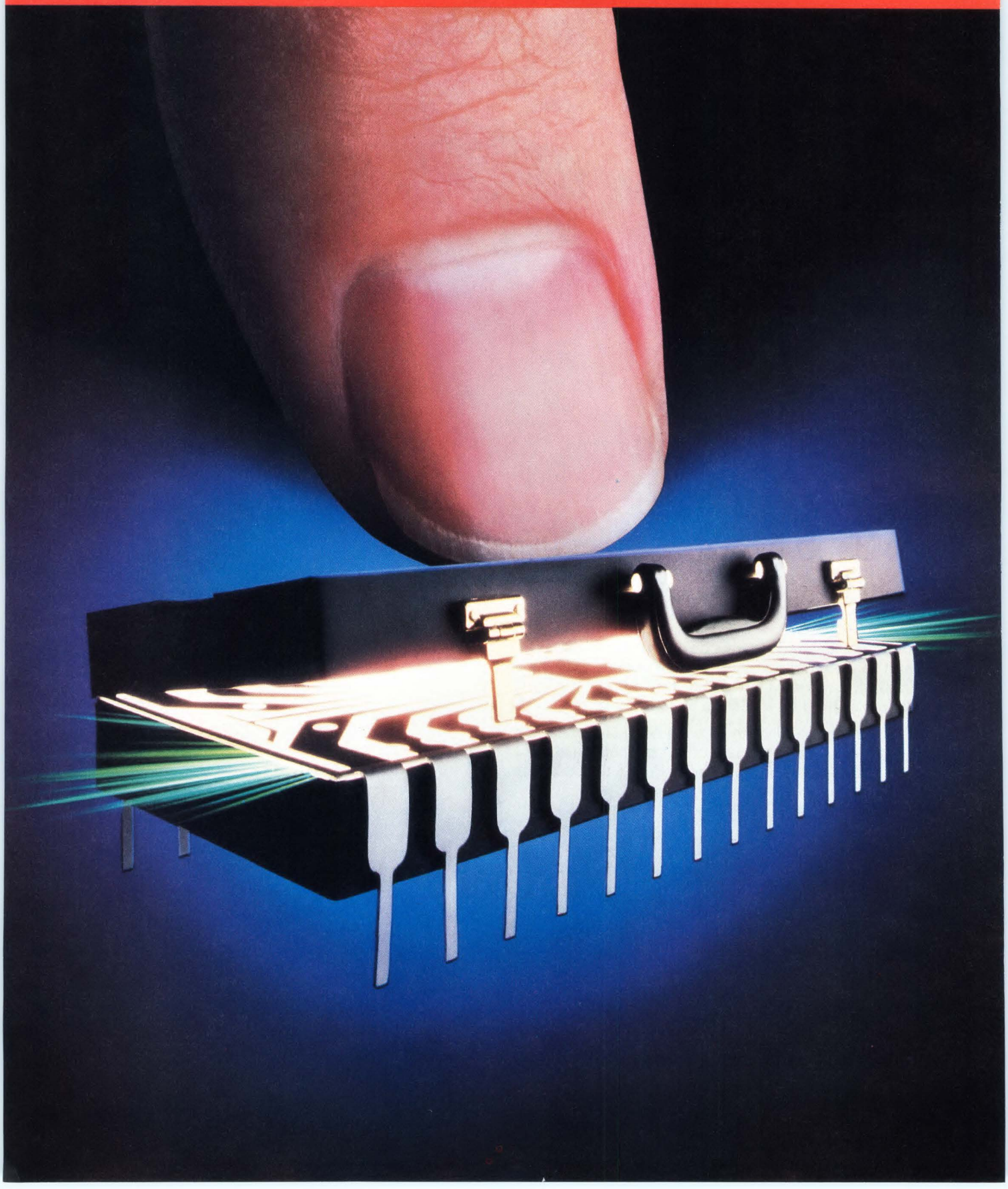

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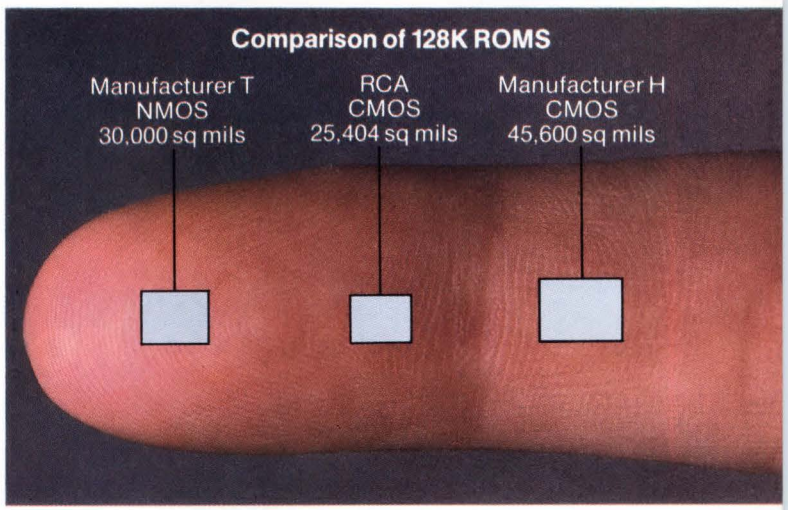

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- Factory Automation
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- Power
- Software
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- DE: Design Entry
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- IFD: Ideas for Design
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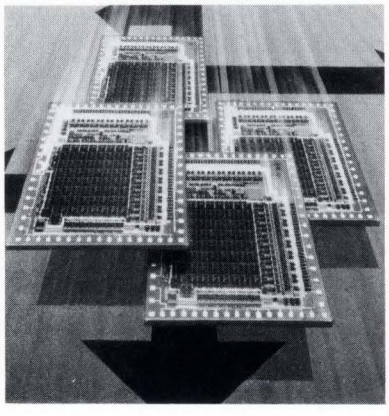

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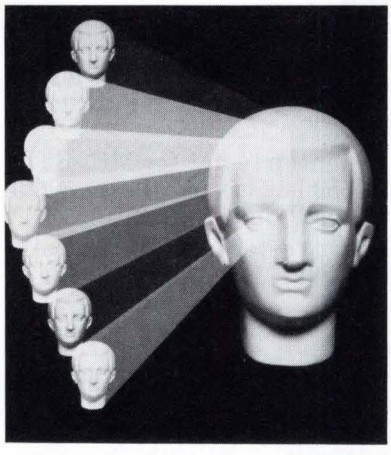

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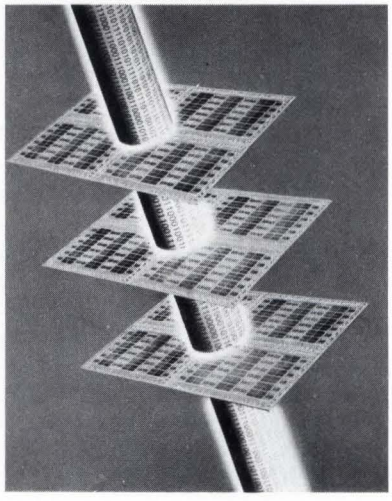

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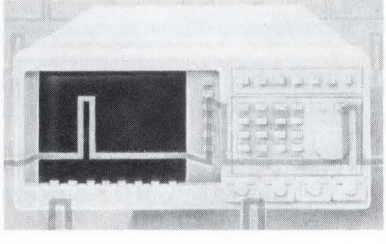

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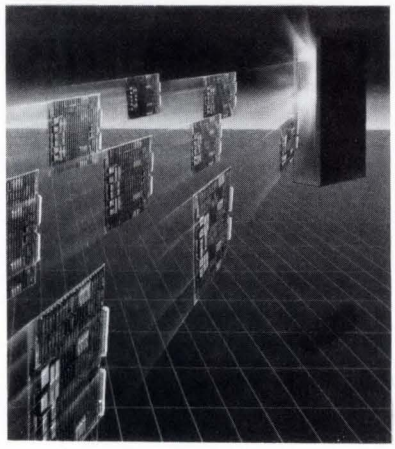

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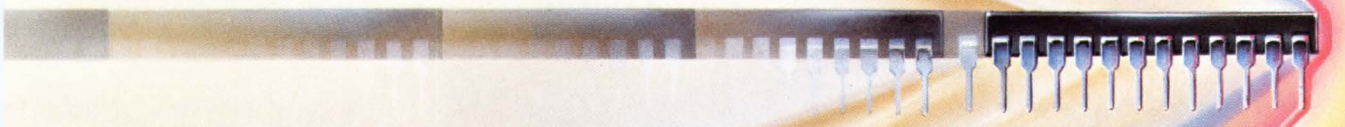

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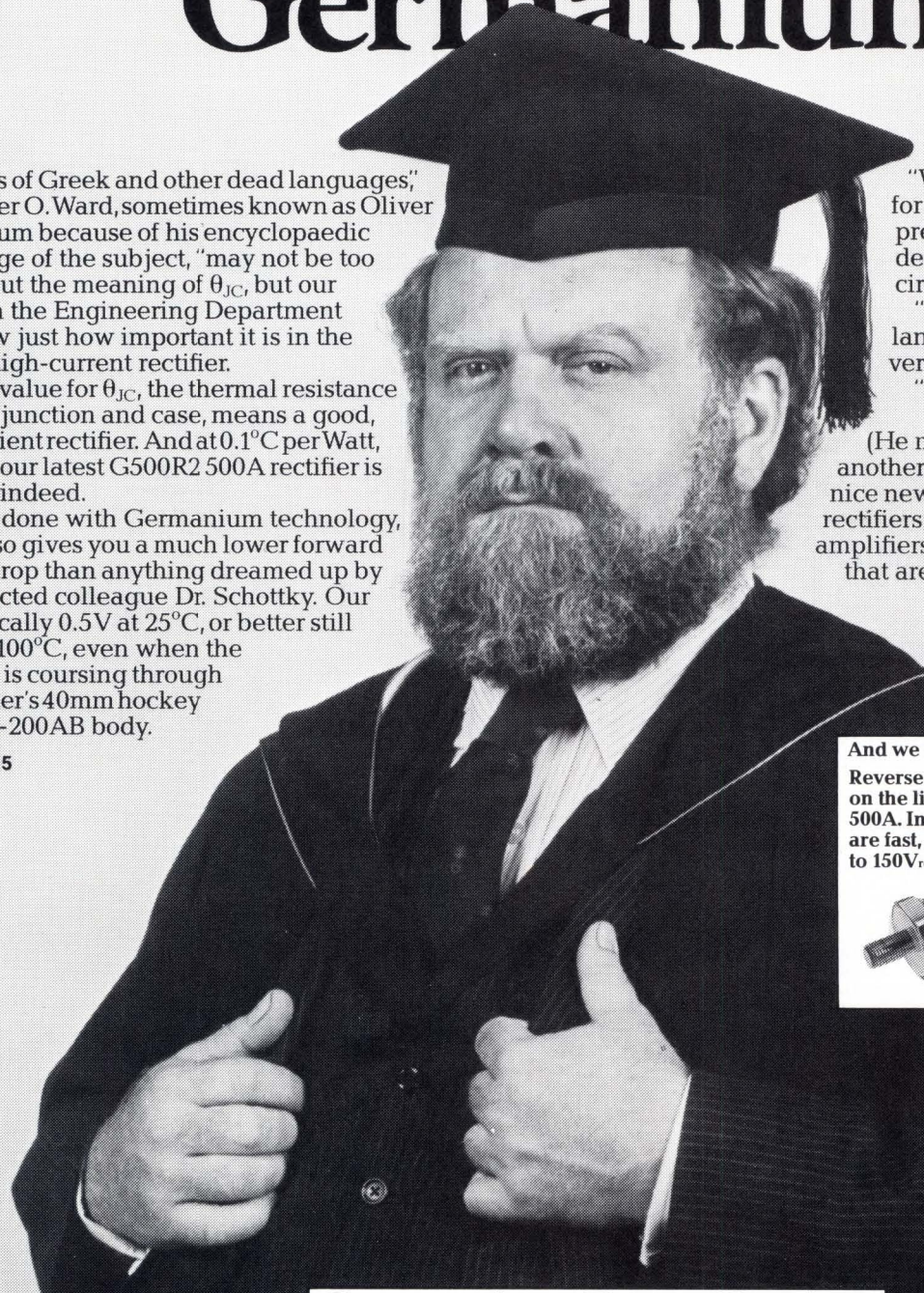

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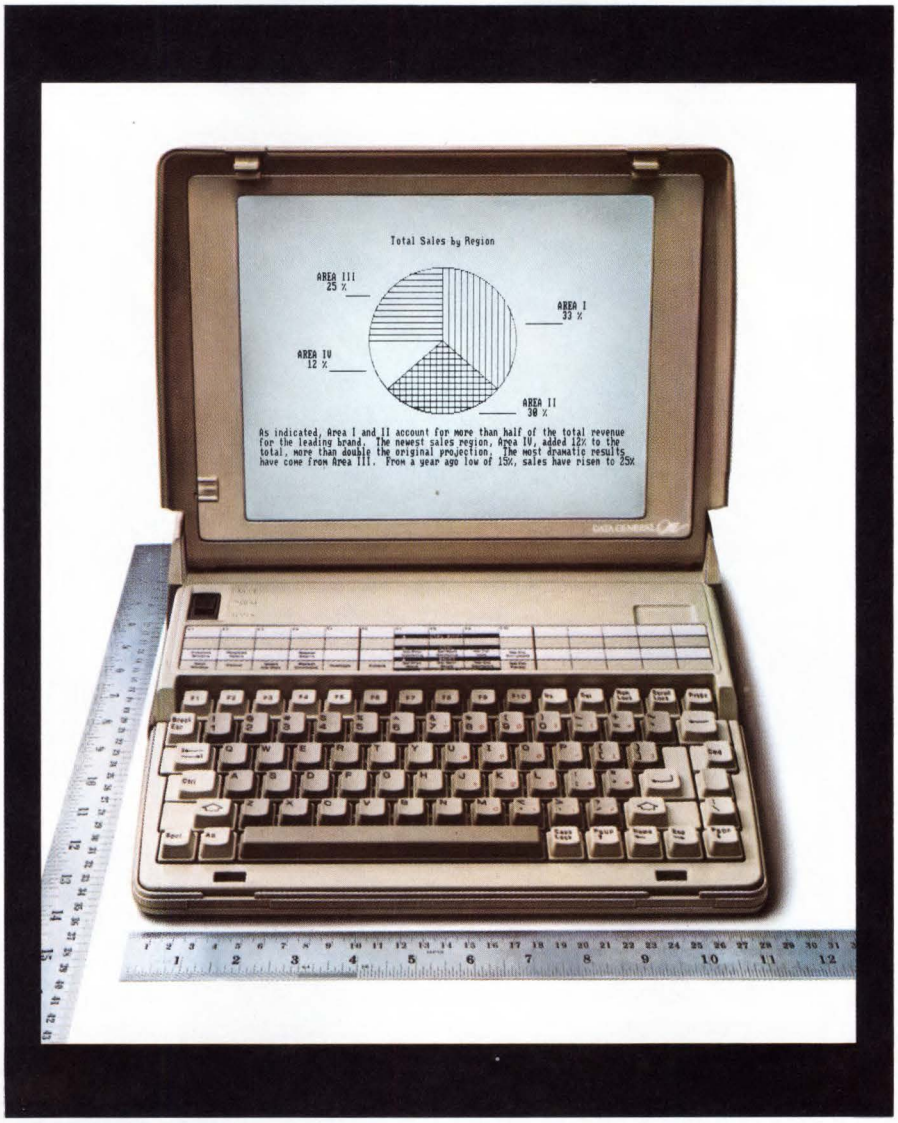

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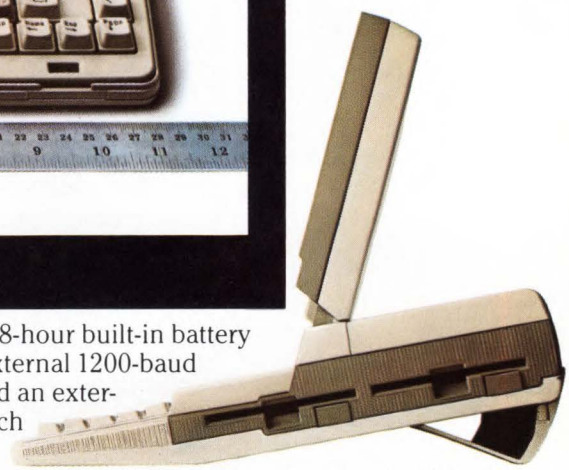

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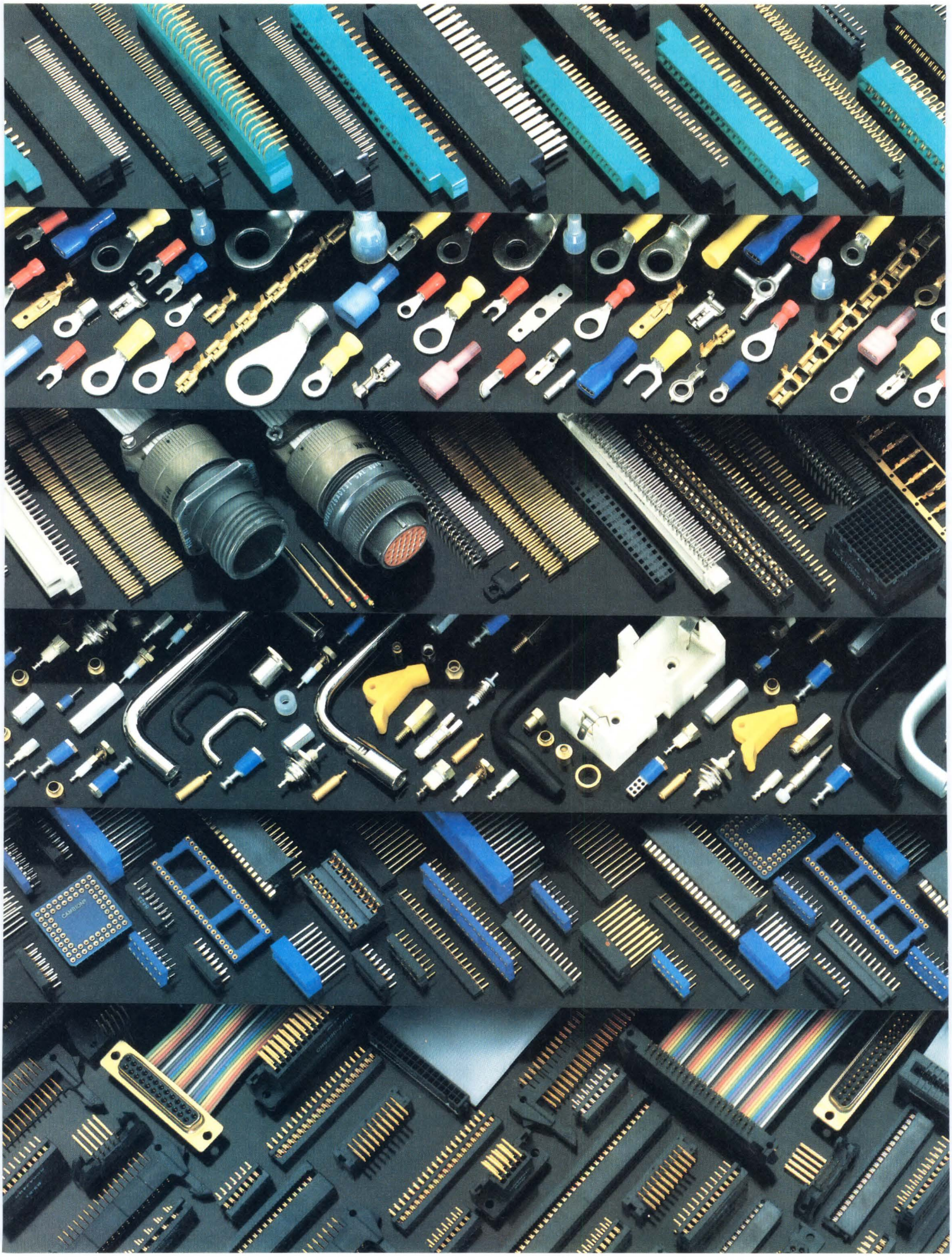

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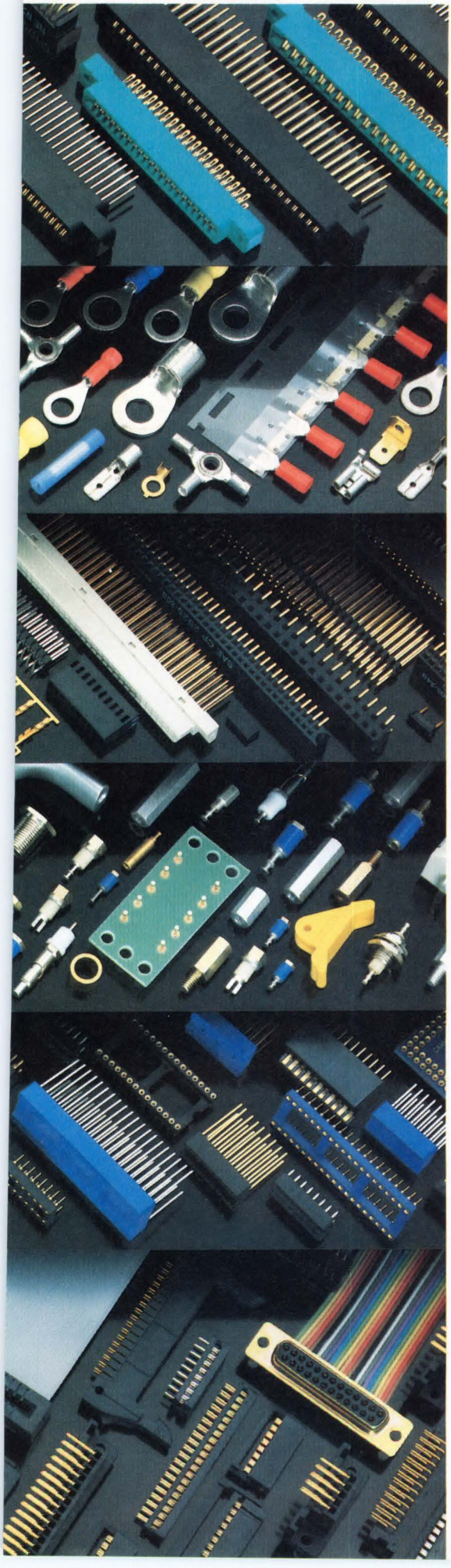

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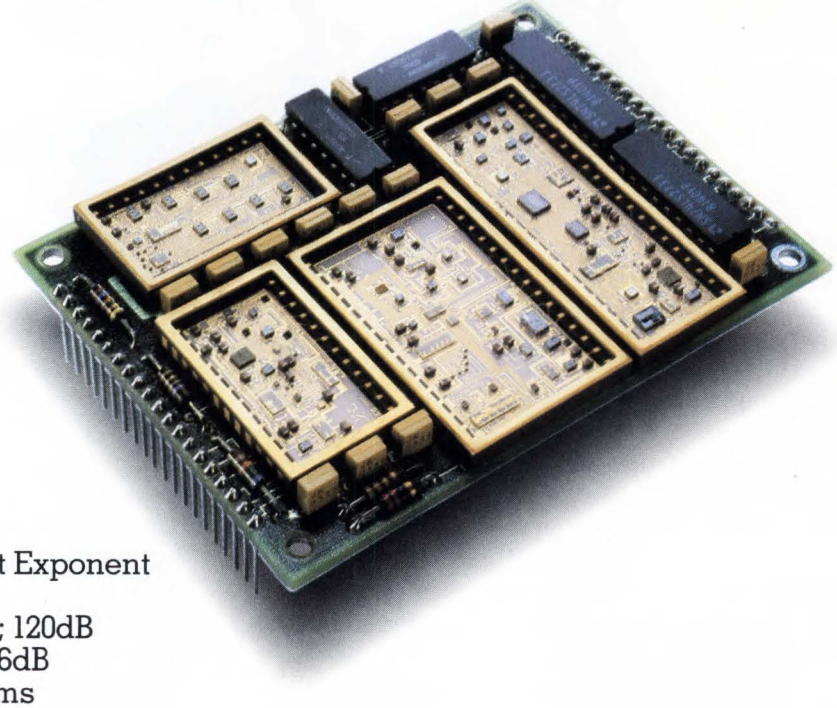

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Absolute Noise Floor: 60μV rms

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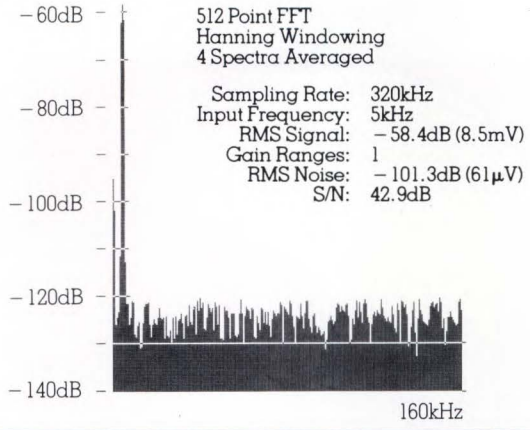

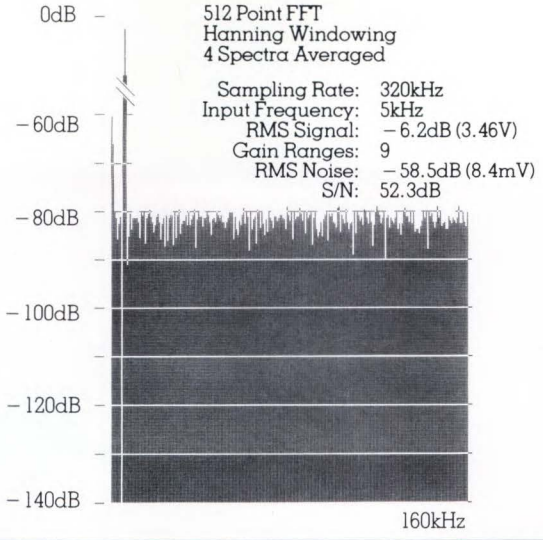

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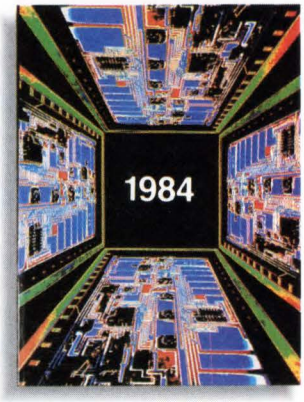

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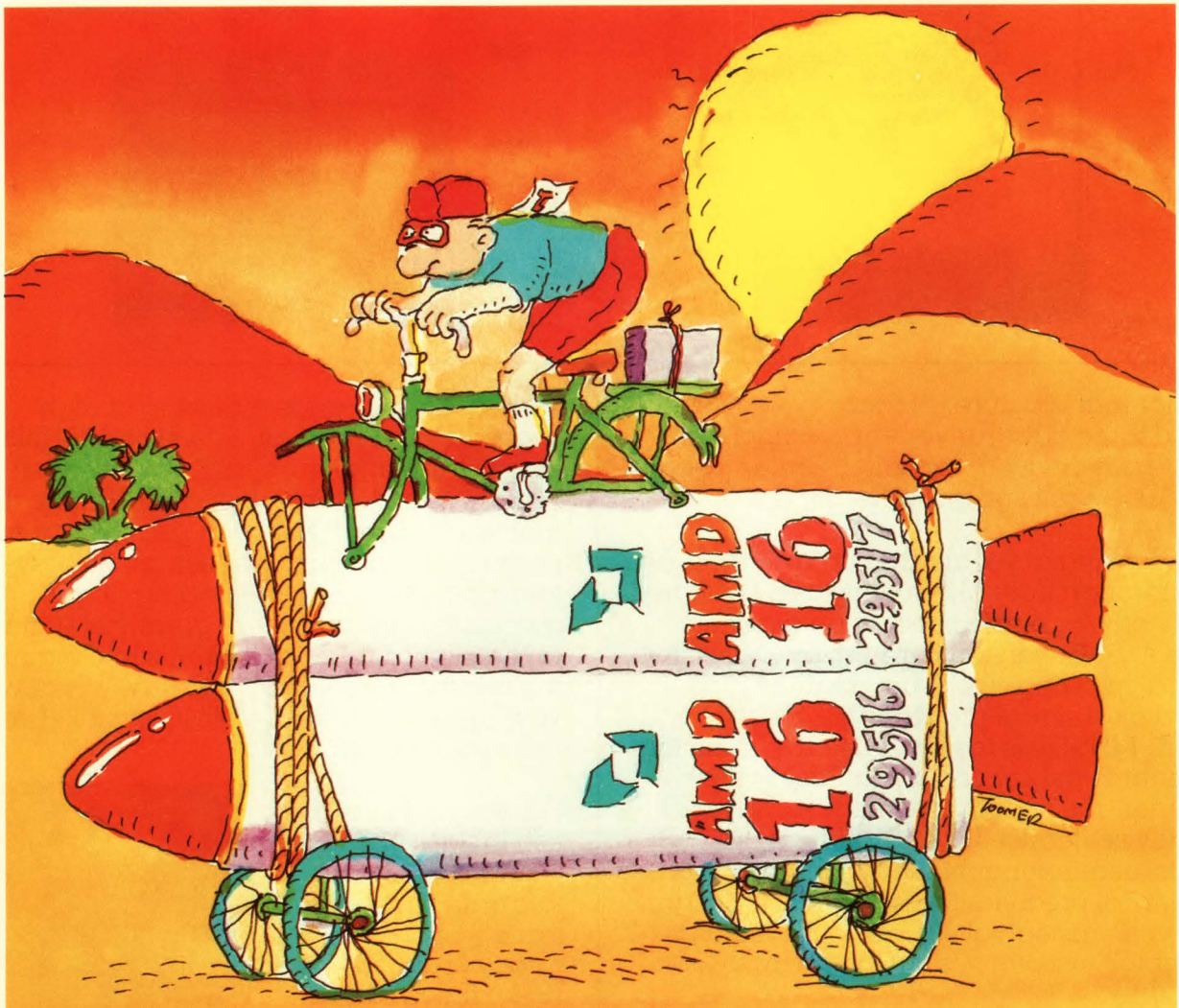

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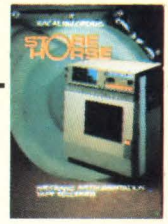

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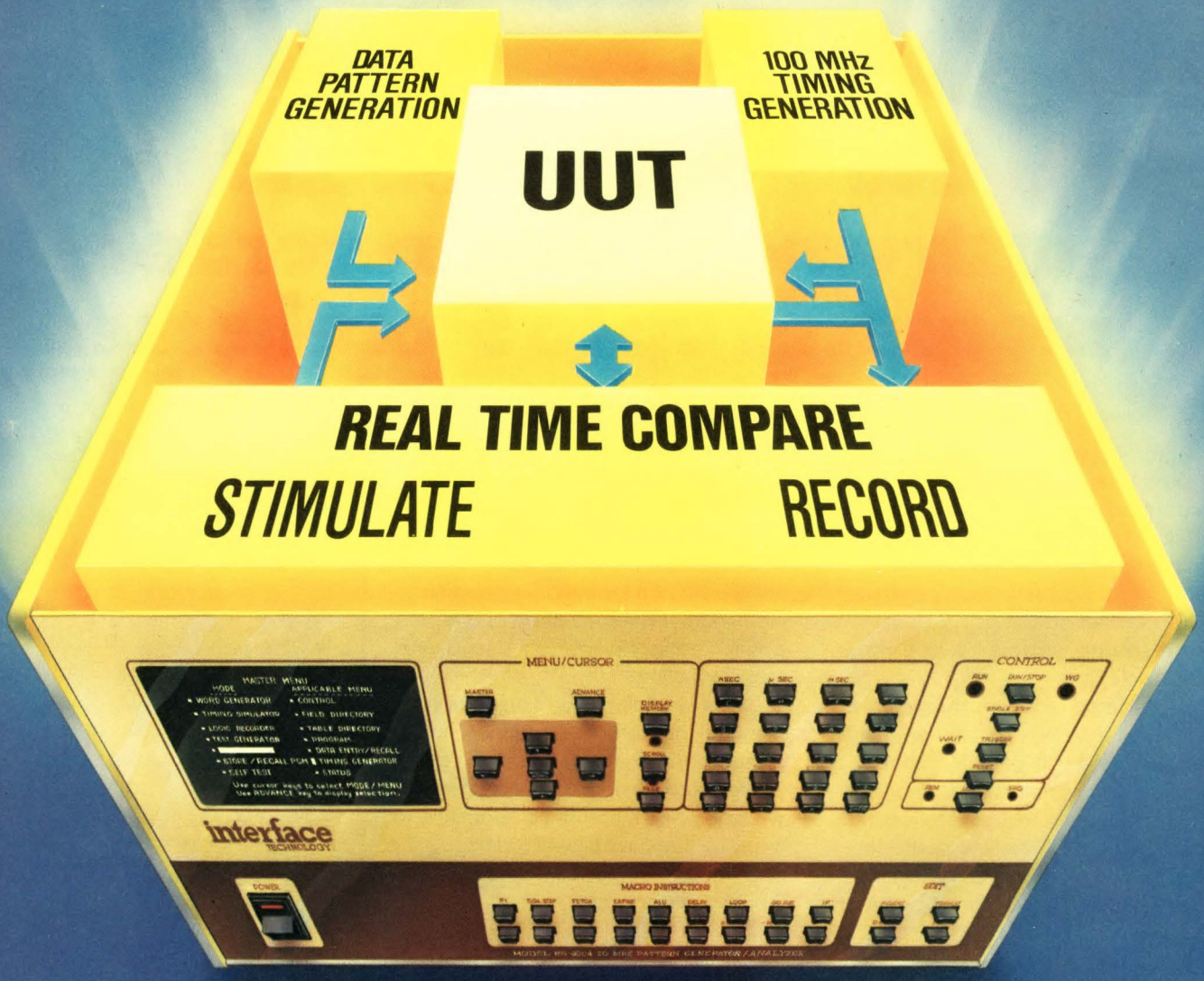

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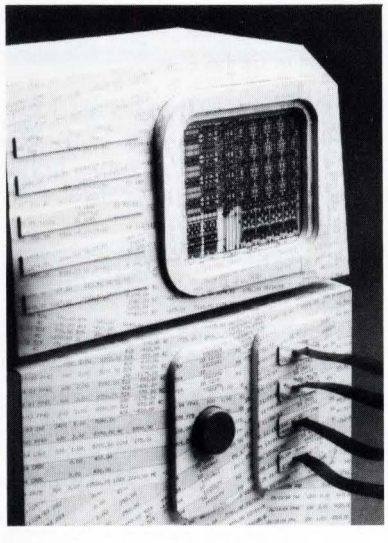

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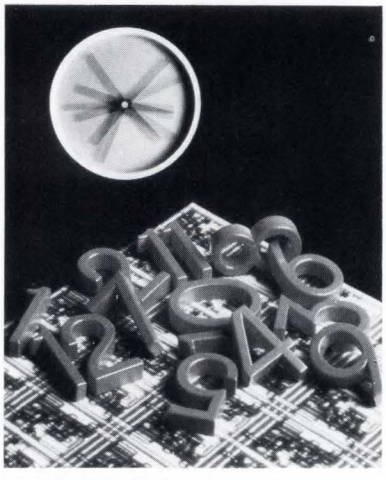

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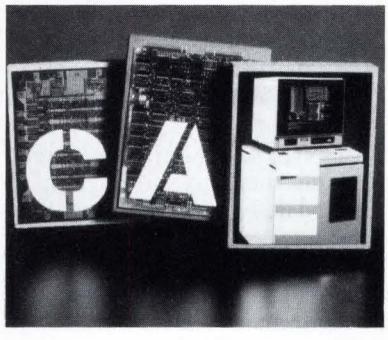

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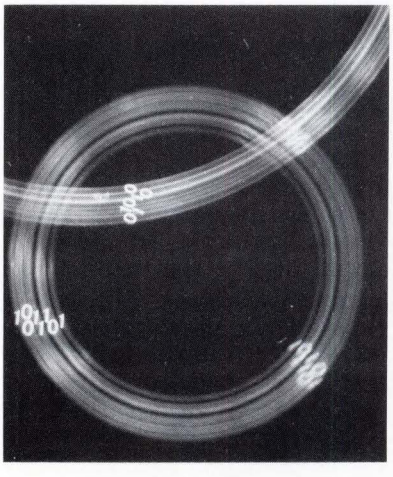

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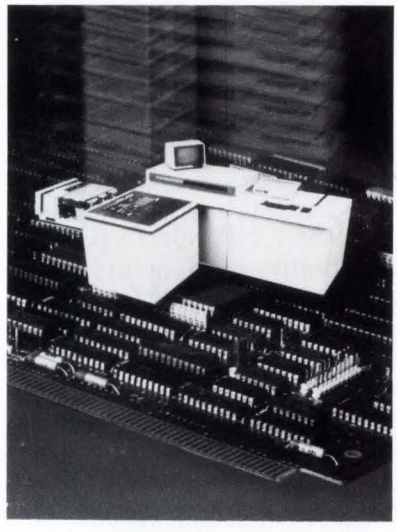

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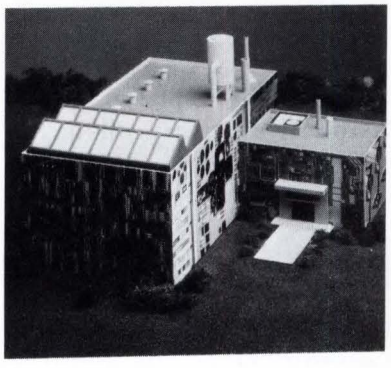

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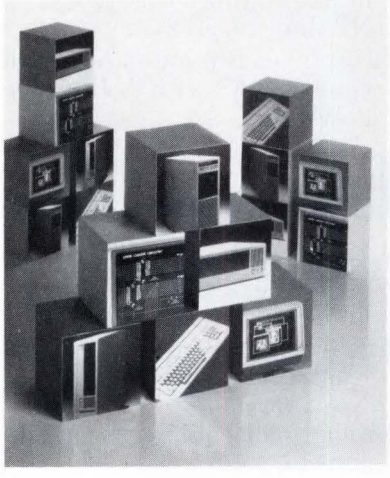

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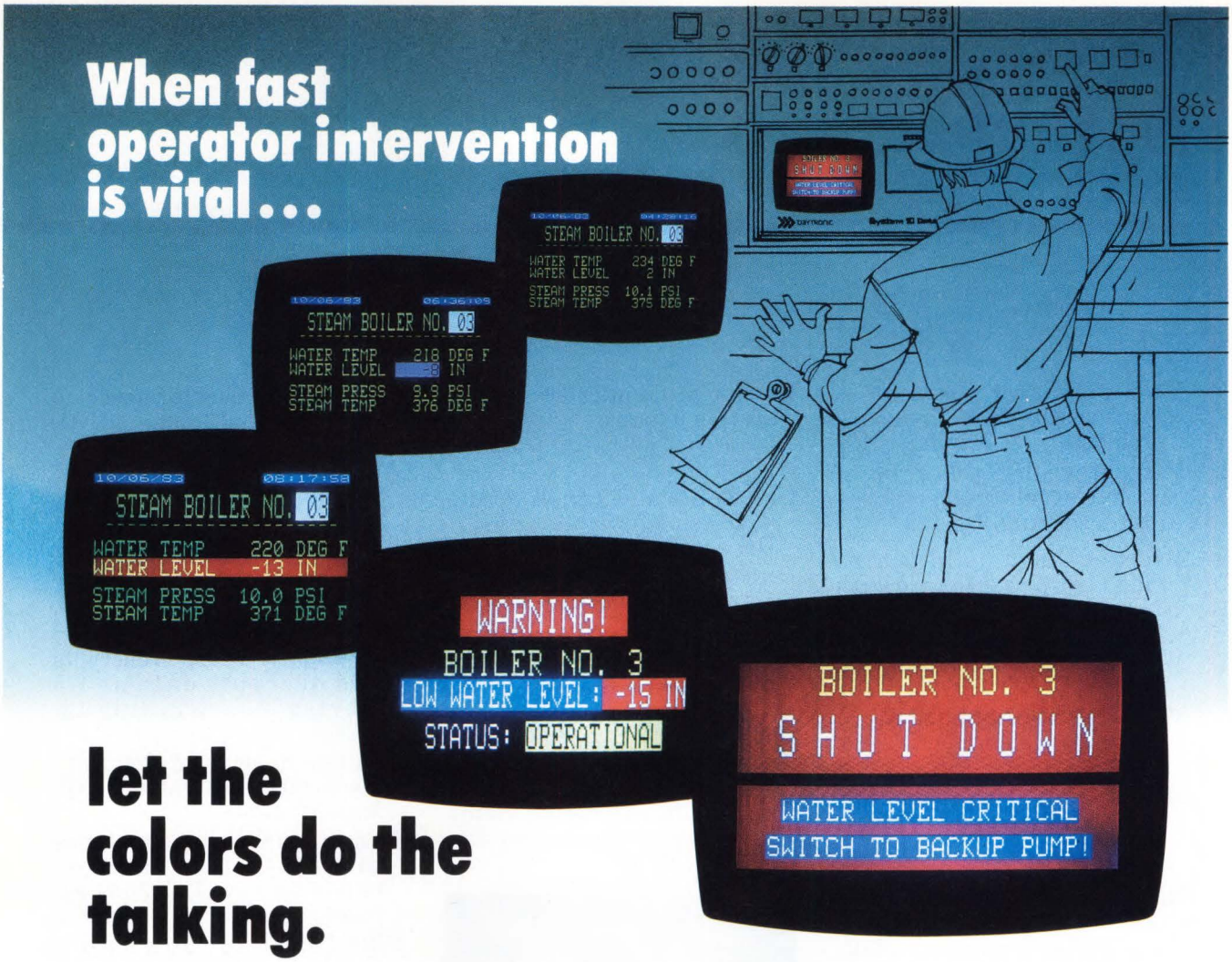

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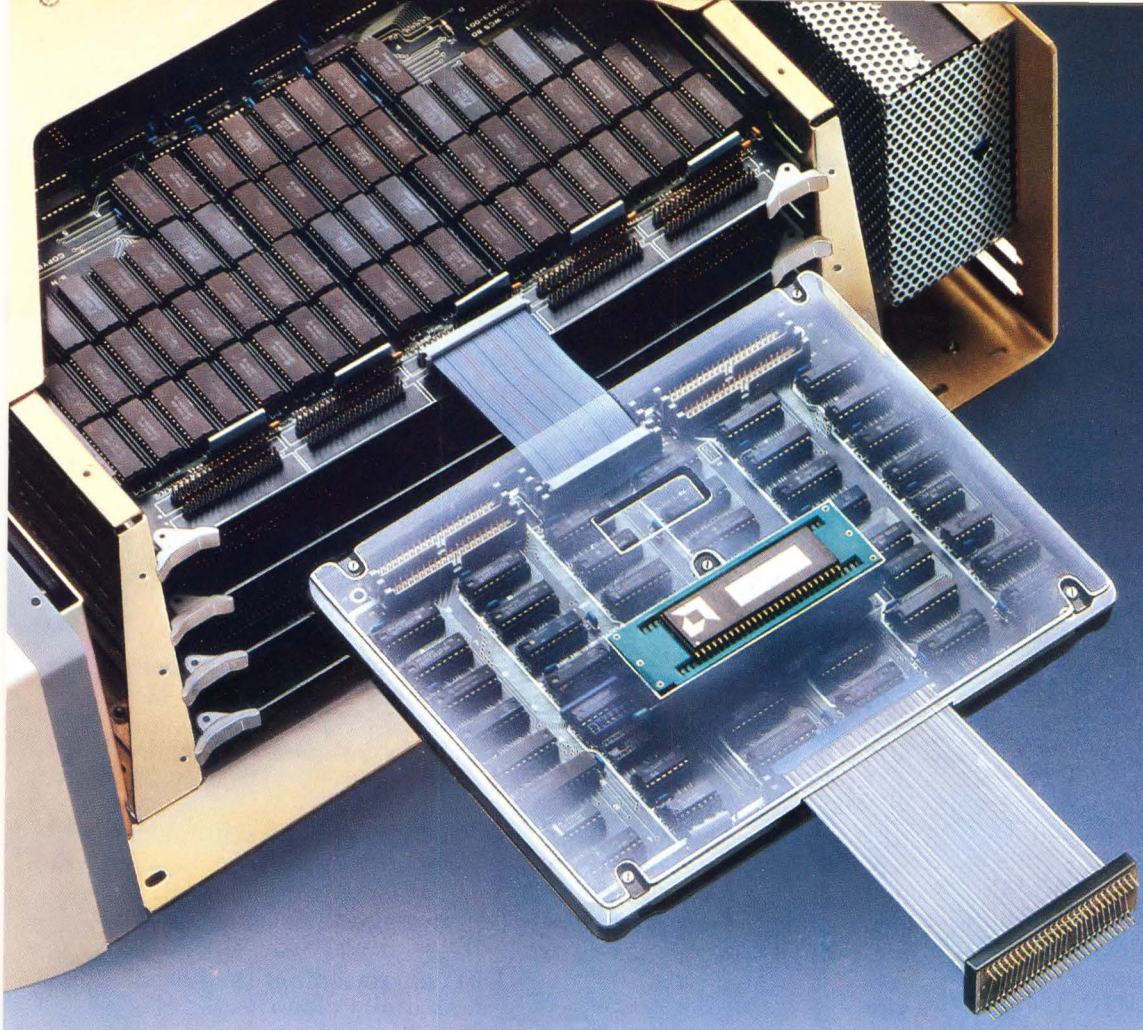

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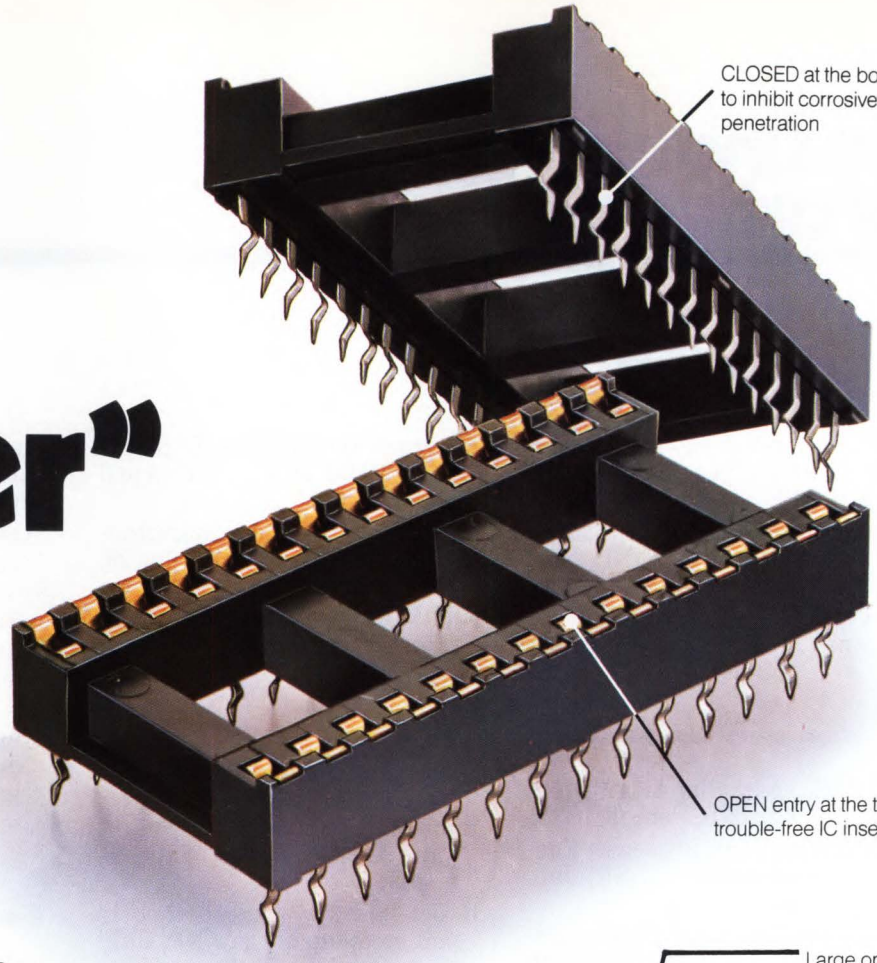

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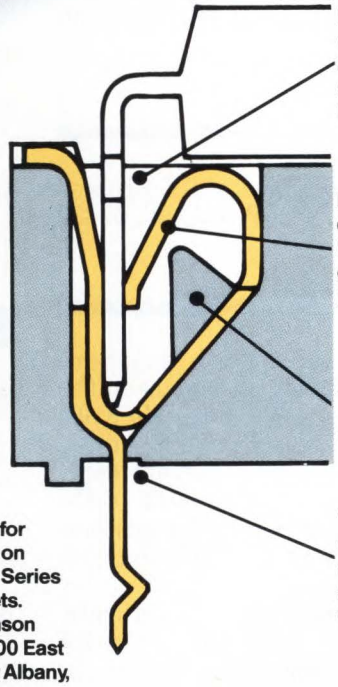

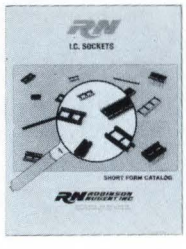

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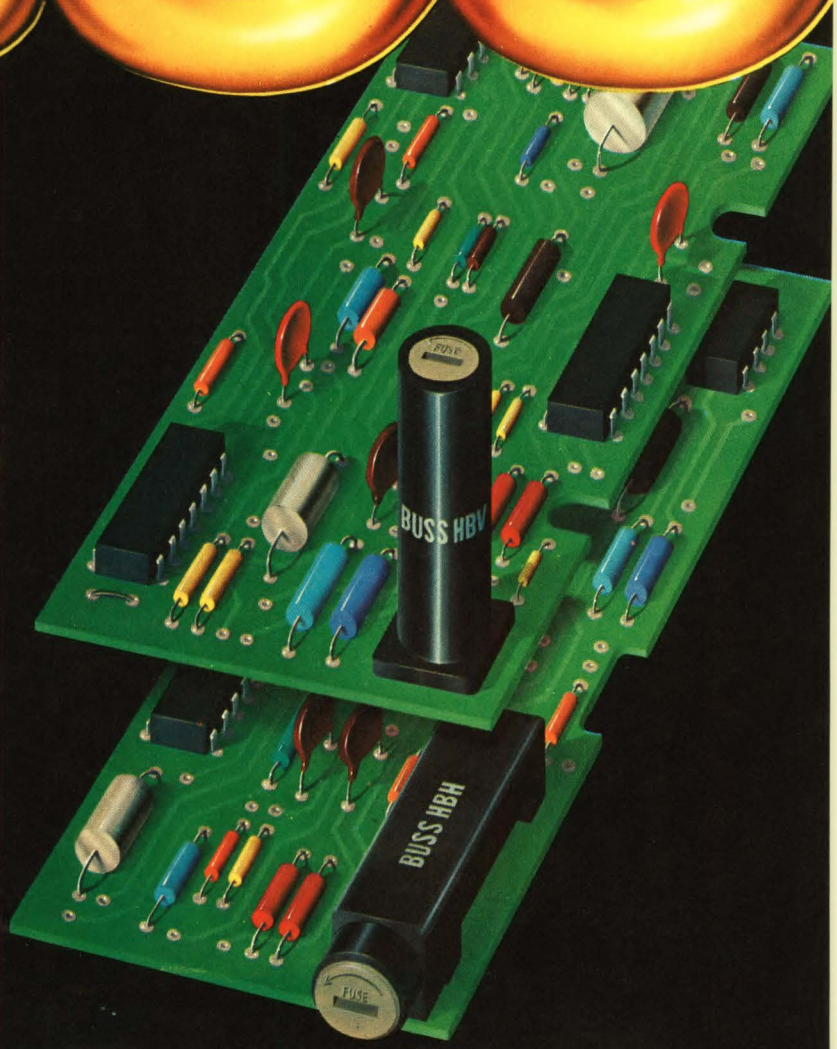

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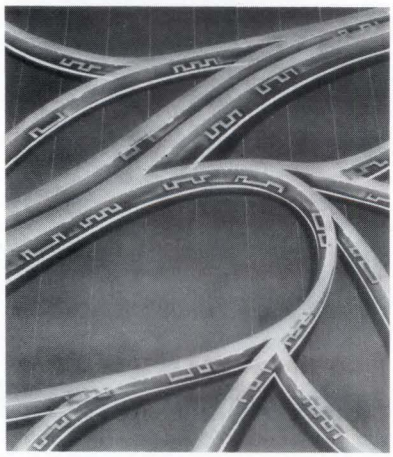

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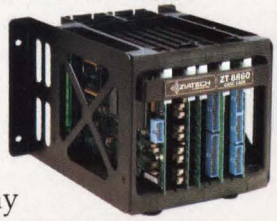

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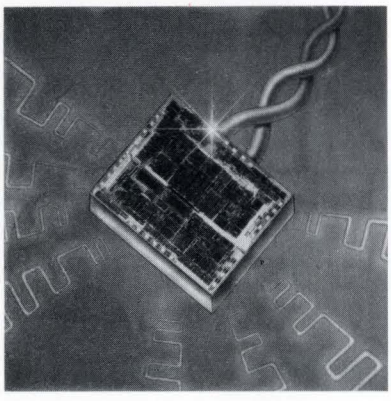

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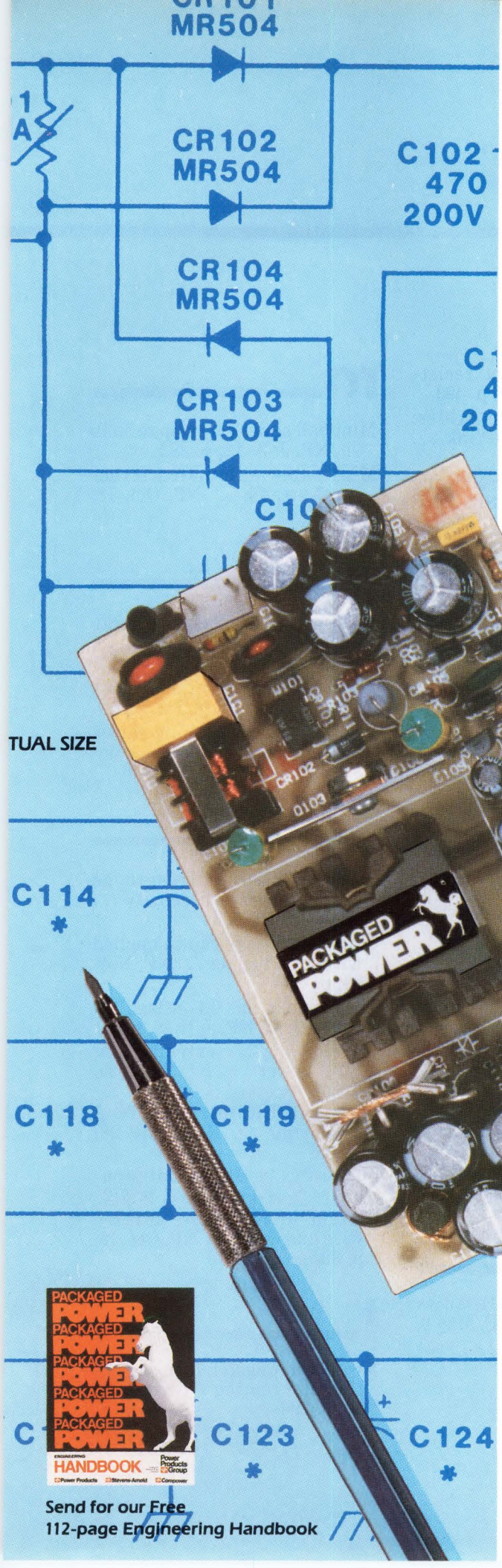

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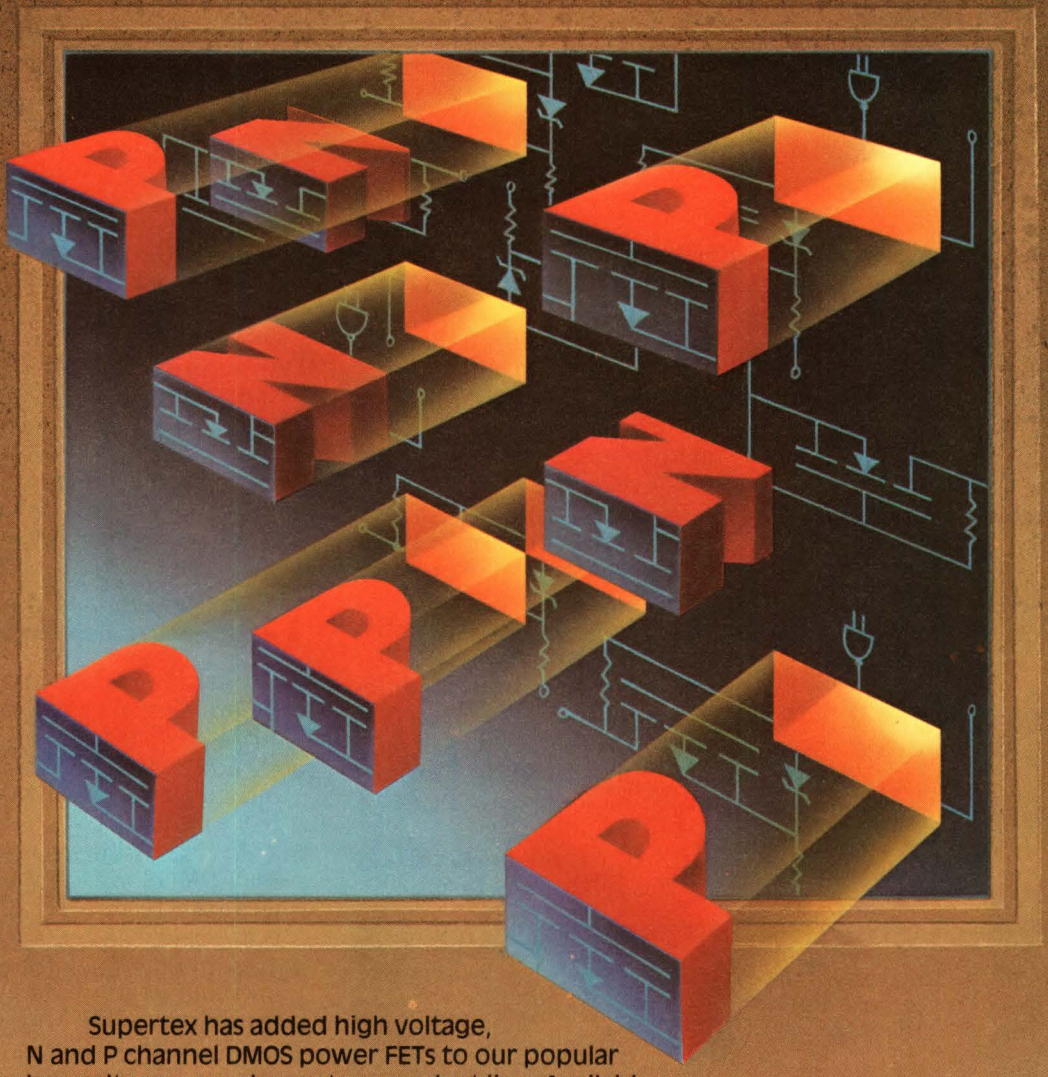

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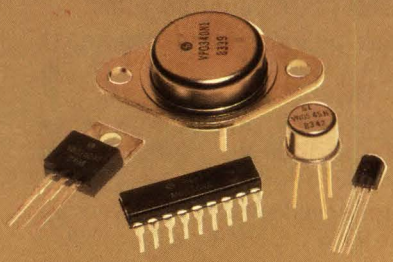

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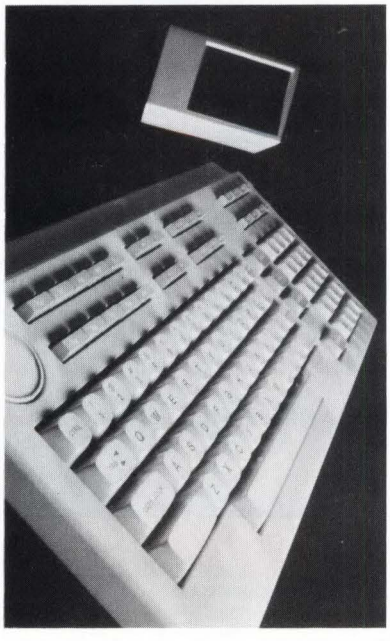

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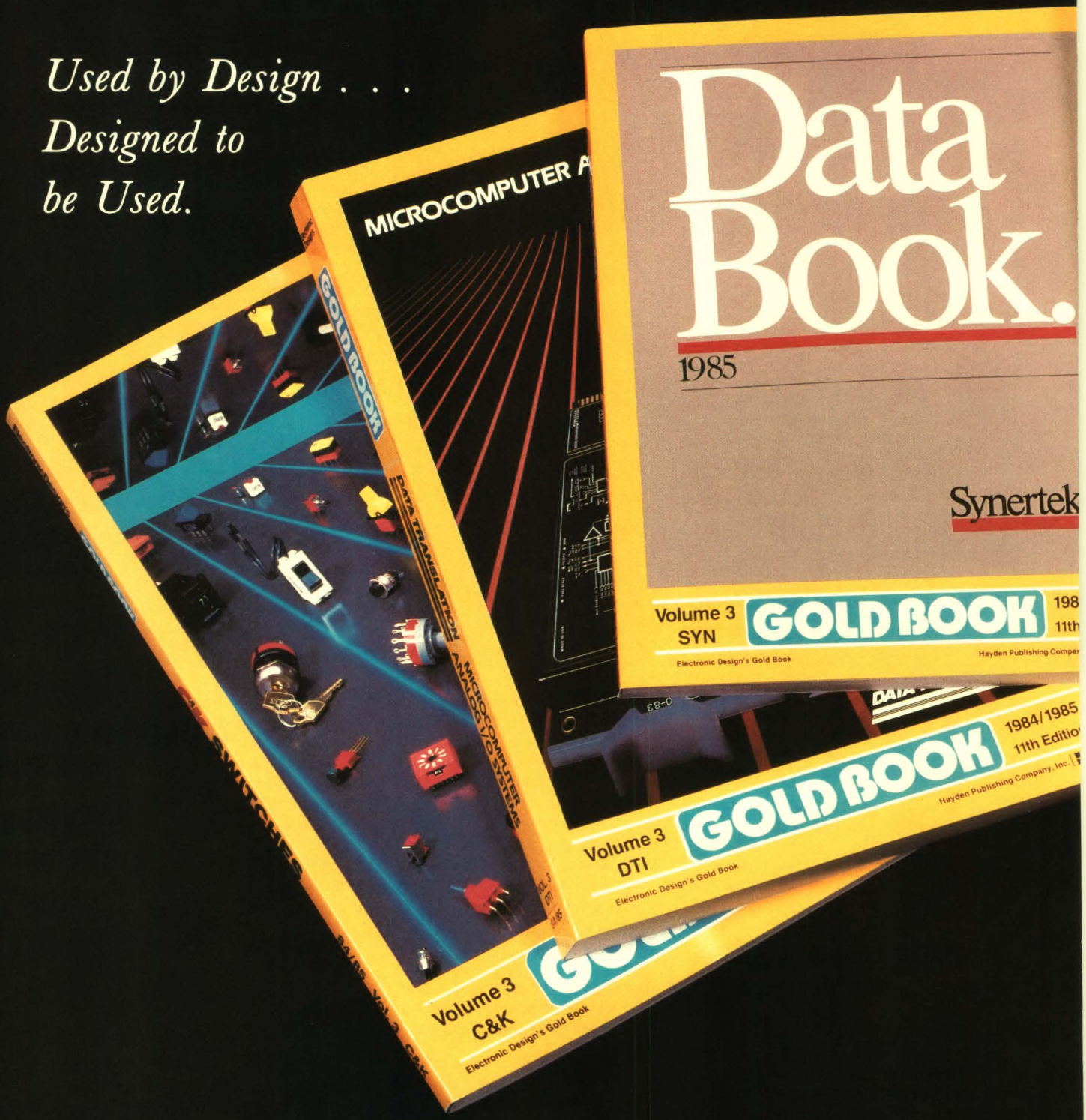

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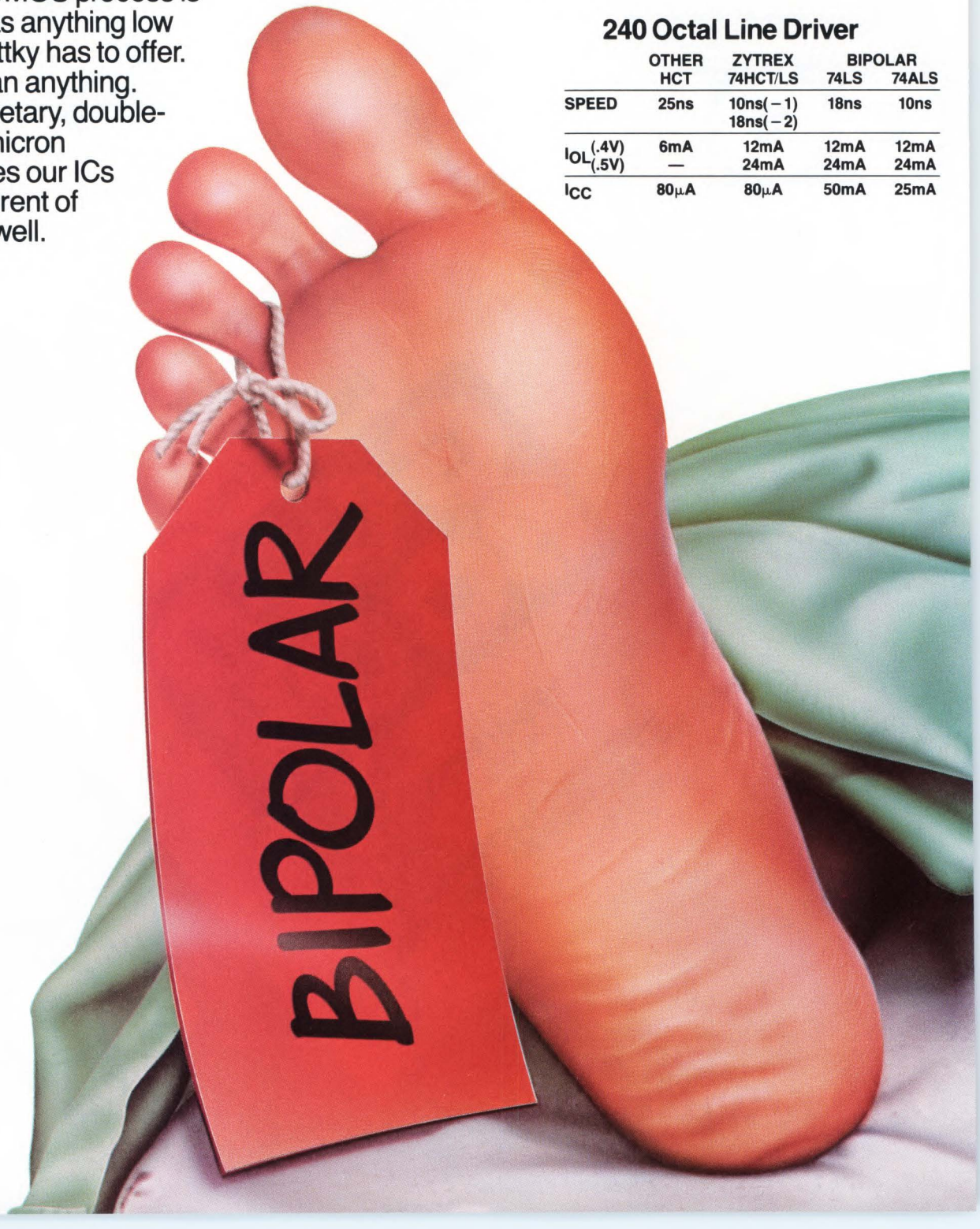

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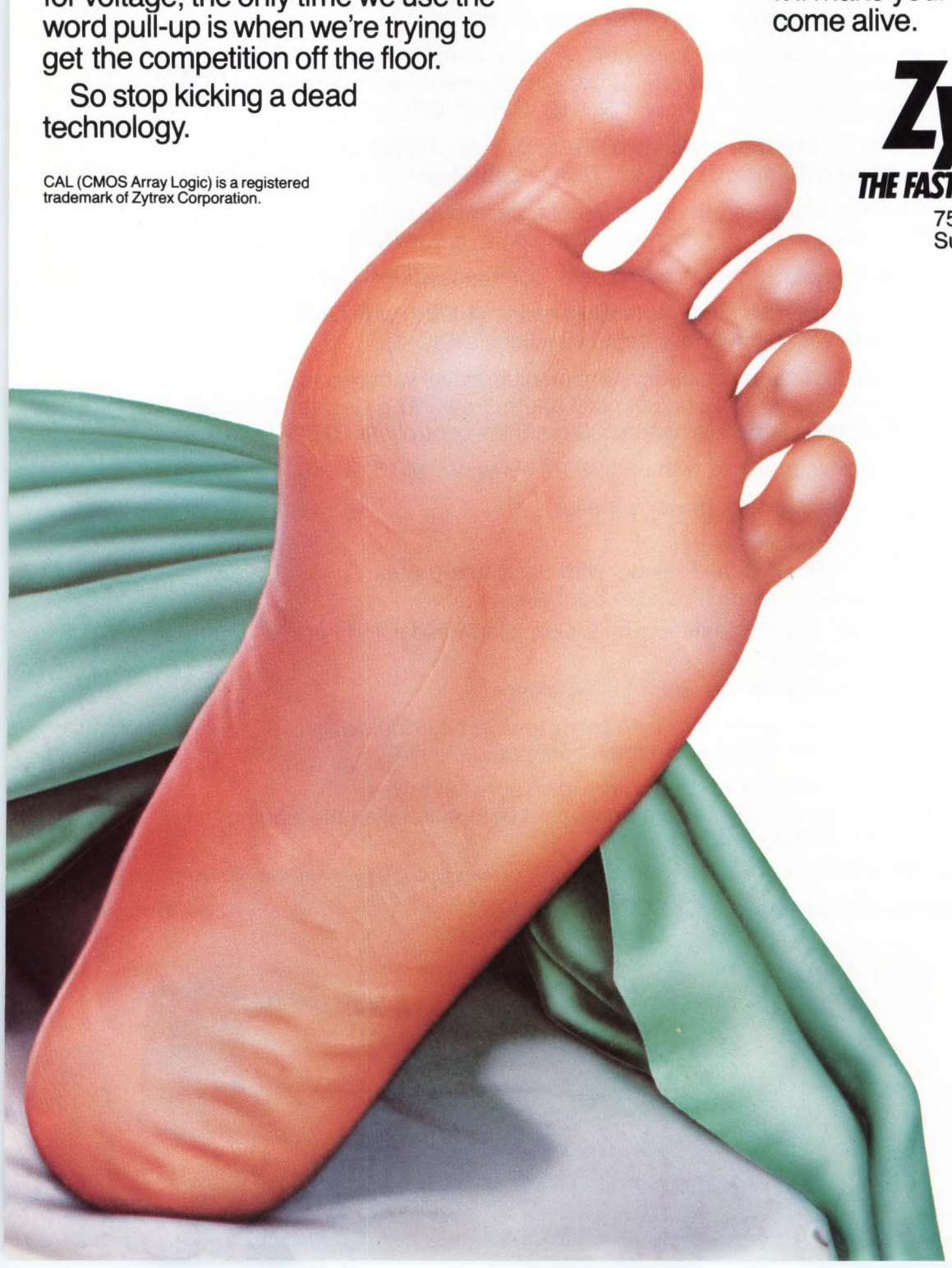

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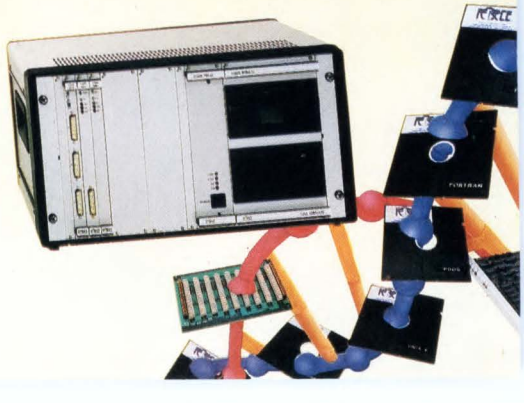

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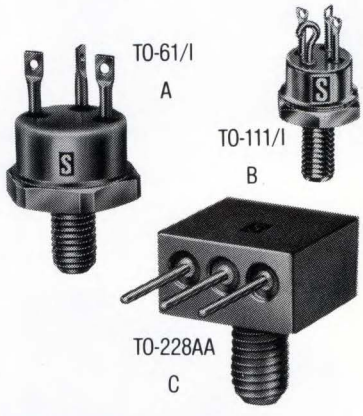

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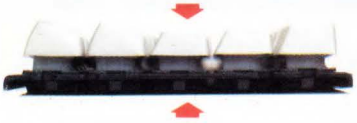

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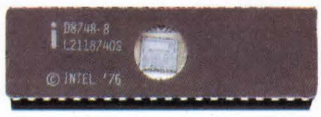

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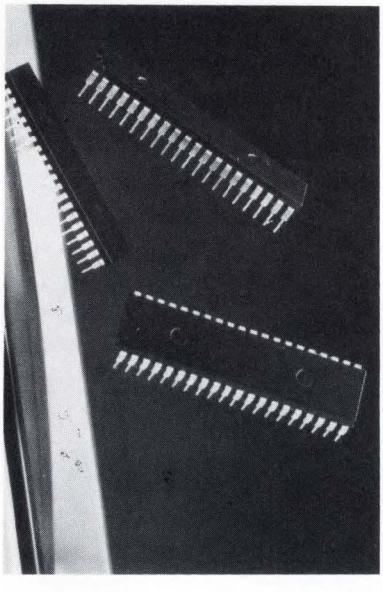

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Cerdip — Ceramic dip.

Characteristic impedance — The number Z_O, which represents the combination of capacitance, inductance and resistance seen by a signal traveling through a circuit.

Chip capacitor — A capacitor housed in a surface mount package, SMD.

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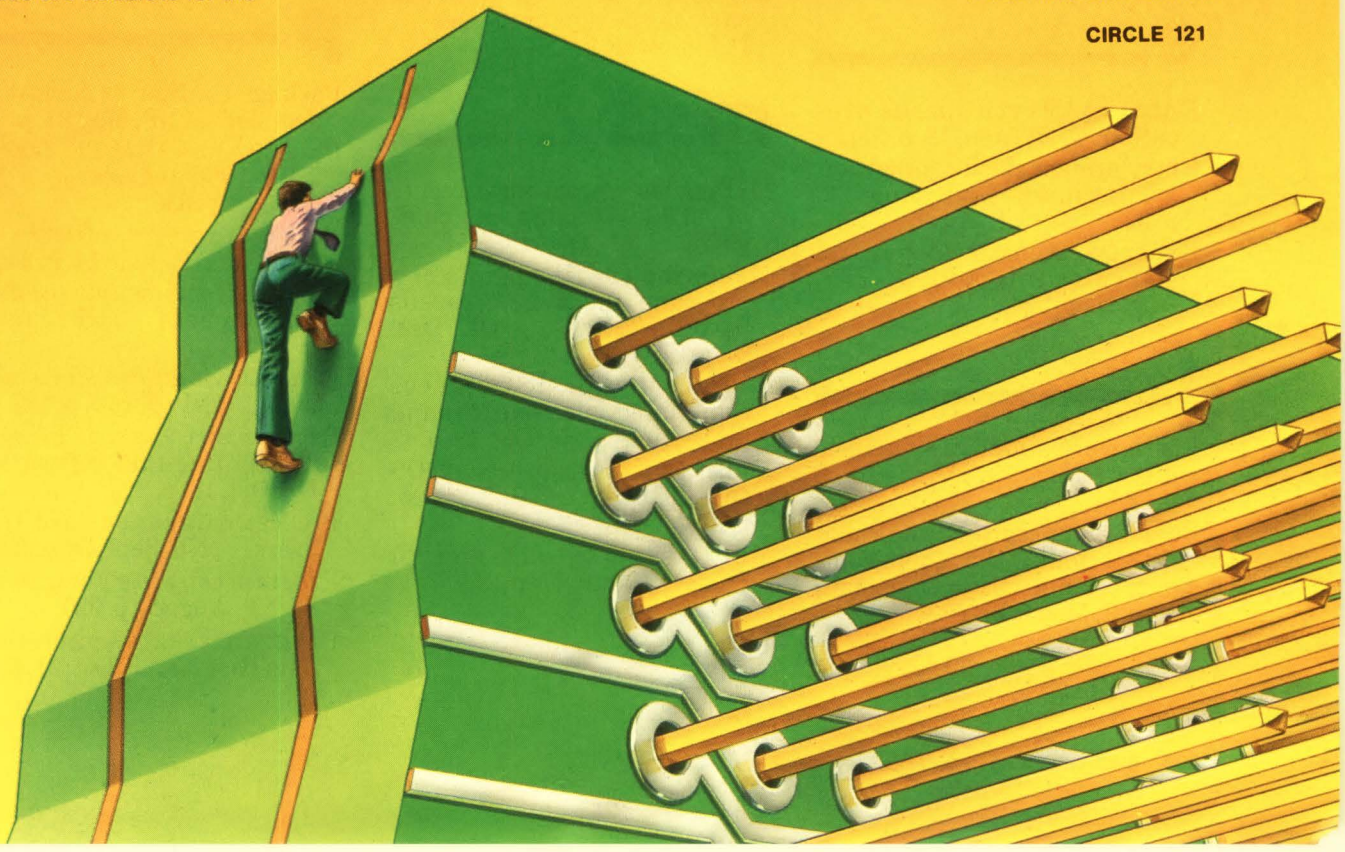

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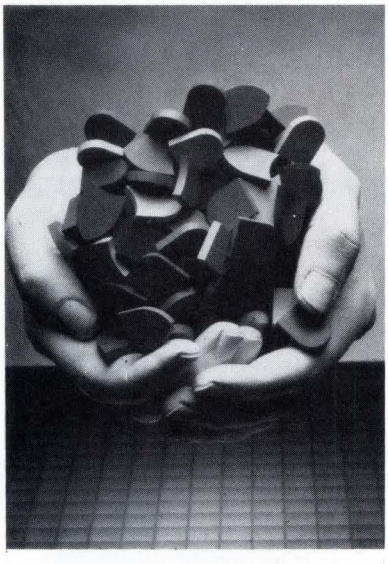

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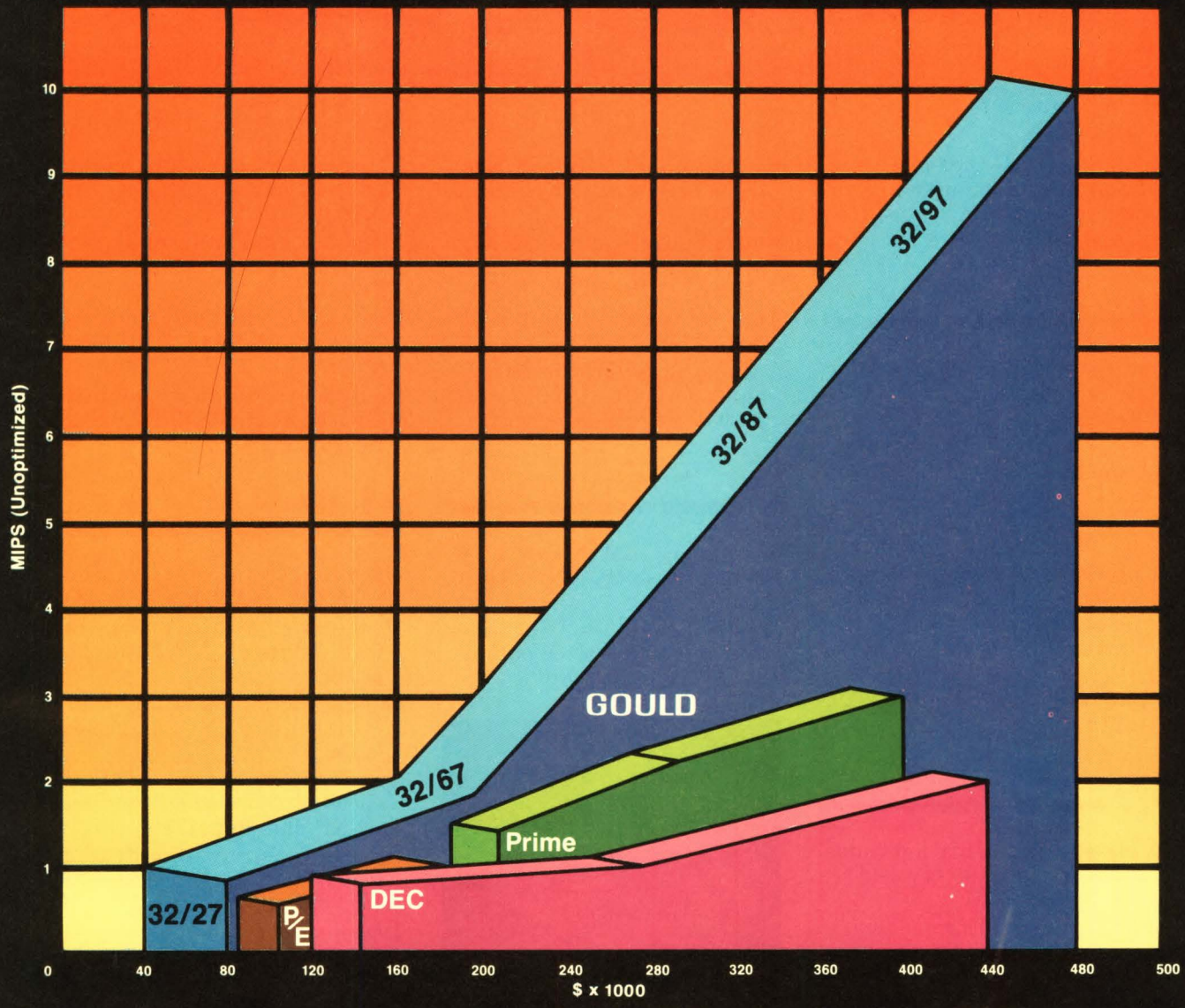

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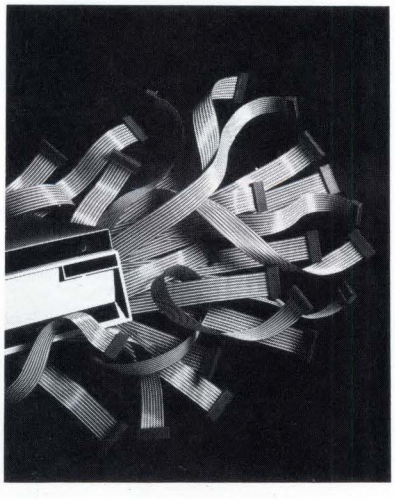

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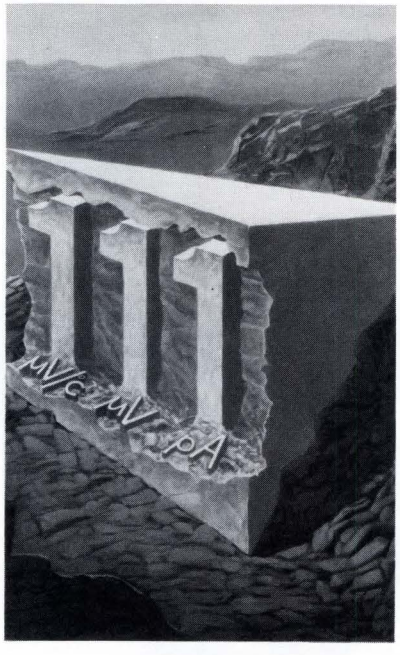

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Quad NOR Gate	10G000	75 ps
Fanout Buffer	10G011	3 GHz
Comparator/ Driver	10G012	3 GHz
Precision D Flip Flop	10G021	3 GHz
2 Stage Divider	10G060	3 GHz
7 Stage Counter	10G065	3 GHz

NAME	PART NUMBER	SPEED
Variable Modulus Divider	10G070	2 GHz
7 Stage Divider	11G566	4 GHz
Diode Array	16G010	500 GHz
Diode Array	16G011	675 GHz
FET Array	16G020	15 GHz
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VOLTAGE AND CURRENT RATINGS
DC INPUT 4.5–6.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV p-p)	MAX CURRENT (A) 45°C	50°C	60°C	65°C	PKG. SIZE	DIMENSIONS (in.)	PRICE QTY. 1	QTY. 100	QTY. 1,000
5V±5% NON-ADJ											
LWS-190-5	0.5%, 1.0%	120	0.5	0.5	–	0.200	90	1.85 × 0.47 × 1.85	$49	$39	$20
LWS-191-5	0.5%, 1.0%	120	1.0	–	0.400	–	91	1.85 × 0.75 × 1.85	59	47	25
12V±5% NON-ADJ											
LWS-190-12	0.5%, 1.0%	150	0.21	0.21	–	0.084	90	1.85 × 0.47 × 1.85	49	39	20
LWS-191-12	0.5%, 1.0%	150	0.42	–	0.168	–	91	1.85 × 0.75 × 1.85	59	47	25
15V±5% NON-ADJ											
LWS-190-15	0.5%, 1.0%	150	0.17	0.17	–	0.060	90	1.85 × 0.47 × 1.85	49	39	20
LWS-191-15	0.5%, 1.0%	150	0.34	–	0.136	–	91	1.85 × 0.75 × 1.85	59	47	25

DC INPUT 4.5–10.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV p-p)	MAX CURRENT (A) 40°C	50°C	60°C	PKG. SIZE	DIMENSIONS (in.)	PRICE QTY. 1	QTY. 100	QTY. 1,000
4.75-16 VOLTS ADJ.										
LWS-193-5	0.1%, 0.4%	100	2.0	1.7	1.5	93	1.25 × 3.5 × 2.5	$ 89	$ 76	$62
LWS-194-5	0.1%, 0.4%	100	3.0	2.6	2.3	94	1.25 × 3.5 × 2.5	119	101	75
15-30 VOLTS ADJ.										
LWS-193-24	0.1%, 0.4%	200	0.65	0.57	0.50	93	1.25 × 3.5 × 2.5	89	76	62
LWS-194-24	0.1%, 0.4%	200	1.00	0.90	0.75	94	1.25 × 3.5 × 2.5	119	101	75

DC INPUT 10.0–15.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV p-p)	MAX CURRENT (A) 45°C	50°C	60°C	65°C	PKG. SIZE	DIMENSIONS (in.)	PRICE QTY. 1	QTY. 100	QTY. 1,000
5V±5% NON-ADJ											
LWS-290-5	0.5%, 1.0%	120	0.60	0.60	–	0.24	90	1.85 × 0.47 × 1.85	$49	$39	$20
LWS-291-5	0.5%, 1.0%	120	1.20	–	0.48	–	91	1.85 × 0.75 × 1.85	59	47	25
12V±5% NON-ADJ											
LWS-290-12	0.5%, 1.0%	150	0.25	0.25	–	0.10	90	1.85 × 0.47 × 1.85	49	39	20
LWS-291-12	0.5%, 1.0%	150	0.50	–	0.20	–	91	1.85 × 0.75 × 1.85	59	47	25
15V±5% NON-ADJ											
LWS-290-15	0.5%, 1.0%	150	0.20	0.20	–	0.08	90	1.85 × 0.47 × 1.85	49	39	20
LWS-291-15	0.5%, 1.0%	150	0.40	–	0.16	–	91	1.85 × 0.75 × 1.85	59	47	25

DC INPUT 10.0–30.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV p-p)	MAX CURRENT (A) 40°C	50°C	60°C	PKG. SIZE	DIMENSIONS (in.)	PRICE QTY. 1	QTY. 100	QTY. 1,000
4.75-16 VOLTS ADJ.										
LWS-294-5	0.1%, 0.4%	100	3.0	2.6	2.3	94	1.25 × 3.5 × 2.5	$119	$101	$75
15-30 VOLTS ADJ.										
LWS-294-24	0.1%, 0.4%	200	1.0	0.9	0.75	94	1.25 × 3.5 × 2.5	119	101	75

VOLTAGE AND CURRENT RATINGS—CONT'D
DC INPUT 20.0–30.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV p-p)	MAX CURRENT (A) 45°C	50°C	60°C	65°C	PKG. SIZE	DIMENSIONS (in.)	PRICE QTY. 1	QTY. 100	QTY. 1,000
5V±5% NON-ADJ											
LWS-390-5	0.5%, 1.0%	120	0.60	0.60	–	0.24	90	1.85 × 0.47 × 1.85	$49	$39	$20
LWS-391-5	0.5%, 1.0%	120	1.20	–	0.48	–	91	1.85 × 0.75 × 1.85	59	47	25
12V±5% NON-ADJ											
LWS-390-12	0.5%, 1.0%	150	0.25	0.25	–	0.10	90	1.85 × 0.47 × 1.85	49	39	20
LWS-391-12	0.5%, 1.0%	150	0.50	–	0.20	–	91	1.85 × 0.75 × 1.85	59	47	25
15V±5% NON-ADJ											
LWS-390-15	0.5%, 1.0%	150	0.20	0.20	–	0.08	90	1.85 × 0.47 × 1.85	49	39	20
LWS-391-15	0.5%, 1.0%	150	0.40	–	0.16	–	91	1.85 × 0.75 × 1.85	59	47	25

DC INPUT 20.0–60.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV p-p)	MAX CURRENT (A) 40°C	50°C	60°C	PKG. SIZE	DIMENSIONS (in.)	PRICE QTY. 1	QTY. 100	QTY. 1,000
4.75-16 VOLTS ADJ.										
LWS-394-5	0.1%, 0.4%	100	3.0	2.6	2.3	94	1.25 × 3.5 × 2.5	$119	$101	$75
15-30 VOLTS ADJ.										
LWS-394-24	0.1%, 0.4%	200	1.0	0.9	0.75	94	1.25 × 3.5 × 2.5	119	101	75

LW SERIES: Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE
regulation, line .....0.1% from minimum to maximum on LWS-194, LWS-294, LWS-394, and LWS-193 models; 0.5% on all other models.
regulation, load .....0.4% for load variations from no-load to full load, or full load to no load on LWS-194, LWS-294, LWS-394 and LWS-193 models; 1.0% on all other models.
ripple and noise .....100 mV p-p for 5 V models of LWS-194, LWS-294, LWS-394, and LWS-193.
200 mV p-p for 24 V models of LWS-194, LWS-294, LWS-394, and LWS-193.
120 mV p-p for 5 V output of LWS-191, LWS-291, LWS-391, LWS-190, LWS-290, LWS-390.
150 mV p-p for 12 V and 15 V outputs of LWS-191, LWS-291, LWS-391, LWS-190, LWS-290, LWS-390.
efficiency .....50% minimum for LWS-194, LWS-294, LWS-394, and LWS-193.
58% minimum for LWS-190.
60% minimum for LWS-191.
64% minimum for LWS-391.
67% minimum for LWS-390.
68% minimum for LWS-291.
70% minimum for LWS-290.
temperature coefficient.....0.03%/°C on LWS-194, LWS-294, LWS-394, and LWS-193; 0.02%/°C on all other models.

AMBIENT OPERATING TEMPERATURE
Continuous duty 0° to 60°C with suitable derating above 40°C for LWS-194, LWS-294, LWS-394, and LWS-193. Continuous duty −5°C to +60°C with suitable derating above 45°C for LWS-191, LWS-291, LWS-391. Continuous duty −5°C to +65°C with suitable derating above 50°C for LWS-190, LWS-290, LWS-390.

OVERLOAD PROTECTION
External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

STORAGE TEMPERATURE RANGE
−55°C to +85°C for LWS-194, LWS-294, LWS-394, and LWS-193; −20°C to +85°C for all other models.

OVERSHOOT
No overshoot at turn-on, turn-off, or power failure.

COOLING
All units are convection cooled. No fans or blowers needed.

MOUNTING
PC board mountable. Refer to outline drawings in catalog.

OUTPUT VOLTAGE ADJUSTMENT
LWS-194, LWS-294, LWS-394, LWS-193
Output voltage can be set to desired value within the entire range by inserting a resistor between + V and RP terminals. Resistor can be selected as per table supplied in instruction manual.

INPUT/OUTPUT CONNECTIONS
DC input and outputs are via pin-type connections. Refer to outline drawings in catalog.

PHYSICAL DATA

Package Model	Weight Lb. Net	Lb. Ship	Size (in.)
LWS-194	0.65	0.9	2.5 × 3.5 × 1.25
LWS-294	0.65	0.9	2.5 × 3.5 × 1.25
LWS-394	0.65	0.9	2.5 × 3.5 × 1.25
LWS-193	0.65	0.9	2.5 × 3.5 × 1.25
LWS-190	0.10	0.12	1.85 × 0.47 × 1.85
LWS-290	0.10	0.12	1.85 × 0.47 × 1.85
LWS-390	0.10	0.12	1.85 × 0.47 × 1.85
LWS-191	0.16	0.19	1.85 × 0.75 × 1.85
LWS-291	0.16	0.19	1.85 × 0.75 × 1.85
LWS-391	0.16	0.19	1.85 × 0.75 × 1.85

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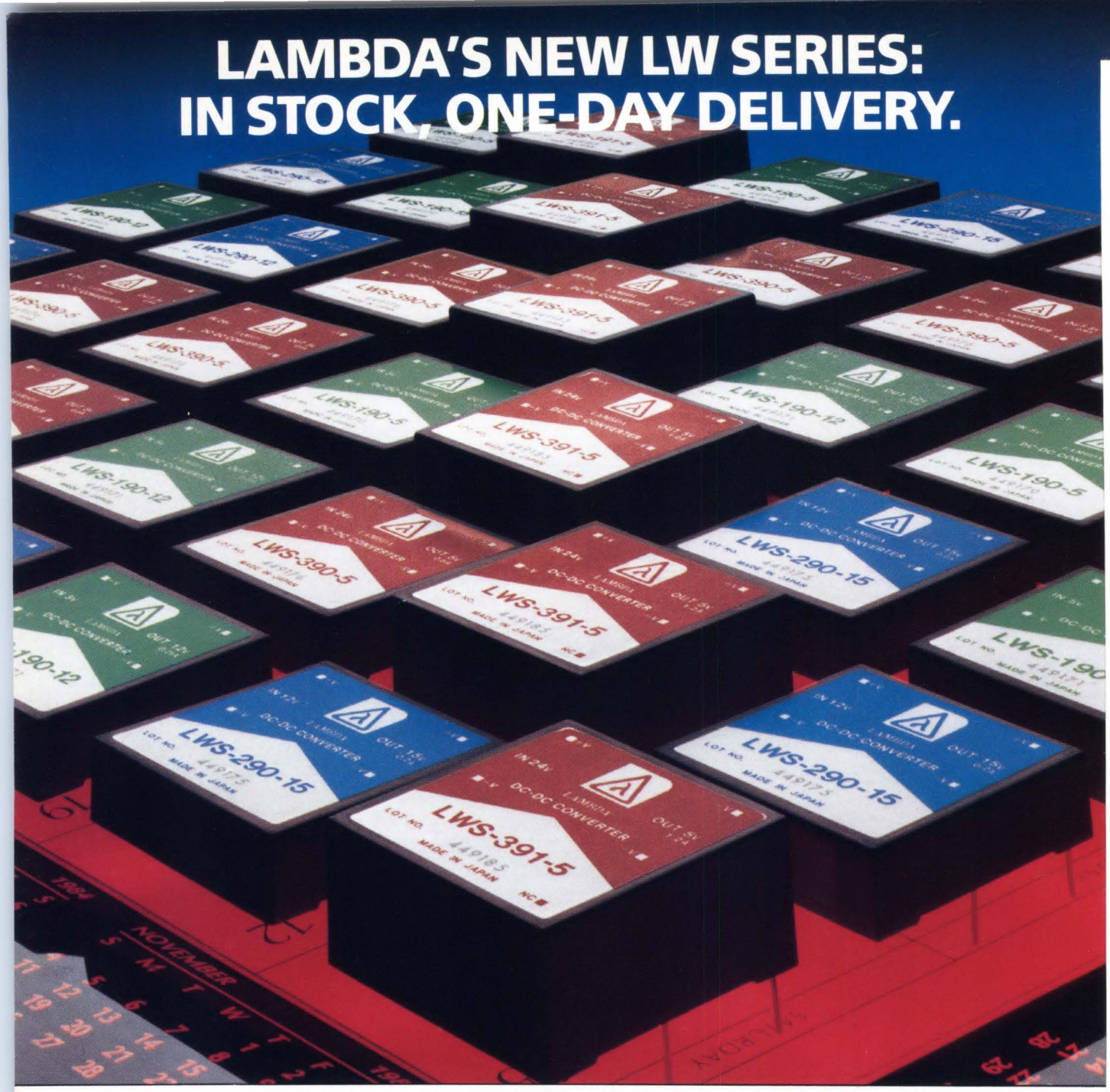

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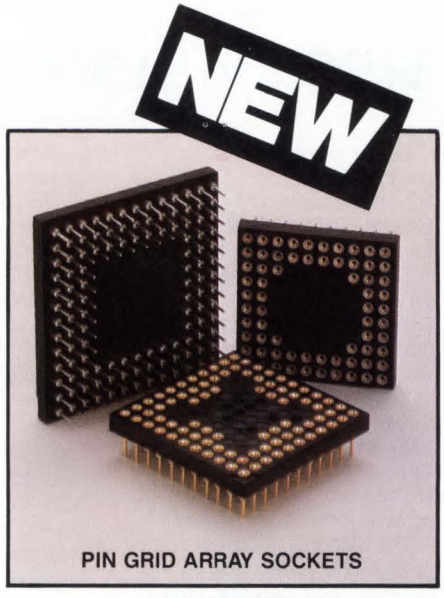

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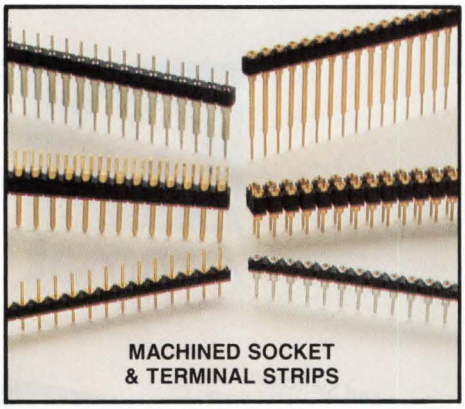

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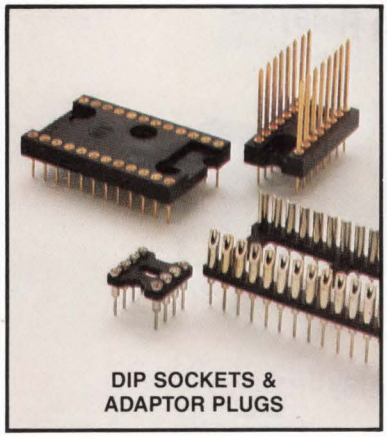

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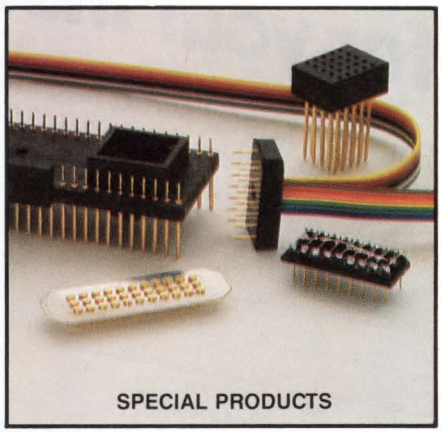

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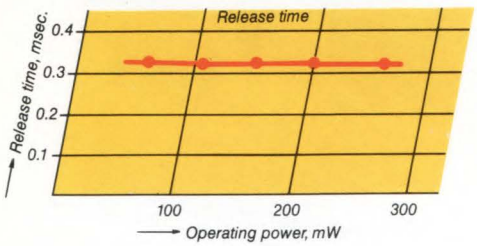

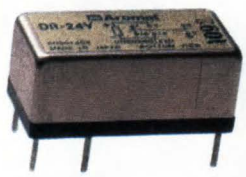

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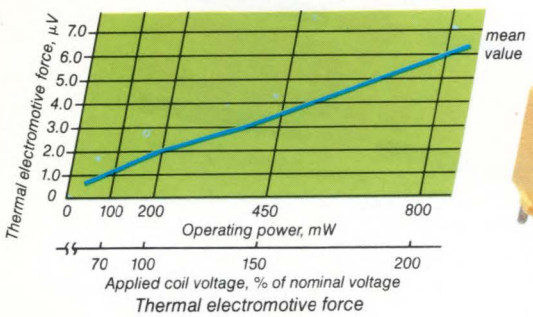

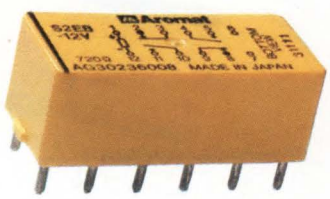

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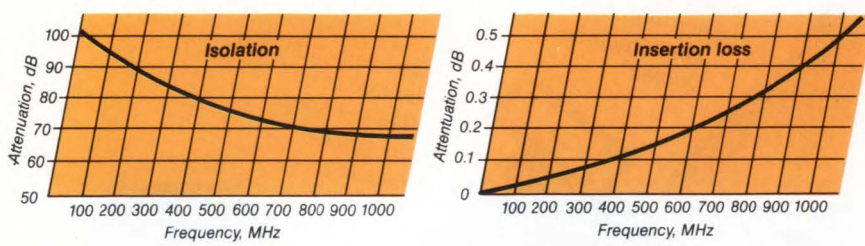

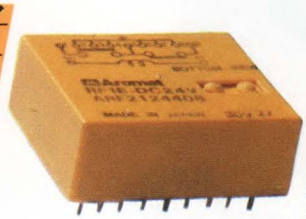

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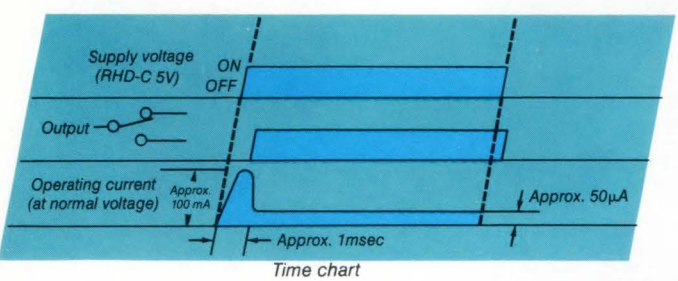

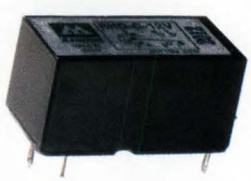

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CIRCLE 136

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Software puts complex FFTs within the grasp of personal computers

Employing a new mixed-radix algorithm for fast Fourier transforms, a software package expands the capabilities of microcomputers. Unlike other small-system FFT programs, the Modular Access Design, Computer-Aided Processing (MADCAP) software handles inverse transforms (from the frequency into the time domain) as well and works on signal sampling points that are not powers of two (Fig. 1).

Furthermore, MADCAP can work as a synthesizer of sine and composite waves. Thus it performs functions that normally require hardware costing thousands of dollars.

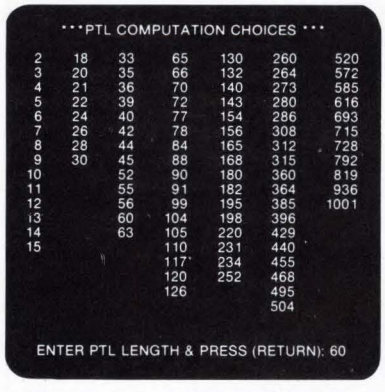
In addition to the length menu and 16 help screens, the user interface includes a data input screen that prompts the user in English (Fig. 2). Out-of-range values are trapped and brought to the user's attention. The main menu offers a choice of weighting (rectangular or Hamming), built-in transformation of files with different formats (e.g., from separate real and imaginary data blocks into an interlaced format), a search for up to 3200 floating-point data files, and up to eight user-defined modules (other transforms or even hardware). Data can be accepted from data acquisition hardware, and the program can interface with a-d and d-a hardware, which would be user-defined modules.

By displaying results on an automatically scaled strip chart, the package facilitates evaluation of both the input and the transformed data. The chart is annotated with either the sample or the filter number for identification. Alternatively, the program issues results in a floating-point format accurate to 7 to 11 significant digits.

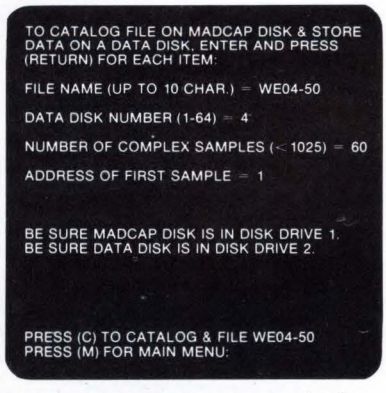
At present, MADCAP runs on the IBM PC, PC XT and PC AT; the Apple II series; Texas Instruments' Professional; and the Zenith Z-100 personal computers. In compiled Basic, the program occupies two 5¼-in. floppy disks and costs $1595. The version for the Apple is available immediately. Shipments of the versions for the IBM, TI, and Zenith machines will begin in January.

Whitman Engineering Inc., PO Box 1929, Maitland, Fla. 32751; (305) 628-4516.

CIRCLE 312



1. The MADCAP FFT software gives the user a wide choice of sampling points—104 possibilities—some of which are not shown on this screen. Here, the user has selected 60 points.

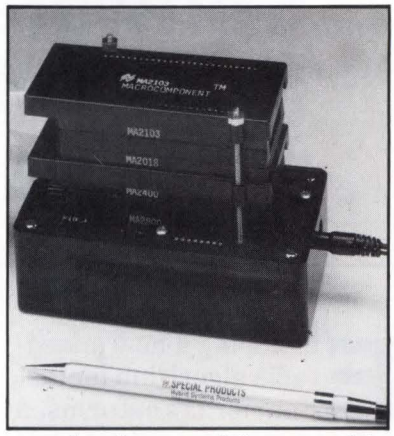


2. For error-free use even by inexperienced personnel, MADCAP prompts users for all required inputs and checks them immediately. Any errors are explained in everyday English.

Max Schindler

SOFTWARE

Forth module completes stacked μC system



The Forth language is embedded in a CMOS EPROM module, completing a basic version of National Semiconductor's recently introduced MA2000 stackable microcomputer system. The MA2000 has battery backup and is portable and readily configured, since it has no backplane and consists of stacked modules. With Forth, the system can be easily programmed for test, diagnostic, control, and data-logging operations.

The module, the MA2301, houses a full implementation of the MVP-Forth version of the Forth-79 standard. It also provides utilities for program development. Multiple tasks can be run simultaneously, and the module generates 25 screens of storage for developed Forth programs.

Containing four NSC27C32 high-speed EPROMs, the module dissipates 1.0 W. It is used with the basic MA2000 system—a CPU (NSC800), two serial I/O units (for a printer and a terminal), a power supply, and 16-kbyte CMOS RAM modules.

The MA2301 is priced at $125 in single quantities. It is available from stock.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000.

CIRCLE 316

ROEDERSTEIN

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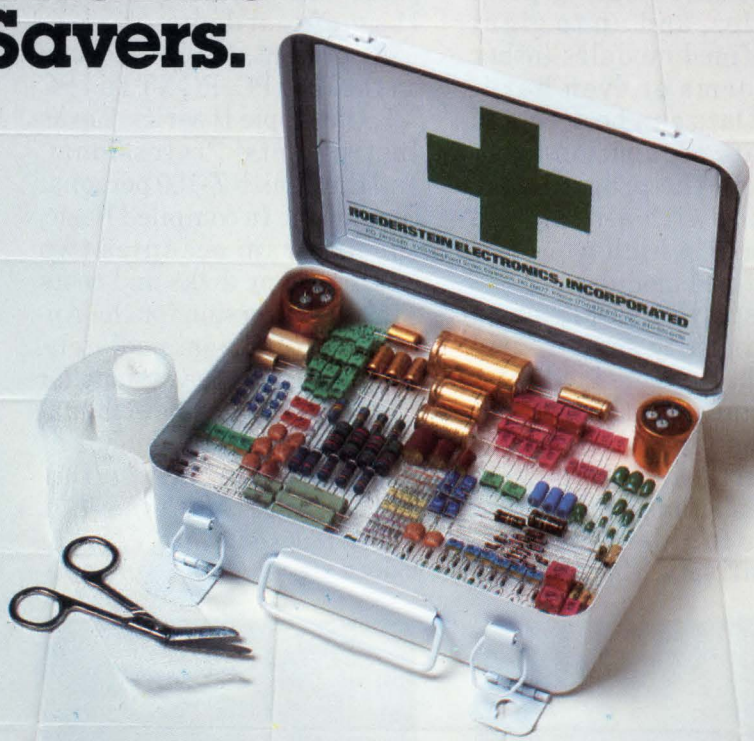

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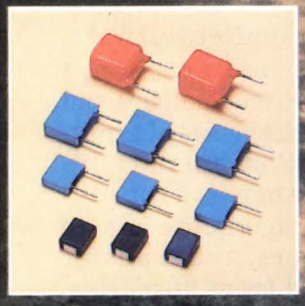

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CG/2000-264 WLM 119

SOFTWARE

APL software speeds development

Pocket APL, an inexpensive APL programming package, enables personal computer users to develop applications programs four to ten times faster than conventional languages, like Basic or Fortran. It saves development time by allowing multiple tasks to be executed in a single line and by eliminating the need to write routines that are incidental to the task. Additionally, Pocket APL serves as an on-line calculator for quick number crunching and analyses.

The software package requires a minimum of 128 kbytes of memory and runs on an IBM PC or PC-compatible computer equipped with PC-DOS or MS-DOS. An APL soft-character set is provided for computers with a graphics board or a color monitor; keywords are supplied for computers with a monochrome monitor.

STSC Inc., 2115 E. Jefferson St., Rockville, Md. 20852; (301) 984-5000. $95.

CIRCLE 319

Index accesses IC data base

Enabling design engineers to locate comprehensive data on integrated circuits by either a base number or the manufacturer's identification number with equal speed is the Integrated Circuit Part Number Index (ICPNI). Available on tape for VAX minicomputers or on floppy disk for use with any MS-DOS-compatible microcomputer, the index provides a quick means to access data in the Tech-Doc/Micro-Index—Inacom's components and materials data base.

Each listing in ICPNI directs the user to the exact location in Tech-Doc where the manufacturer's data sheets on the desired component can be found. Subscribers receive updated versions of ICPNI every 60 days.

Inacom International, 4830 S. Syracuse St., Denver, Colo. 80237; (800) 443-4636 or (303) 694-4200.

CIRCLE 320

Program eases project management

MacProject, a project-management tool for the Macintosh computer, enables the design of simple or complicated project schedules on the screen. The user enters the date on which the project is to begin, required task completion dates, resources, and fixed and variable cost data for each task. MacProject than calculates the beginning and ending dates for each task, as well as for the entire project. Furthermore, the program's "what if" analytical capability allows instant recalculation of dates, resources, and costs if variables are introduced into the project.

Apple Computer Inc., 20525 Mariani Ave., Cupertino, Calif. 95014; (408) 996-1010. $125.

CIRCLE 321

Unix-based OS runs fault-tolerant systems

Stratus USF, a Unix-based system facility, combines the functionality of a Unix environment with the power and reliability of fault-tolerant continuous processing. Operational across the entire family of Stratus/32 continuous-processing systems, USF offers an extensive library of Unix tools, utilities, and subsystems. It is fully integrated with VOS, the Stratus Virtual Operating System, and it allows applications to be easily ported from other Unix-based systems.

Stratus Computer Inc., 55 Fairbanks Blvd., Marlboro, Mass. 01752; (617) 460-2000. $8000 (one to 16 users); March, 1985.

CIRCLE 322

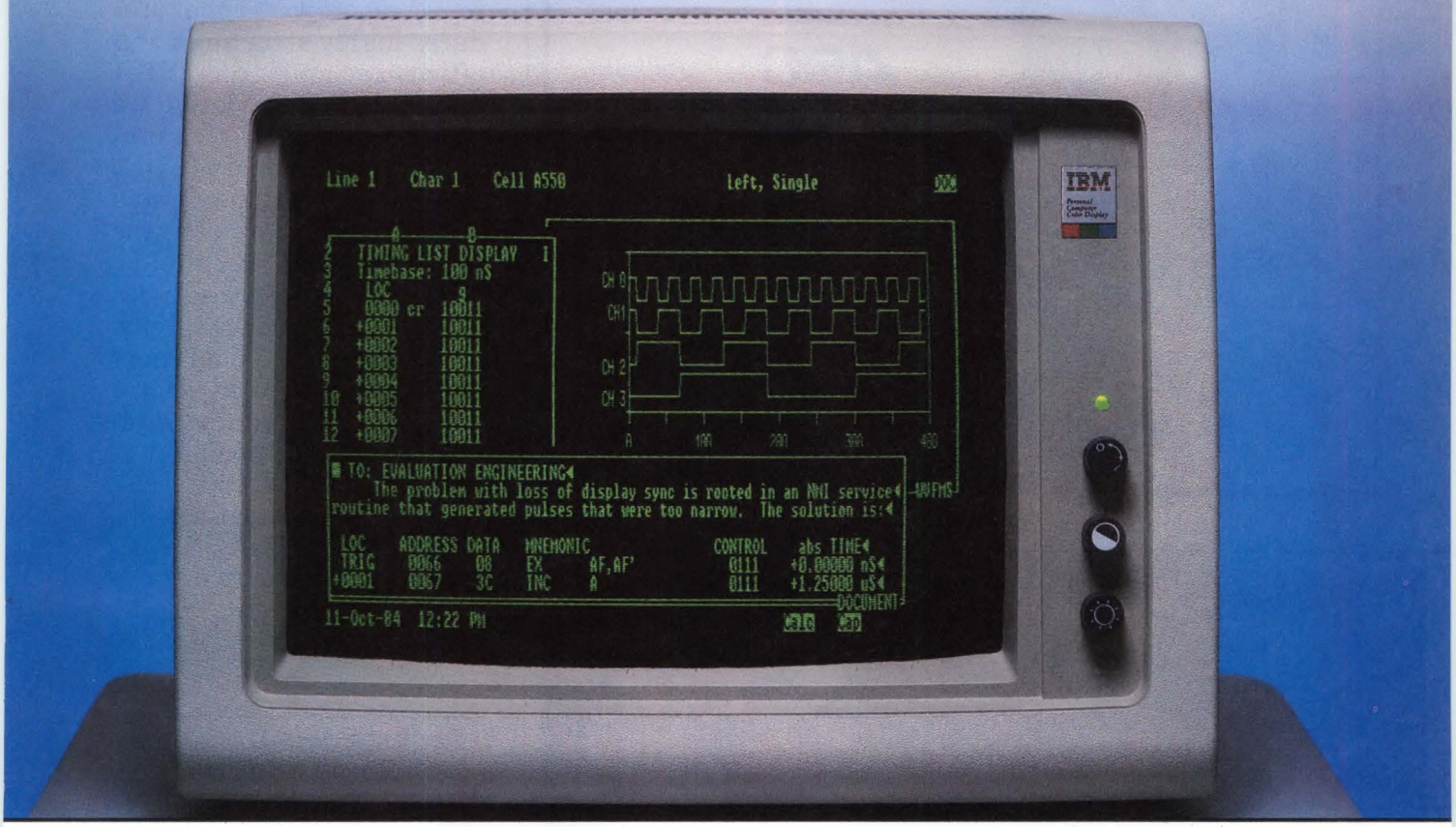
PC-DOS commands gain access to mainframes

With EComNet software, IBM PC users can access host mainframe facilities and files through the use of familiar PC-DOS commands. PC users on the network can utilize host storage, gain access to host printers, and transfer data to and from host files. EComNet can be installed on most IBM mainframes running the MVS 3.8, MVS/SP, or VM/SP operating system. The PC requires the Forte-PJ or PC78-2 communications board.

Forte Data Systems, 2205 Fortune Drive, San Jose, Calif. 95131; (408) 945-9111.

CIRCLE 323

Only our Logic Analysis Workstation can pass this screen test.



Why? Because it's the first system that combines logic analysis with an integrated software package on the new IBM PC AT*, PC XT* or IBM PC*. The μAnalyst LAW from Northwest Instrument Systems.

And what a logic analyzer! The μAnalyst brings you the industry's most powerful analyzer for under $10,000. Up to 80 channels of state acquisition with 15 trigger levels. 16 channels of 100 MHz timing acquisition, both conventional and transitional. Correlated state and timing displays. 8, 16, and 32-bit disassembly.

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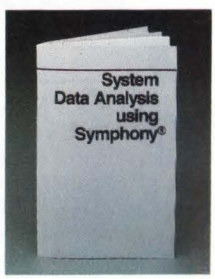
How well does it work? Very well, indeed. Contact us for a free application note on how the μAnalyst LAW works with Lotus software to provide unique and valuable engineering insights. While you're at it, ask for free technical literature and a demonstration.



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"For logic analysis, you can't beat the LAW."
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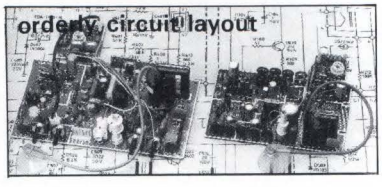

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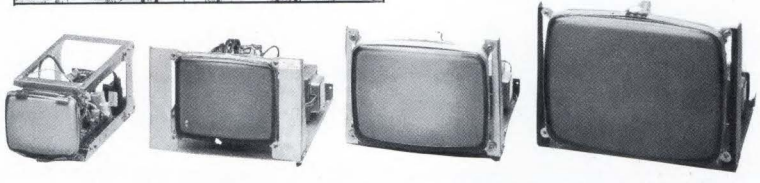
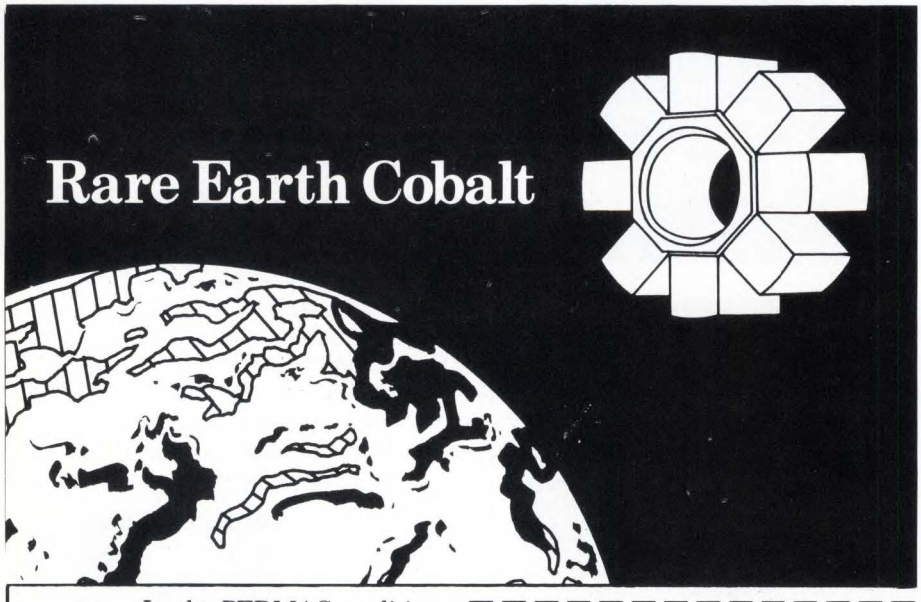


CIRCLE 139

Rare Earth Cobalt



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Business Controls Corp., 3-7 W. First St., Clifton, N.J. 07011; (800) 526-0161 or (201) 340-9893. $4500.

CIRCLE 324

Package lets DAS 9100 check VLSI devices

The latest DesignLink software package allows the DAS 9100 digital analysis system and the IBM PC to perform VLSI chip verification and test. A key program in the package allows response data acquired by the DAS 9100 to be uploaded to the PC and automatically compared with the data outputs of a simulation program, data acquired from a known-good device, or user-supplied data.

Tektronix Inc., PO Box 1700, Beaverton, Ore. 97077; (800) 547-1512 or in Oregon, (800) 452-1877. $1000.

CIRCLE 325

ANALOG

4-to-20-mA transmitter for process control shrinks down to one chip

A 4-to-20-mA voltage-to-current converter, or process control transmitter, is available for the first time as a monolithic circuit. Not only that, but the XTR110 from Burr-Brown is more versatile than many other transmitters: Not limited to use as a converter in standard process control applications, it can work in other applications as a current source. Furthermore, it costs approximately half that of hybrid implementations and an order of magnitude less than most modules.

Most transmitters convert their voltage inputs only into the standard 4-to-20-mA current, because that is the most popular for industrial process control in the U.S. However, the XTR110 has selectable output ranges as well of 0 to 20 mA, 5 to 25 mA, and others, for European or special applications.

This flexibility is made possible because, unlike its predecessor, the hybrid two-wire XTR100, the XTR110 is a three-wire transmitter, allowing the input signal to be to ground. (On the other hand, the device will not operate from loop power, a disadvantage in many applications.) The input signal range is selectable as either 0 to 10 or 0 to 5 V.

Another important feature is the 10-V ±0.2% reference output for exciting strain-gauge bridges, RTDs, and thermistors. This output can provide loads with up to 10 mA.

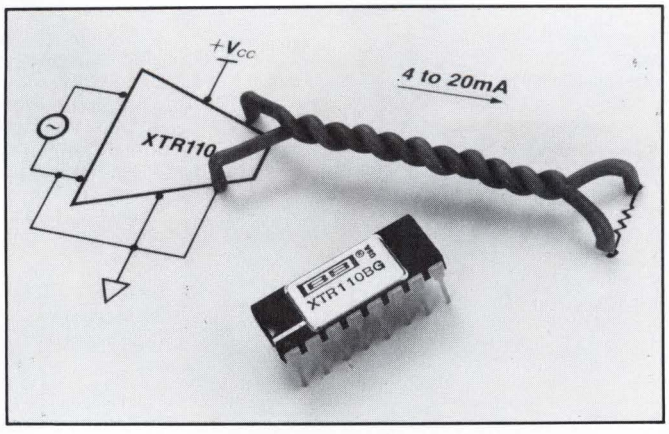
The chip is accurate, too. It is linear to within 0.01%, or 12 bits, fulfilling the standard requirements for virtually all process control applications. Moreover, its output drift with temperature is less than 0.005% of span per degree Centrigrade. This stability is achieved by requiring the use of a single additional part, a p-channel MOSFET, to handle the 4 to 20 mA. As a result, changes in the output current cause only minimal changes in the chip's temperature.

The XTR110 accepts a wide power supply range: A single supply of 13.5 to 40 V is all that is needed to power the device.

The converter costs $10.95 each in quantities of 100. Lots of 50 units or fewer are available from stock; larger orders require four to six weeks for delivery.

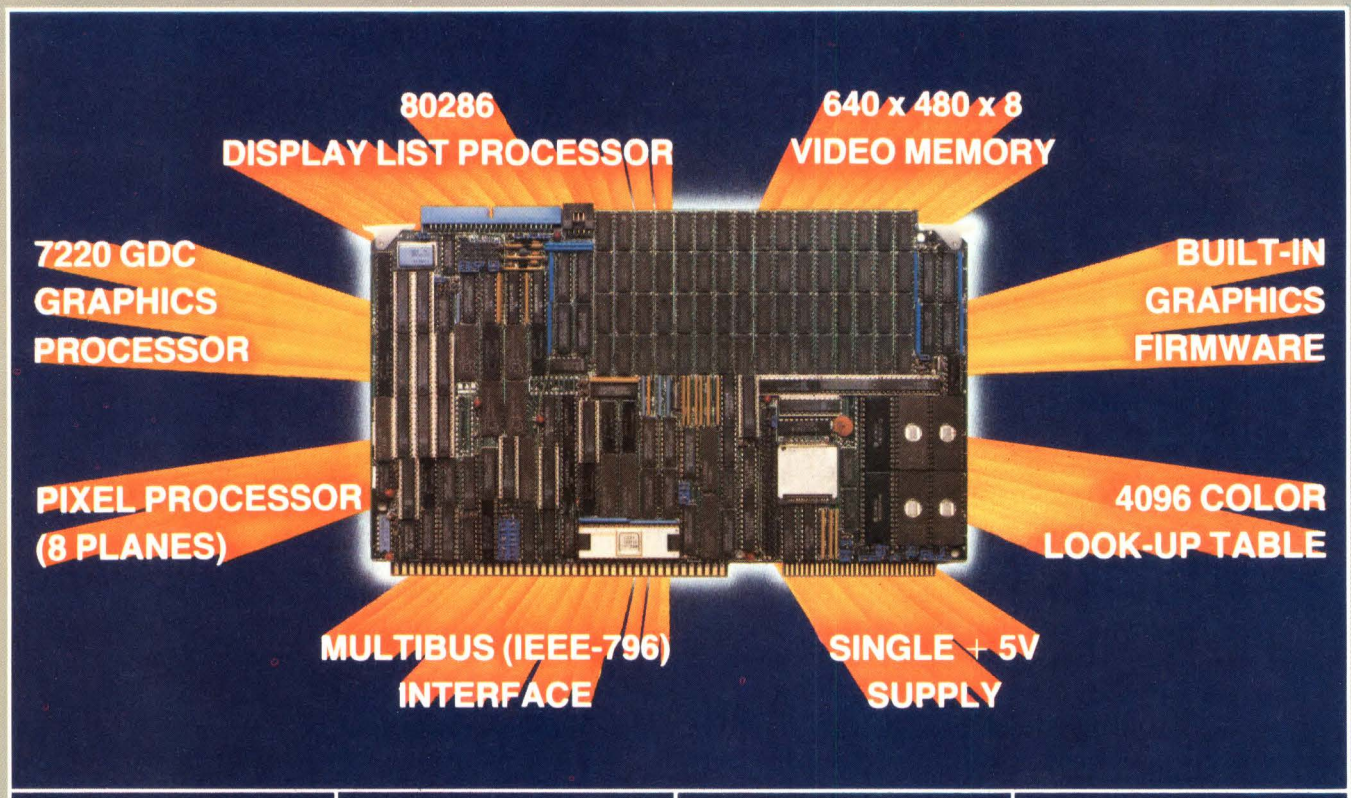
Burr-Brown Corp., PO Box 11400, Tucson, Ariz. 85734; Naresh Shah, (602) 746-1111.

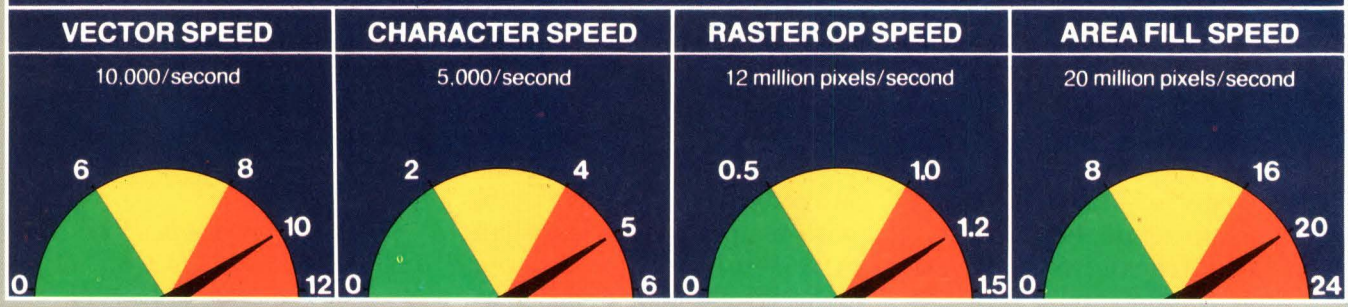
CIRCLE 315



Heather Bryce

BREAKTHROUGH IN MULTIBUS GRAPHICS!





SX-900 - The New Performance Standard For Color Graphics Boards

- **Powerful on-board graphics firmware**
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- **4096 color look-up table**
- **80286 display list processor**
- **7220 GDC graphics primitive processor**
- **8 plane pixel processor**
- **Built-in diagnostics**
- **Complete IEEE-796 (Multibus) interface**
- **+5V only power required**
- **10,000 vectors/second**
- **5,000 characters/second**
- **1,200,000 pixels/second raster ops**
- **20,000,000 pixels/second area fill**

The new Matrox SX-900 is a high performance color graphics display controller. It is the perfect solution for OEM manufacturers of process control and instrumentation equipment. The SX-900 is software compatible with the popular Matrox GXB-1000A high resolution display controllers, but occupies only a single Multibus card slot, and provides high speed drawing capability.

The hardware provides 640 x 480 pixel resolution, 4 or 8 bit planes, a 4096 color look-up table, and a 60Hz flicker free video refresh rate. The fast performance of the SX-900 results from a multi-processor pipelined architecture. A powerful 80286 CPU is used as the front end display list processor and is supported by a 7220 graphics primitive processor and a high speed pixel processor for simultaneous 8 plane drawing.

The SX-900 incorporates the proven on-board graphics firmware used by the GXB-1000. Over 256 high level display list commands are supported including line drawing, character drawing, circle and arc drawing, area fills, cursors and raster ops.

In addition to graphics boards, Matrox can also supply color monitors, cardcages, CPU cards, memory boards, and communications controllers for complete OEM display system requirements.

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ANALOG

Synchro converter tracks at 8 rps

The first synchro/resolver-to-digital converter to track at a rate of 8 revolutions per second, the SDC/RDC1711 from Analog Devices also boasts an overall accuracy to within ±1.3 arc-minutes and internal transformer isolation on both its signal and reference inputs.

The module accepts three-wire synchro or four-wire resolver inputs and has a reference frequency range of 360 Hz to 2.6 kHz. A 16-bit unit, it resolves 19.8 arc-seconds and responds to a 179° step in 250 ms maximum.

Tracking is continuous, with no conversion commands or status wait loops. Latched three-state outputs provide an easy interface with 8- or 16-bit data buses, so that data can be transferred without disturbing the converter's tracking.

Because the unit is a ratiometric device, operating on a type 2 servo loop principle, it can reside at a distance from the synchro or resolver without suffering any loss of accuracy from voltage drops. Noise rejection on the input lines is provided by an internal phase-sensitive detector.

The device is capable of driving six TTL loads and has separate Enable inputs for both the high and the low input byte.

The maximum signal impedance is 50 kΩ for an 11.8-V signal, 100 kΩ for a 26-V signal, and 300 kΩ for a 90-V signal. The allowable phase shift between signal and reference is ±20°.

The converter requires +5- and ±15-V power supplies and dissipates a maximum of 3.65 W. It stands 3.125 by 2.625 by 0.4 in. and comes in versions for the commercial and military temperature ranges.

The price for lots of 25 to 99 of the commercial version is $518 each. Delivery is in six to nine weeks after the receipt of an order.

Analog Devices Inc., 2 Technology Way, Norwood, Mass. 02062; Richard Parker, (617) 329-4700.

CIRCLE 317

Gary Elinoff

ANALOG

Fast converters consume little power

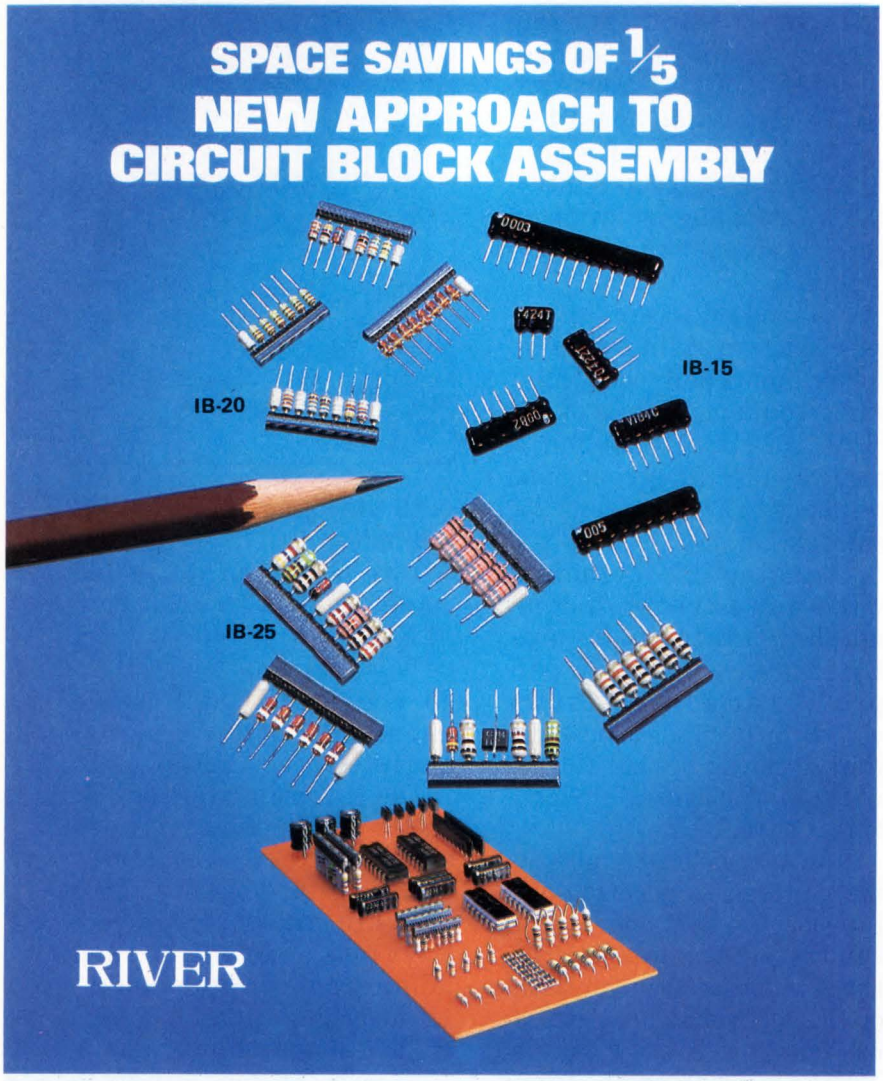
Two NMOS converters for video signal processing—the PNA7518 8-bit d-a and the PNA7507 7-bit a-d—combine high speed with low power consumption. The 30-MHz d-a converter settles to within 1 LSB in 40 ns and consumes 200 mW. Housed in a 16-pin dual-in-line SOT-84B package, the 7518 has transparent latch inputs and requires no deglitching circuits on the outputs.

The PNA7507, a 15-MHz a-d converter, offers a typical conversion speed of 160 ns and consumes 350 mW. Its output can be in two's complement or binary-coded format. The 24-pin IC, encapsulated in a dual-in-line SOT-101A package, operates from supply voltages of 5 and 12 V.

Philips Elcoma, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 757005; Telex: 51573.

Signetics Corp., 811 E. Arques Ave., Sunnyvale, Calif. 94086; (408) 739-7700.

CIRCLE 326



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CIRCLE 142

Data separator chip replaces 10 TTL devices

Designed specifically for use with the WD1010/2010 hard-disk controller, a self-adjusting Winchester disk data separator and write precompensation chip saves pc board real estate by replacing 10 TTL devices. The chip also provides a higher tolerance to bit jitter than previous data separators.

Designated the WD10C20, the device is capable of reading or writing data at 5-MHz. Its three major functional sections comprise a crystal-controlled reference oscillator, data timing and precompensation circuits, and a phase-locked VCO.

Western Digital Corp., 2445 McCabe Way, Irvine, Calif. 92714; (714) 863-0102. $30 (100 units).

CIRCLE 327

COMPUTER BOARDS

Host adapter board gives the IBM PC family access to SCSI devices

A host adapter board is the first to allow the IBM PC to work with SCSI (Small Computer Systems Interface) devices. The ASC-88, from Advanced Storage Concepts, fits directly inside the IBM PC, PC XT, PC AT, or compatible personal computer and connects directly to the 50-pin ribbon cable of the SCSI bus.

Previous IBM PC host adapters provide for only the SASI bus. That bus (basically a subset of SCSI) accomodates only one peripheral. The SCSI bus, in contrast, provides for 8 devices now (including the host) and will likely soon support 64—which the ASC-88 will be able to handle.

The board works at the fastest data rate defined by the SCSI standard, 1.5 Mbytes/s. Further, to enhance performance it supports the disconnect-and-reconnect feature so critical in multiple-device systems. With this feature, a device can disconnect itself from the bus during an access. The bus may then be used by other devices, increasing the effective bus bandwidth substantially.

Heather Bryce

The ASC-88 remembers the system pointer information—command, data, and status—for each device that has disconnected in preparation for reconnection.

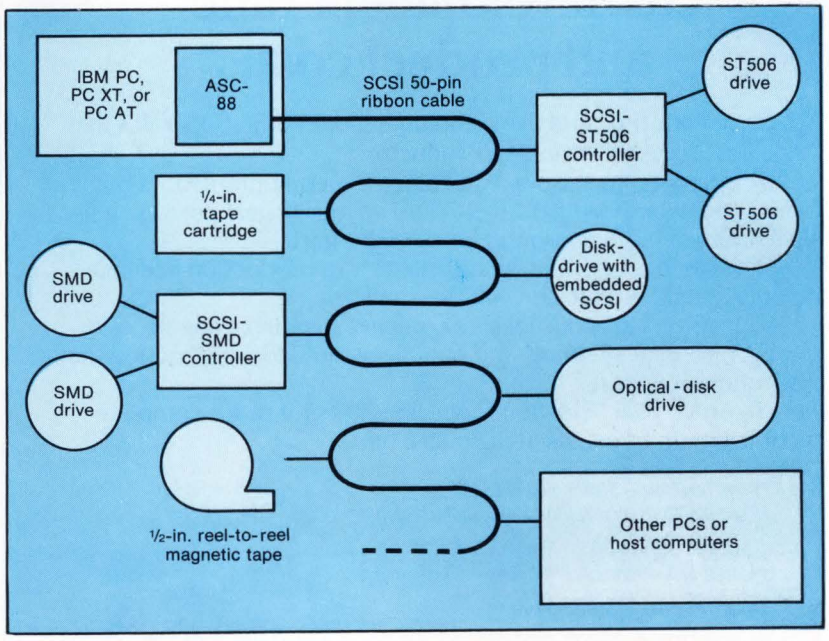
The ASC-BIOS on the board provides user calls to the SCSI command set. It allows direct emulation of fixed-disk BIOS commands and also arbitrates among the various devices.

Menu-driven configuration software, stored on a floppy disk, asks the user for configuration information and stores it in an EEPROM on the board. Thus the user need define the system only once.

A single board plus the configuration software costs $249. It will be available in January, with delivery in two weeks.

Advanced Storage Concepts Inc., 9800 Hillcroft, Suite 325, Houston, Texas 77096; (713) 729-6388.

CIRCLE 314



Serving as an SCSI–IBM PC host adapter, the ASC-88 enables seven peripheral devices of various types to be connected in an IBM PC system. It supports the future extension of SCSI to 64 devices.

COMPUTER BOARDS

Interface links IBM PC with VMEbus

Linking the IBM PC with the VMEbus is an interface package that enables the computer to act as a master controller for a VMEbus-based system. The package consists of two plug-in boards (one for the PC and one for the VMEbus), cable, and system software.

The PC/VME interface meets the timing requirements of both the IBM PC and the VMEbus system. Function cards can be assembled and verified independently of the 68000-based controller card. Programs for data acquisition, process control, and robotics, to name a few, can be written in almost any language, from simple Basic to advanced Forth.

Ajida Technologies, 2226 Durant Ave., Suite 309, Berkeley, Calif. 94704. (415) 548-6434.

CIRCLE 328

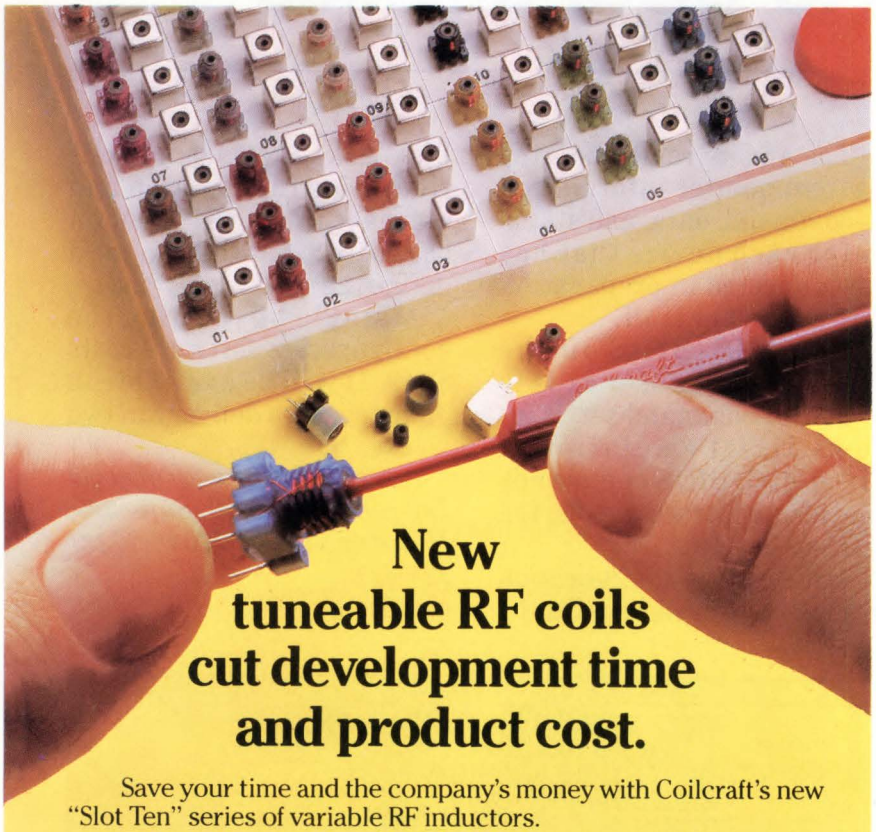
Single-board computer runs IBM PC programs

The AD-88, an IBM PC-compatible single-board computer, runs applications software written for the PC under MS-DOS. What's more, the AD-88 features an on-board video controller and a floppy-disk controller. Additionally, it offers one serial port, one printer port, and 128 kbytes of dynamic RAM. (A 512-kbyte version is also available.)

The use of standard programmable logic chips allows the implementation of a full microcomputer system on a single double-layer Eurocard with dimensions of 9.2 by 9 in. A stand-alone system can be constructed by simply adding a power supply, a disk drive(s), a keyboard, and a monitor.

Advanced Data Processing Systems, PO Box 10417, San Jose, Calif. 95157; (408) 446-9332. $880.

CIRCLE 329



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CIRCLE 144

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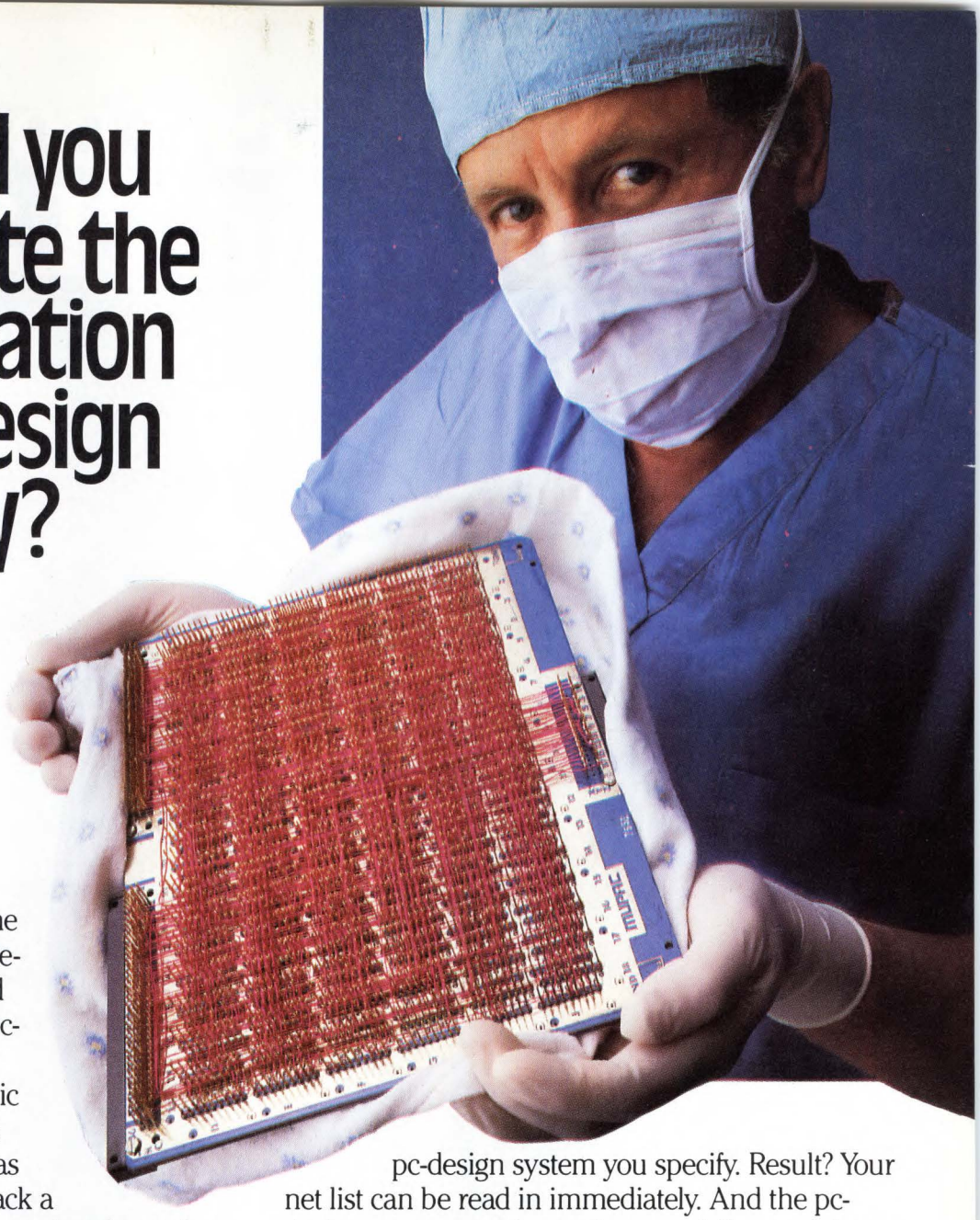

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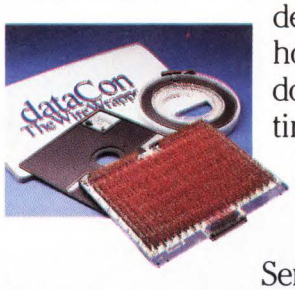

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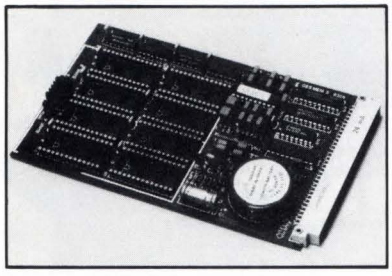
COMPUTER BOARDS

Eurocards accept RAM/EPROM devices

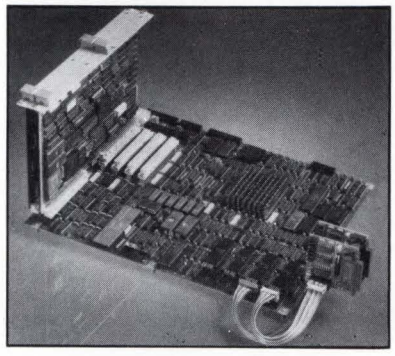


Two universal memory boards conform to the single-height Eurocard form factor (100 by 160 mm) and are compatible with the standard G-64 bus. The GESMEM-3 board has an 8-bit data path, while the GESMEM-2A has a 16-bit data path. The Eurocards each have two totally independent memory blocks, consisting of four sockets per block. Each block can be placed anywhere in the memory map and can be individually configured with RAM or EPROM devices. When the boards are populated with EPROM devices, the maximum capacity is 256 kbytes; using CMOS RAM chips, the maximum capacity is 64 kbytes. The latter can be powered from the standby power line on the G-64 bus or from an optional on-board lithium battery.

Gespac Inc., 550 E. Grandview, Mesa, Ariz. 85203; (602) 962-5559. $175 and $225 for the 8- and 16-bit boards, respectively (unpopulated).

CIRCLE 330

Multifunction SBC packs dual processors

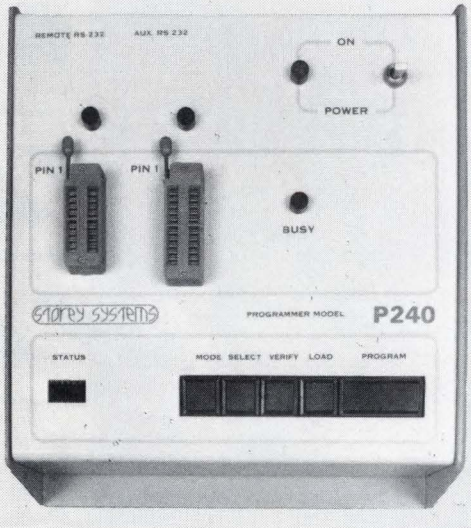


Easing systems integration is a single-board computer that combines the functions of nine individual cards. Called the Baseboard, the VMEbus-compatible microcomputer employs two processors—a 68010 CPU with virtual memory and demand paging and a 68008-based disk controller. The latter supports a mixture of three ST506, ESDI, or ST412HP Winchester disk drives, plus four 5¼-in. floppy disk drives. The former includes up to 2 Mbytes of dynamic RAM and an optional Unix Version 5.2 operating system.

For multi-user, multitasking environments, the Baseboard offers five built-in VMEbus expansion slots and eight independently programmable serial ports. Up to 32 additional users can be added with VMEbus serial cards. The system accommodates single- and double-height VMEbus modules to permit optimum configuration flexibility.

Interphase Corp., 2925 Merrell Road, Dallas, Texas 75229; (214) 350-9000. $5995.

CIRCLE 331



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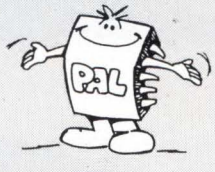

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CIRCLE 147

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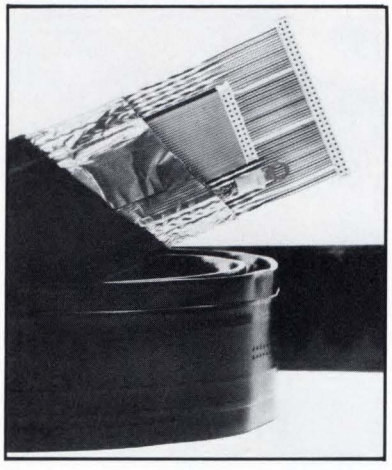
CIRCLE 148

PACKAGING & MATERIALS

Cable assembly is shielded, jacketed



Used for interfacing disk drives and other peripheral equipment, an A&B flat cable assembly consists of Vari-Twist cable and ground plane cable covered with a Beldfoil aluminum-polyester shield. The shield provides optimum protection from electrostatic discharge and interference at audio and radio frequencies. The PVC-jacketed assembly is an attractive alternative to bulky and more costly zipper tubing.

Belden 9V28060 Vari-Twist is used as the A cable. Vari-Twist reduces crosstalk by the use of twisted pairs, but it can be mass-terminated in programmed flat sections with any IDC connector. It has 30 28-gage stranded pairs with conductor spacing of 0.050 in. Controlled-impedance 9GP1026 ground plane cable is used as the B cable.

Belden Electronic Wire and Cable, 2000 S. Batavia Ave., Geneva, Ill. 60134; (312) 232-8900. $650.33 per 10 ft (in quantities of 1000 ft).

CIRCLE 332

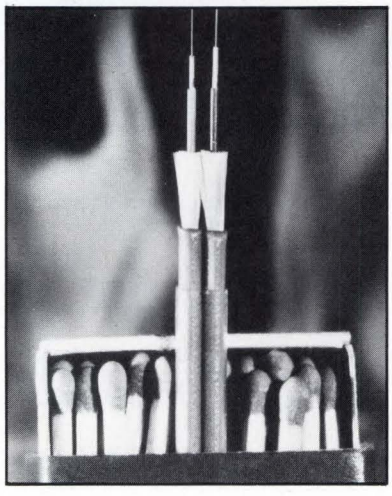
Interconnection kit eases prototyping

Containing $500 worth of ready-to-use interconnects for only $99, the Prototyper's Lab Kit allows designers to quickly check out prototype designs without hard wiring. It contains a selection of Sculptured flexible interconnects and a sample of the SNAP connector, a zero-insertion-force device with twice the density of standard insulation-displacement connectors. The kit also suggests improved interconnection methods.

Advanced Circuit Technology Inc., PO Box 547X, Nashua, N.H. 03061; (603) 880-6000.

CIRCLE 333

Optical cables meet UL, NEC safety codes



A family of fiber-optic cables has been tested and classified to the Underwriters Laboratory and National Electrical Code requirements for direct air plenum installation. Designed to comply with the low-smoke and minimum flame-spread requirements of the UL 910 and NEC 770 safety codes, the true plenum-rated optical cables make the installation of local area networks and building distribution systems economically practical.

The PL series is available in 2 through 10 fiber configurations, with both 50- and 100-μm core waveguides.

Phalo Corp., Optical Systems Division, 900 Holt Ave., Manchester, N.H. 03103; (603) 669-4347.

CIRCLE 334

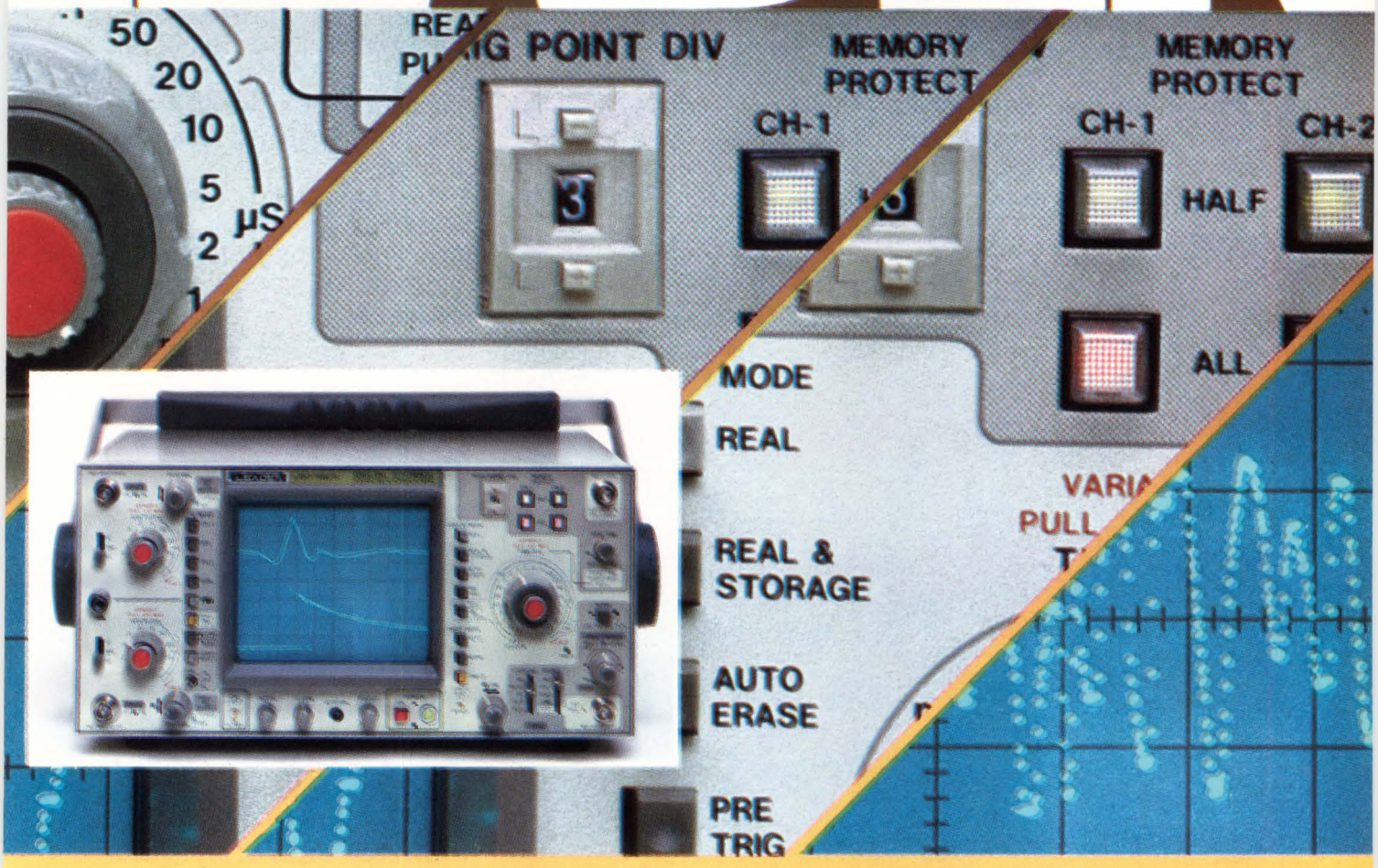
Hand lotion won't contaminate pc boards

Developed exclusively for the electronics industry, IC Lotion contains no silicone, lanolin, mineral oil, or other types of ingredients commonly found in hand care products that can contaminate pc boards and adversely effect solderability. Although circuit contamination due to hand contact is certainly not limited to the use of conventional hand care products, this type of contamination can be eliminated by IC Lotion. In addition to being non-contaminating, the lotion also creates a moisture layer that assists in static discharge. IC Lotion is cosmetically formulated to meet the user's approval as well.

R&R Lotions, 4251 N. Brown Ave., Suite A-3, Scottsdale, Ariz. 85251; (602) 941-1475.

CIRCLE 335

LEADER



The Next Generation Digital Storage Oscilloscope.

Only the LBO-5825 has: Two Separate A/D Converters, True 5-MHz Digital Sampling Rate, Non-Volatile Memory, 35-MHz Analog Bandwidth, and a Very Affordable Price!

Makes other digitals obsolete.

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Matchless features and performance.

No other Digital Storage Oscilloscope equals the 2-channel LBO-5825's performance, versatility, and value: most other units in its class have a 1 or 2-MHz digital sampling rate and share a single A/D converter between channels. But, we gave the LBO-5825 a true 5-MHz sampling rate to provide higher resolution, even on fast single-shot signals. Two separate A/D converters ensure super-accurate, simultaneous, point-by-point, channel comparisons. An 8-bit, 2-channel by 1K-word non-volatile memory enables you to compare a real waveform to a stored reference or to record field-service waveforms for comparison in the shop. Its 14-day battery backup protects memory between charges or if ac fails. Up to 9-division pre-trigger view isolates transient causes. Roll mode makes the CRT read like a chart recorder. X-Y outputs are supplied for hard copies. The LBO-5825 is also a rugged Real Time Oscilloscope with a two-year warranty.

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CIRCLE 206 FOR PRODUCT DEMONSTRATION

CIRCLE 207 FOR PRODUCT INFORMATION

PACKAGING & MATERIALS

Kit allows speedy pc board repairs

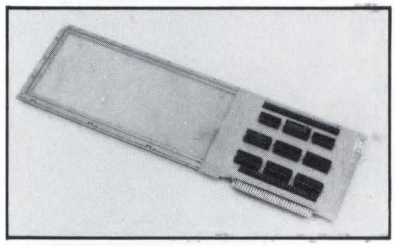
Containing an assortment of adhesive-backed copper products, the E-Z Circuit kit enables burnt, broken, and lifted circuitry on printed circuit boards to be quickly repaired or modified. The kit includes conductive tape, donut pads, and a 5-by-6-in. copper sheet, plus a roll of polyester insulating tape. The E-Z Circuit kit offers flexibility not found with conventional repair or modification techniques and provides an alternative to scrapping damaged boards.

Bishop Graphics Inc., 5388 Sterling Center Drive, Westlake Village, Calif. 91359; (818) 991-2600. $14.95.

CIRCLE 336

CIRCLE 150

Prototyping board plugs into IBM PC

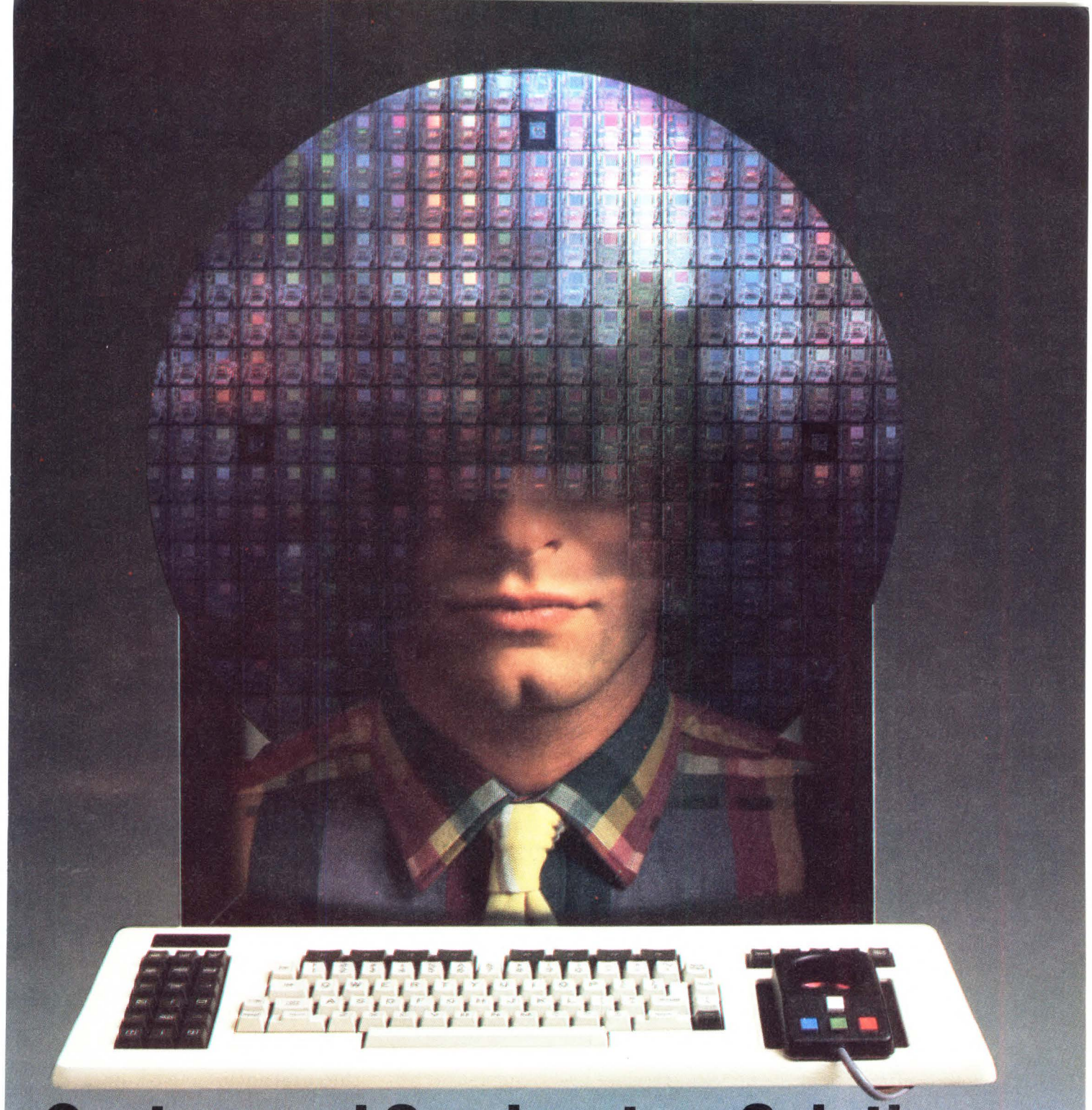


Providing a means to interface prototype circuitry with the IBM PC is the eZ Card. The board has two areas for building prototype circuits, the larger of which accommodates over 60 wire-wrapped sockets. The smaller prototyping area is for mounting I/O connectors. Users may also develop and debug prototype circuits on the solderless eZ Board and transfer them to the eZ Card.

The eZ Card's on-board DIP switch permits the selection of up to eight unique addresses, covering the entire I/O address range of the IBM PC. The fully buffered address, data, and control bus signals are accessible at wire-wrapped terminals.

Sabadia Export Corp., PO Box 1132, Yorba Linda, Calif. 92686; (714) 630-9335. $89.95; stock to four weeks.

CIRCLE 337



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CIRCLE 181

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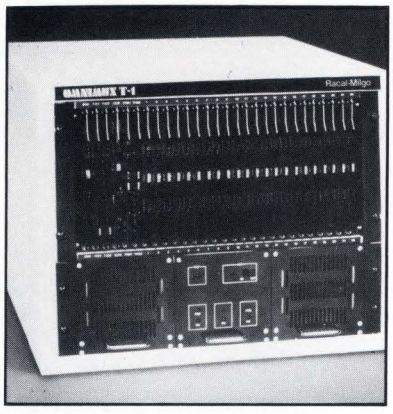
COMMUNICATIONS

Multiplexer supports 1.544, 2.048 Mbits/s



The Omnimux T-1, a time-division multiplexer, mixes voice with asynchronous and synchronous data for efficient high-speed transmissions. It combines up to 96 data and voice channels over wideband circuits and supports both 1.544- and 2.048-Mbit/s data rates.

The multiplexer handles voice channels with bandwidth requirements of 16, 32, 48, and 64 kbits/s, and data channels with rates from 110 bits/s to 460.8 kbits/s. These features may be combined and varied to meet design requirements, ranging from simple point-to-point systems to cascaded and multinode configurations.

Racal-Milgo, 8600 NW 41st St., PO Box 520399, Miami, Fla. 33152; (305) 592-8600. $35,000 (44 RS-232-C synchronous channels).

CIRCLE 338

1200-baud modem sells for $299

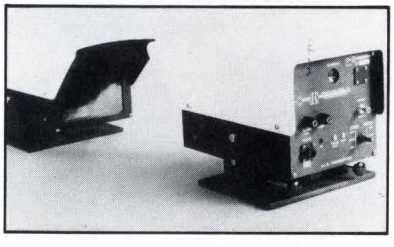
For unattended operation at an economical price, the Volksmodem 12 provides 300/1200-baud operation and automatic dialing and answering capabilities for only $299. The modem, which comes with cables for connecting it with most computers, operates asynchronously for full- or half-duplex transmissions.

The Volksmodem 12 can be configured for DCD (data carrier detect) and DTR (data terminal ready) operation. The unit is powered via a 12-V dc, 60-mA adapter.

Anchor Automation Inc., 6913 Valjean Ave., Van Nuys, Calif. 91406; (818) 997-7758.

CIRCLE 339

Atmospheric system transmits T-1 signals



An optical infrared system transmits T-1 (1.544-Mbit/s) signals through the air at distances of up to 1.5 miles. The transmitter/receiver pairs, complete with T-1 interface boxes, transmit the data stream license-free as an alternative to microwave, telephone, cable, and fiber-optic transmissions.

The Model ALS829-T1 can be used in numerous applications requiring short-range line-of-sight transmissions. The user simply introduces a T-1-formatted signal (any combination of data and voice channels) to the interface box. Coaxial cables carry the signal from the box to the transmitter. The signal is then transmitted on an invisible low-power beam of light to the receiver. When securely mounted and aligned, the transmitters and receivers provide a secure and reliable link that is immune to interference.

American Laser Systems Inc., 106 Fowler Road, Goleta, Calif. 93117; (805) 967-0423. $14,000 for full-duplex capability.

CIRCLE 340

Switching system cuts networking costs

PACX 2000 is a software-controlled distributed switching system that functions as both a local and a wide area network. It helps reduce networking costs by improving transmission facility utilization. The system links groups of workstations together and connects these groups to corporate mainframe computing centers (as opposed to centralized networking).

The PACX 2000 is based on the international 64-kbit/s digital communications standard, enabling it to support transparent asynchronous data at speeds of up to 19.2 kbits/s. Expansion is accomplished by simply adding interface modules or gateways to outside private and public networks.

Gandalf Data Inc., 1019 S. Noel, Wheeling, Ill. 60090; (312) 541-6060.

CIRCLE 341

We've got the power and the proof.

Whether you're designing in power for high drain portable tools or fail-safe on-board memory backup, Sanyo has the dependable nickel cadmium batteries you need. Standard versions can provide from 50 mAH to a full 10.0 AH. And there are also Quick Charge, one hour fast charge, high temperature, memory backup and complete battery pack assemblies.

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The proof of Sanyo superiority can be found in our hundreds of satisfied customers. Demanding customers who subject incoming Sanyo batteries to the strictest inspection standards. Result? Sanyo batteries consistently exceed customer specs for quality. So much so in fact, that we've been named "Vendor of the Year" several times by some of the toughest customers around.

For quality and dependability, Sanyo delivers. We'd like to be able to convince you with the proof. Contact Sanyo for complete technical information on Sanyo nickel cadmium and lithium batteries.

CIRCLE 182

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Los Angeles Office
West Artesia Blvd.
Compton, CA 90220
(213) 537-5830

COMMUNICATIONS

Chip set offers 2-Mbaud token passing

A two-chip set transmits and receives digital data at speeds of up to 2 Mbauds over IEEE-802.3-compatible local area networks. The FSK modem transmitter and receiver, designated the NE-5080/NE5081, can be used in LANs providing either point-to-point or token bus service. A modem built with these ICs offers a dynamic range exceeding 30 dB and a bit error rate of 10^{-12}

In point-to-point applications, the chip set can implement a ½-Mbit/s full-duplex data link between computers as far apart as 15 km. When used in token bus architectures, the chips allow the carrier frequency to be adjusted between 50 kHz and 20 MHz.

Philips Elcoma, PO Box 523, 5600 AM Eindhoven, the Netherlands; (040) 757005; Telex: 51573.

Signetics Corp.. 811 E. Arques Ave., Sunnyvale, Calif. 94086; (408) 739-7700.

CIRCLE 342

2400-bit/s modem performs auto log-on

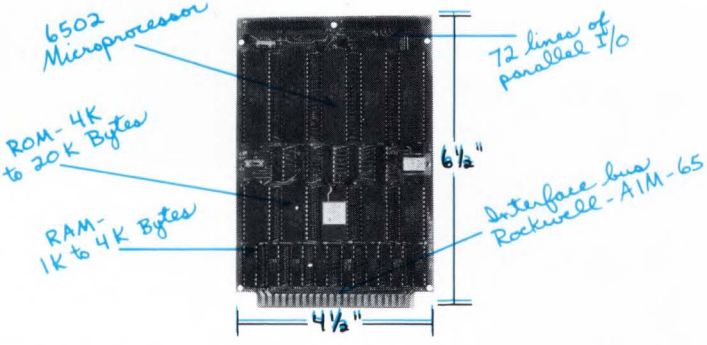
The recent addition to the DialNet 3000 modem line, the Model 3024+ is an autodialing 2400-bit/s unit that automatically logs onto a host computer. It allows synchronous or asynchronous full-duplex transmissions to be sent over the two-wire dial telephone network. At $895, the 3024+ costs less than most modems having the same features.

In addition to 2400 bits/s, the modem has a secondary 1200-bit/s transmission mode. The unit's autodialer supports both pulse and tone dialing, and the two modes can be mixed within a number to ensure access to all long-distance carriers.

Micom Systems Inc., 20151 Nordhoff St., Chatsworth, Calif. 91311; (213) 998-8844.

CIRCLE 343

6502 BASED MICROCOMPUTER FOR INDUSTRIAL APPLICATIONS



When you buy a microcomputer from Cubit, we don't forget you need software and peripherals to talk to it.

Cubit starts with an inexpensive board based on the 6502 microprocessor. We have 72 lines of I/O and plenty of memory, but that is just the beginning.

You can add a 20 character display, or a CRT, a printer and any of several keyboard options. And you can program the board in any of the Rockwell languages: Assembler, FORTH, BASIC, PL/65 or PASCAL. Include our EPROM Programmer, and you have a complete development system for under $1,000.

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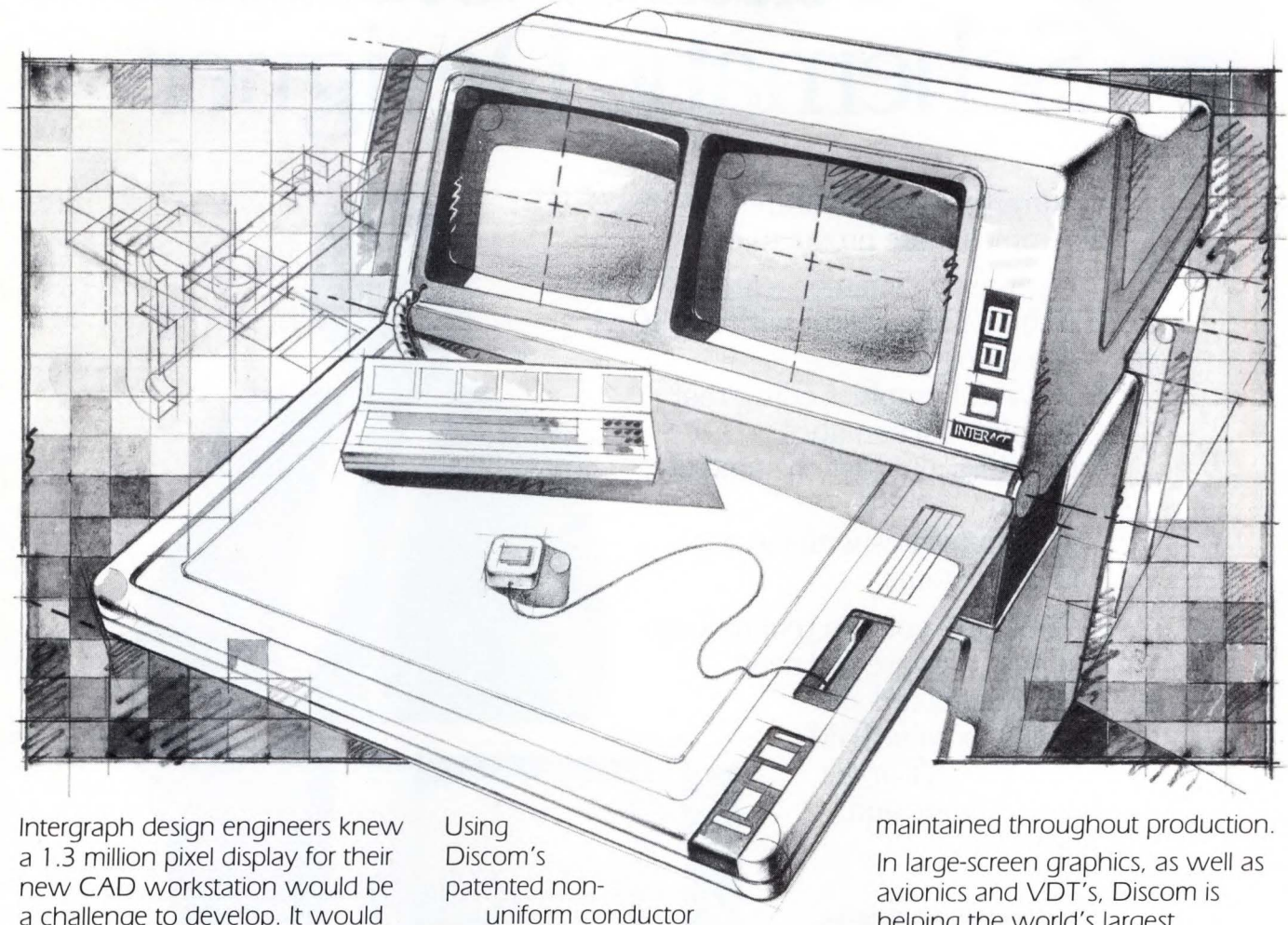
CIRCLE 183

THE CHALLENGE:

Develop a yoke that will produce a 1.3 million pixel display on a 20-inch CRT screen.



Intergraph design engineers knew a 1.3 million pixel display for their new CAD workstation would be a challenge to develop. It would require a deflection yoke with a very wide deflection angle and very tight geometry. That by increasing resolution, they could reduce operator strain.

So they turned to Discom. Taking advantage of Discom's thirteen-plus years of developing components that have continually raised the state-of-the-art in display technology, Intergraph engineers were able to realize their objectives.

Using Discom's patented non-uniform conductor distribution process, Discom engineers developed a yoke with a 114° deflection angle and less than 1% geometry tolerance. And 1000 line resolution. Then Discom's full-capability prototype lab built prototypes for testing and evaluation.

And, when they were ready for production, Intergraph again turned to Discom. They knew Discom's precision stator construction would assure that design tolerances would be maintained throughout production.

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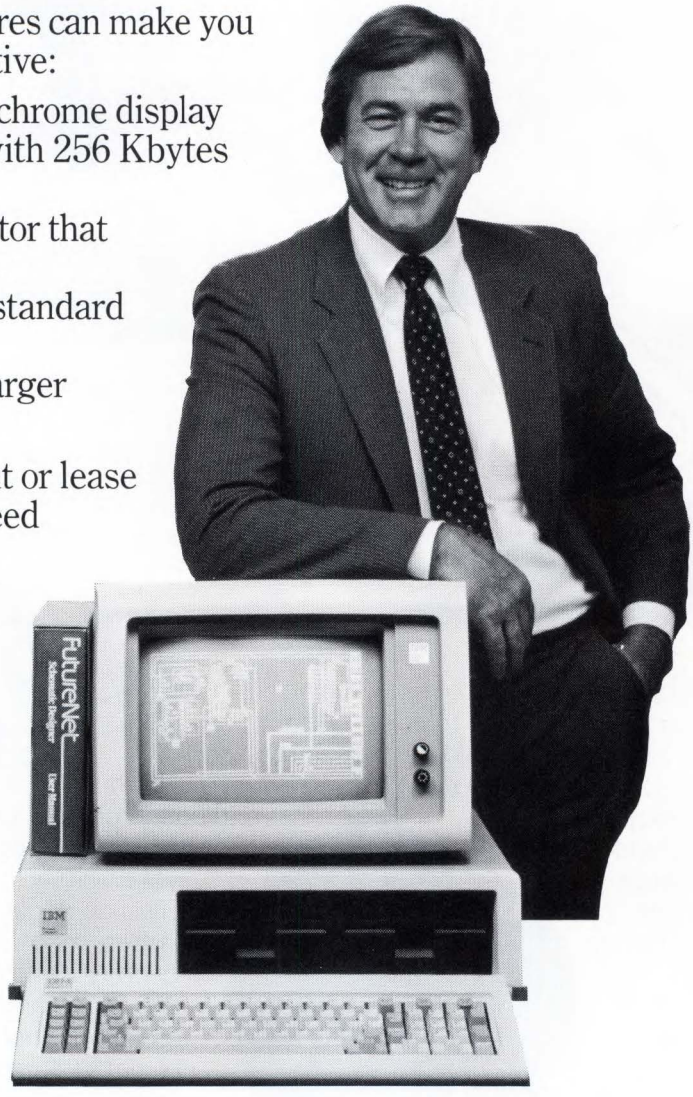
With USIR, you can rent or lease just the software you need (including board and mouse) for your IBM PC, XT, or AT or get both software and hardware.



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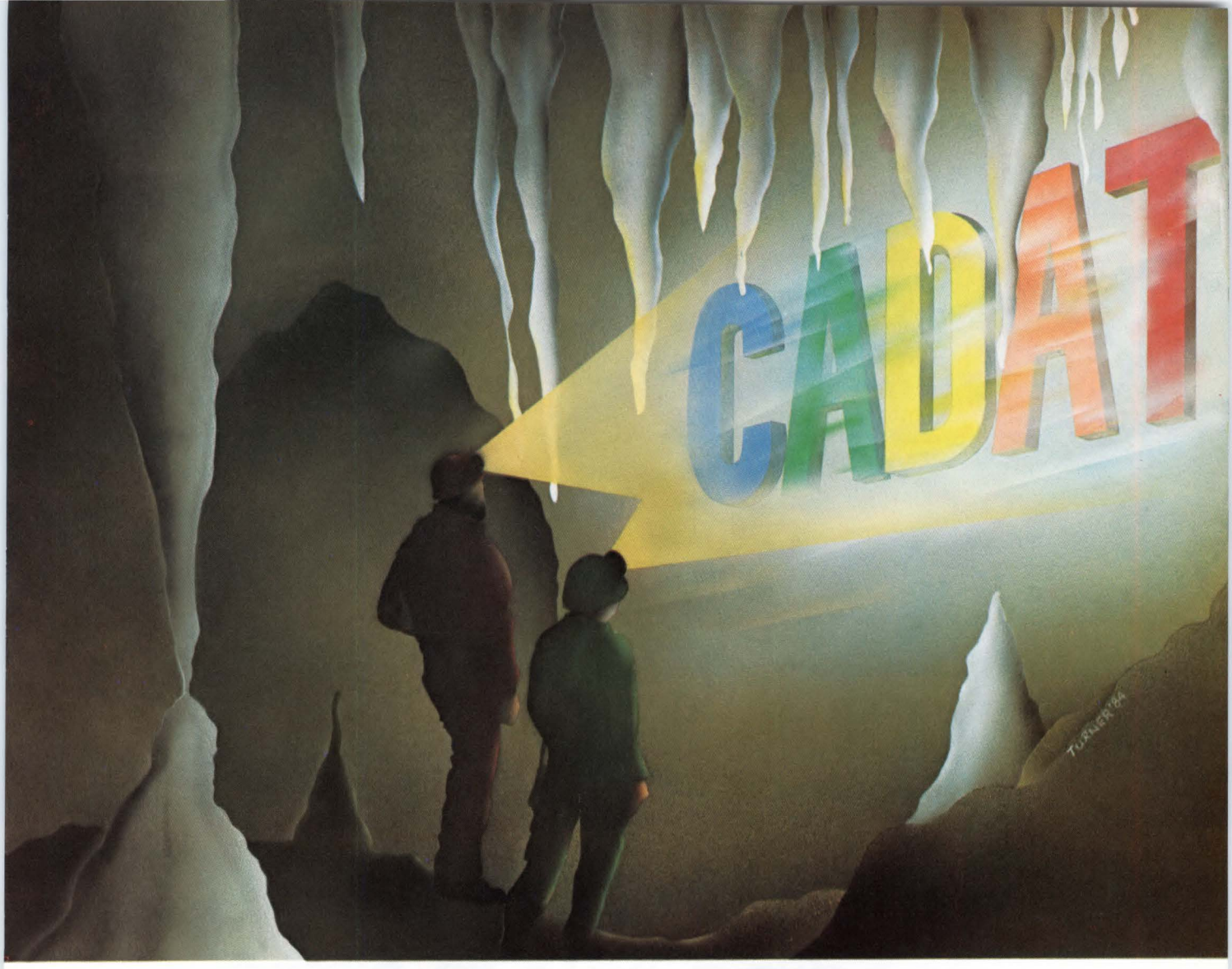

The Missing Link Isn't Missing Any Longer.

Never has a simulation system linked the functions of design and test. *That is*, until the discovery of CADAT, the only simulator that supports MOS design verification and concurrent functional fault simulation.

CADAT succeeds where other systems have yet to venture.

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CADAT also has an abundant graphics capability that greatly facilitates the design and test functions and ensures the design engineer optimum performance.

These are just some of the many reasons why CADAT, the most cost-competitive system available, is so widely distributed.

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CIRCLE 187

Mepco//Electra Film Capacitor Typical Characteristics

	Polyester	Polycarbonate	Polypropylene	Polystyrene
Operating Temp. °C	−55°C to +125°C	−55°C to +125°C	−55°C to +105°C	−55°C to +70°C (85°C)
Dissipation Factor %1KHz 25°C	1.0% MAX	.3% MAX	.1% MAX	.1% MAX
Dielectric Constant (Practical)	3.1	3.0	2.2	2.5
% Capacit. Change (Temp. Range)	−6% to +16%	±2% Over Temp.	±2% Over Temp.	−120 to ±60 PPM/°C
Relative Cost	Low	Med.	Med.	High
Cautions	None	Humid	Temp.	Temp.

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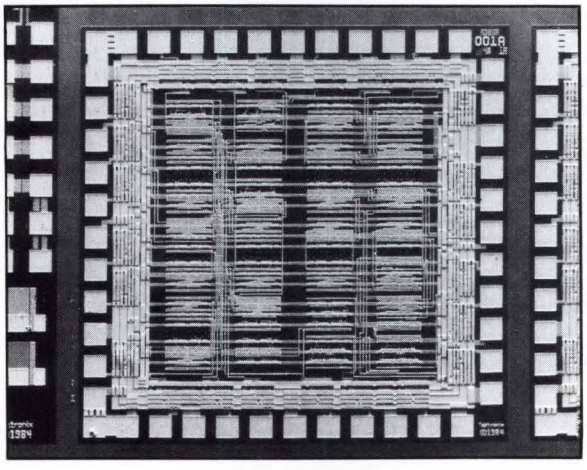
DIGITAL ICs

GaAs arrays appear—with digital, analog cells



When the performance of ECL gate arrays is not fast enough or gigahertz analog circuits cannot be made in silicon, the Quick Chip "cell" array fits the bill. The first commercial semicustom array in gallium arsenide, it is intended for systems that operate at clock rates above 500 MHz, implementing digital functions with clock rates as high as 2 GHz and analog circuits with bandwidths of up to 5 GHz (ELECTRONIC DESIGN, Nov. 29, p. 217).

On the chip are 28 prediffused cell regions—each of which contains 20 depletion-mode transistors, 8 diodes, and 12 resistors—plus 24 I/O buffers that can be tailored for either ECL, TTL or CMOS signal levels. With ECL compatibility, the output signal rise times are about 200 ps. For digital circuits, buffered FET logic is used, which requires both positive and negative power supplies.

Circuit customization is done by two levels of metal interconnections. For more sophisticated needs, more processing steps can be added, and special customizing can be done as well. Such choices would, of course, require more design time.

The chip is housed in a specially developed leadless chip carrier. Just 0.42 in. on a side it contains chip-bypass capacitors, for power-bus decoupling. With a heat sink, the package dissipates a maximum of 3 W in still air.

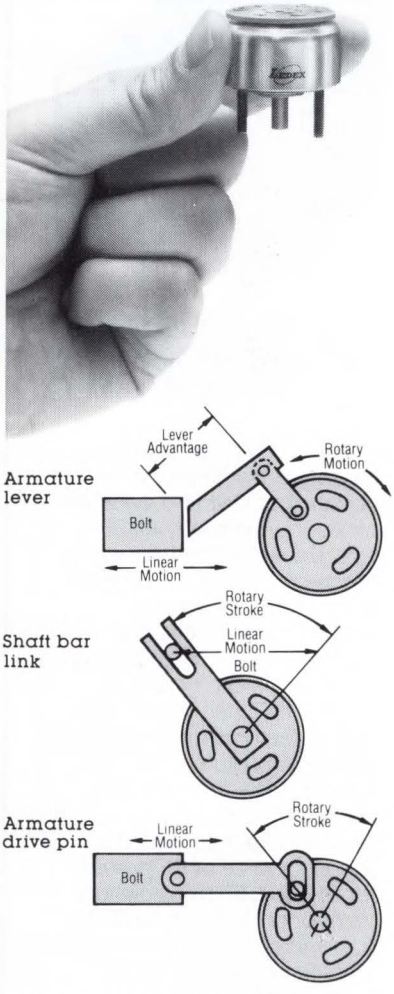
The minimum cost is $55,000, from design to first sample. Delivery time is nominally about 12 weeks after submission of a final circuit net list.

Tektronix Inc., PO Box 500, M/S 59-600, Beaverton, Ore. 97077; Louis Pengue, (503) 627-4082.

CIRCLE 309

Dave Bursky

Ledex solenoids simplify locking mechanisms



Here are three of hundreds of possible design approaches to locking mechanism design using reliable, durable, economical, and easy-to-apply Ledex rotary and linear solenoids. Request catalogs.

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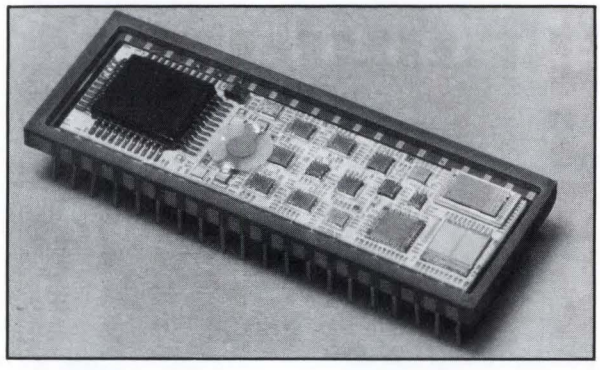
CIRCLE 189

Hybrid microcomputer works at 200°C



Very few off-the-shelf microcomputer subsystems operate beyond the 125°C upper limit of the military temperature range. Thus a hybrid 8-bit microcomputer specifically designed for applications that require an operating temperature range of −55° to +200°C is noteworthy.

The DHC8-P85, made by White Technology, consists of an 8-bit CMOS microprocessor, a crystal oscillator, I/O buffers, both hardware and software serial interfaces, 2048 bytes of static RAM, and 2048 bytes of CMOS fuse-link PROM, all housed in a 0.8-by-2-in. 40-pin DIP.

The entire circuit operates from a 5-V supply and draws just 11 mA typically and 35 mA in the worst case.

The system memory can be expanded up to 64 kbytes with separate RAM modules of 16 kbytes each (the DHC8-M16). Housed in a similar 40-pin package, these modules contain all the decoding logic.

So that a user can familiarize himself with the system, a small internal monitor program is included, to bring the system up when power is applied. When the user is ready, he can turn the monitor off via a control pin and write and debug the application software using any standard 2048-byte PROM. The company will copy the code into the system's PROM.

The CPU is the 80C85 microprocessor, which operates at clock frequencies of 1.8, 3.6, or 7.8 MHz. The housing is a ceramic package with the lid bonded via a high-temperature polymer.

The hybrid costs $2400 each for fewer than 10 units, and its add-on memory modules cost $1600 apiece in similar quantities. Delivery is from stock or in eight weeks.

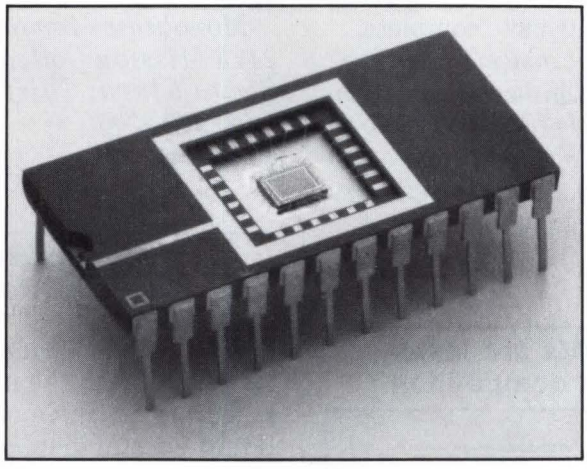
White Technology Inc., 4246 E. Wood St., Phoenix, Ariz. 85040; Peter Conner, (602) 437-1520.

CIRCLE 308

Dave Bursky

DIGITAL ICs

8-, 12-bit SARs in CMOS slash current drain



Two of the first successive-approximation registers made with CMOS drop the maximum power supply current by at least an order of magnitude, to just 3 mA at 1 MHz.

The Si2503 and Si2504 contain all the digital control and storage circuitry needed to implement 8- and 12-bit analog-to-digital converters, respectively. The circuits, developed by Siliconix, also can be used as ring counters and serial-to-parallel converters.

Both chips are guaranteed to operate with clock frequencies of up to 10 MHz (with a current drain of 20 mA maximum, 10 mA typical) but typically can run at 15 MHz. The maximum conversion speed for a converter built with the chips can be estimated by dividing the clock frequency by the word length plus one.

Unlike their bipolar counterparts, the CMOS units have outputs that can be put into a three-state mode, permitting multiple units to share a common bus. Also, they can be cascaded if more bits are needed or short-cycled if fewer bits are needed by the applications. To permit either one's or two's complement conversion, the complement of the most significant register bit is available.

The 8-bit device is housed in a 16-pin DIP, and the 12-bit unit in a 24-pin DIP, in either plastic or ceramic; bare chips can also be obtained. Samples are available from stock.

Both units operate over the commercial or the military temperature range, from supply voltages of 4.5 to 5.5 V. In 100-unit quantities, the 12-bit commercial version in plastic costs $5.

Siliconix Inc., 2201 Laurelwood Road, Santa Clara, Calif. 95054; (408) 988-8000.

CIRCLE 311

Dave Bursky

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CIRCLE 190

DIGITAL ICs

Macro arrays mix TTL and ECL I/O

Three bipolar macro arrays can be configured to simultaneously interface with external TTL and ECL logic. They are fabricated with an oxide-isolated two-level metal process that yields equivalent internal gate delays of 800 ps at 1 mW/gate.

Designated the V1200, V1700, and V3500, the macro arrays have maximum equivalent gates of 1338, 1712, and 3632, respectively. Each device is supported by an extensive library of physical macros that are functionally equivalent to the Motorola, Advanced Micro Devices, and Advanced Micro Circuits macro libraries. Designs are now being accepted for the V1200 and the V1700, while the V3500 will be available for design during the second quarter of 1985.

Vatic Systems Inc., 761 E. University, Mesa, Ariz. 85203; (602) 962-8998.

CIRCLE 344

16k EEPROM is 2816-compatible

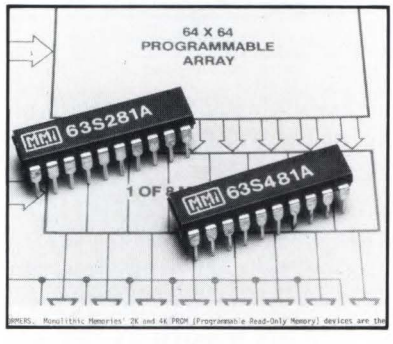
Available for off-the-shelf delivery, the XL2816A 16k EEPROM is fully compatible with the industry-standard 2816A from Xicor, as well as older-generation 21-V EEPROMs (such as Intel's 2816). The chip is designed for applications requiring 10 years of data retention with or without power applied and up to 10,000 write cycles/byte of memory.

The XL2816A, which is organized as 2048 by 8 bits, features 5-V read and write cycles. Read access times range from 250 to 450 ns. The self-timed write cycle requires less than 10 ms to complete.

Exel Microelectronics Inc., 2150 Commerce Drive, San Jose, Calif. 95131; (408) 942-0500. From $21.45 to $30 (100 units, commercial temperature range).

CIRCLE 345

PROMs are faster than competition



Two PROMs have been added to MMI's high-speed product line that boast the industry's fastest access times. The 63S281A is a 2k device with a maximum access time of 28 ns, at least 60% faster than current devices of its type. The second PROM, the 4k 63S481A, offers a maximum access time of 30 ns, nearly 20% faster than comparable 4k PROMs.

The 63S281A is organized as 256 words by 8 bits; the 63S481A, as 512 words by 8 bits. The latter device has nine inputs and eight outputs, enabling 512 product terms per output. The former has eight inputs and eight outputs, permitting 256 product terms per output.

In quantities of 100, the prices for the 2k and 4k parts are $4.84 and $6.51, respectively, in 20-pin plastic packages.

Monolithic Memories Inc., 2175 Mission College Blvd., Santa Clara, Calif. 95050; (408) 970-9700.

CIRCLE 346

CMOS decoders drive LCDs

Two CMOS decoder-driver ICs contain the necessary circuitry to drive standard liquid-crystal displays in applications such as digital meters and calculators. Designated the CD22104 and the CD22105, the devices contain an internal ROM, which decodes four data inputs into seven-segment outputs that are used to drive the LCD.

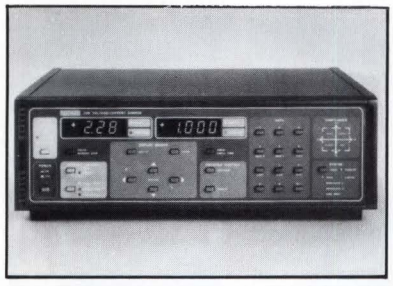
Each device is available for two modes of operation. The CD22104 decodes binary inputs into hexadecimal outputs, while the 22104A decodes binary inputs into decimal outputs. Similarly, the CD22105 is a binary-to-hexadecimal decoder and the 22105A, a binary-to-decimal unit. The devices differ only by the manner in which the digit-select inputs are used to activate each of the four LCDs in a display. All versions of the decoder-driver are supplied in 40-pin plastic DIPs.

RCA Corp., Solid State Division, Route 202, Somerville, N.J. 08876; (800) 526-2177 or (201) 685-6000. $5.95 (100 units); eight weeks.

CIRCLE 347

INSTRUMENTS

Current, voltage unit sinks or sources 100 W



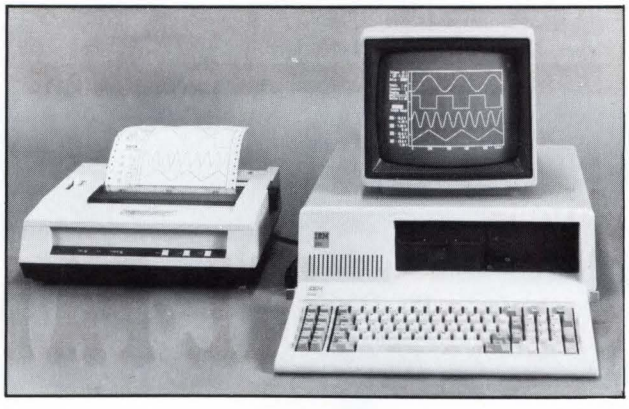
Featuring an IEEE-488 interface, the Model 228 programmable bipolar source can sink or source 100 W in either a constant-current or a constant-voltage mode. The instrument's nonvolatile memory is capable of storing operating parameters for up to 100 different test setups. To accommodate a broad range of test applications, memory sequencing can be controlled over the 488 bus or via the unit's front panel.

In sink operation, a full 100 W is available with a maximum voltage of 100 V or a maximum current of 10 A. Voltage and current are separately programmable in three ranges, each having a resolution of 1000 counts. The recovery time for load transients is less than 1 ms, and the output remains stable during and after recovery. The Model 228's output can be controlled by an external modulating signal with a frequency range of dc to 600 Hz. An integral monitor provides a 3½-digit readout of both voltage and current.

Keithley Instruments Inc., 28775 Aurora Road, Cleveland, Ohio 44139; (216) 248-0400. $3300.

CIRCLE 348

Package turns IBM PC into fast digital scope



A package consisting of a single card and software transforms the IBM PC or PC XT personal computer into a digital storage oscilloscope capable of sampling up to 16 analog inputs at a maximum rate of 1 MHz and then converting the resulting data into display waveforms. The ISC-16, from RC Electronics, resolves 12 bits and holds up to 64 kbytes of sample data.

The package can be programmed for sampling rates and triggering modes. Compatible with MS-DOS, the software stores data in standard record formats for later manipulation and controls the basic data acquisition and waveform displays.

Printing routines are provided for the most popular printers. The printed waveforms feature a resolution of 640 by 800 pixels per page, vs 460 by 200 pixels for the monochrome screen.

Ray Weiss

On the card, the 16 analog input channels are multiplexed into a register that feeds a 12-bit flash a-d converter whose output is clocked into one of two 32-kbyte RAM data banks. One bank can be used for sampling while the other is accessed for analysis. Also, the unit provides both external and internal trigger options for sampling and features both pre- and post-sample triggering.

Software packages are available for analyzing post-sample data, among them ones for spectrum analysis, signal averaging, auto- and cross-correlation, and histogram analysis. Also, a utility program is available to continually store sample data on a floppy or a hard disk.

The ISC-16 is priced at $2495 for a single package, with delivery in four weeks from receipt of an order.

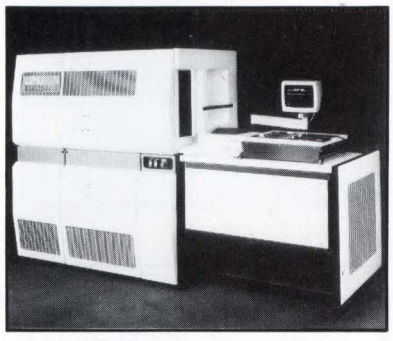
RC Electronics Inc., 5386 Hollister Ave., Santa Barbara, 93111; (805) 964-6708.

CIRCLE 307

INSTRUMENTS

Board tester ups pin count, drops cost

The L210 board tester from Teradyne represents a price/performance breakthrough for the production testing of printed circuit boards housing LSI and VLSI circuits. This latest member of the L200 family,



the *ne plus ultra* of board testers, uses new test electronics that enable the unit to be configured with up to 3024 10-MHz test pins—30% more than previous models—at a cost savings of 30% to 50%. At the same time, it requires only half the floor space of its predecessors.

Like the rest of the family, the unit employs a test strategy, known as "MultiMode," that combines in-circuit bus cycle emulation and board-level functional tests. The combination simplifies the testing of systems using commercial microprocessors and support chips. Moreover, the unit can be used for functional testing at speed from the edge connector, an important feature for boards that contain gate arrays or other semicustom logic.

The base price of the L210 is $235,000, but typical system configurations will range from $500,000 to $750,000. Deliveries will begin in the first quarter of 1985.

Teradyne Inc., 321 Harrison Ave., Boston, Mass. 02118; (617) 482-2700.

CIRCLE 305

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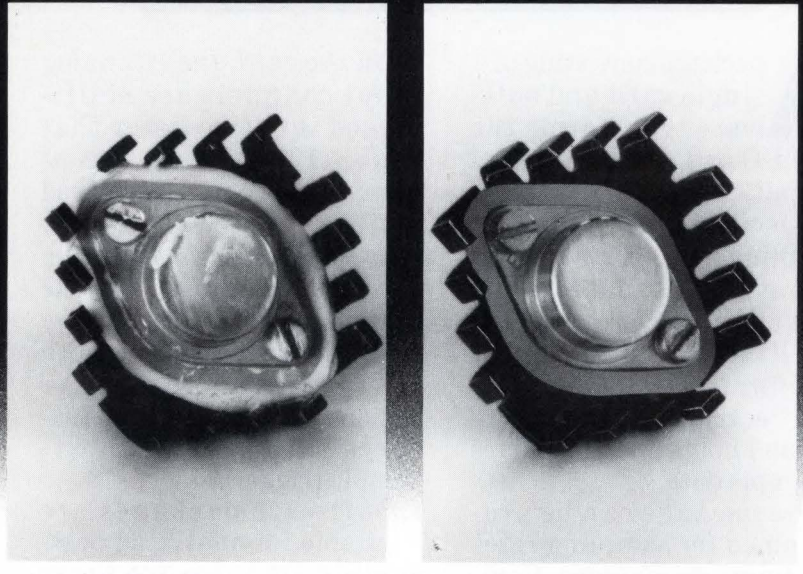

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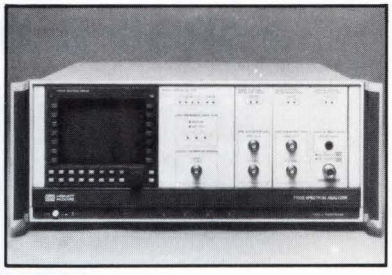
CIRCLE 191

INSTRUMENTS

Spectrum analyzers are modular

Pushing the concept of modularity to the hilt, a family of spectrum analyzers can be tailored to perform manual or automatic measurements over the frequency range of 100 Hz to 325 GHz. Consisting of a mainframe enclosure, two display units, and different analyzer modules, the HP 7000 modular measurement system from Hewlett-Packard uses a high-speed digital interface bus to achieve rapid communication between the system components. Moreover, the systems can communicate with other instruments or controllers via the IEEE-488 interface bus.



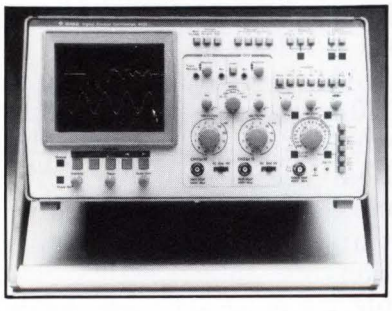
The systems are operated manually using 14 soft keys located on both sides of the display unit's CRT screen. These keys give an operator access to an extensive set of built-in measurement, signal-processing, and trace-manipulation functions.

Initially, three standard factory-configured systems are being offered: the HP 71100A rf system (100 Hz to 2.9 GHz), priced at $31,000; the HP 71200A microwave system (50 kHz to 22 GHz), for $35,000 or $36,600 (26.5-GHz option); and the HP 71300A millimeter system, priced at $33,000 excluding external mixers. Delivery is in eight weeks.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadaro Road, Palo Alto, Calif. 94303.

CIRCLE 302

Digital scope includes bus and plotter ports



A low-cost digital storage oscilloscope comes with an IEEE-488 interface, plus an automatic plotter interface for producing grids, scales, and plots of oscilloscope traces. The instrument also features automatic cursor measurements of time and voltage, displayed alphanumerically on the screen. An optional remote keypad enables mathematical manipulation, filtering, averaging, and individual TV line examination of stored traces. The 20-MHz Model 4035 performs dual-channel sampling at 20 megasamples/s.

Gould Inc., Design and Test Systems Division, 4600 Old Ironside Drive, Santa Clara, Calif. 95050; (408) 988-6800. $4450; 90 days.

CIRCLE 349

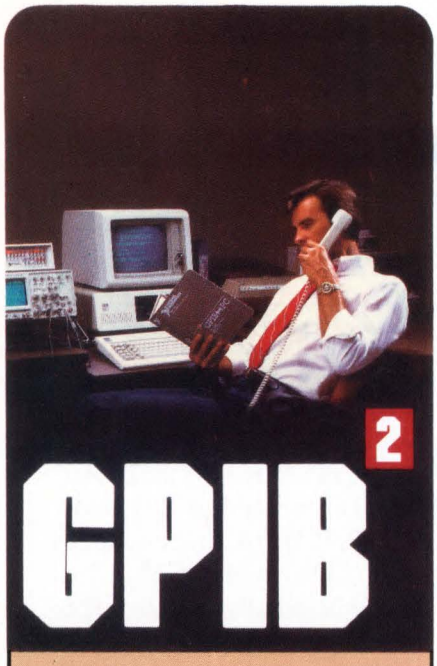
Multimeters survive harsh environments

To meet the rigors of harsh industrial use, a family of analog/digital multimeters is guaranteed to operate in calibration for one year despite shock, vibration, drops, contaminants, and moisture. The 20 Series' 3½-digit liquid-crystal display, which updates twice per second, works at temperature extremes of −15° to +55°C and to −40°C for 20 minutes. Typical continuous operation is from −20° to +60°C. The 3200-count display also provides up to a tenfold greater resolution than conventional 3½-digit, 2000-count multimeters.

The units offer 0.1% dc accuracy and ranges of 100 μV to 1000 V ac and dc, 0.1 μA to 10 A ac and dc, and 0.1 Ω to 32 MΩ resistance. High-speed autoranging automatically selects the correct measurement range. The two models that comprise the series, the Models 25 and 27, are identical except that the latter offers min/max and relative operating modes.

John Fluke Manufacturing Co. Inc., PO Box C9090, Everett, Wash. 98206; (206) 342-6300. $229 and $259 (Models 25 and 27, respectively); November.

CIRCLE 350



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CIRCLE 192

POWER

25-W switching supplies leak a mere 5 μA

Providing input-to-output isolation of 3750 V ac, the PSPM series of 25-W single-output switching power supplies from Total Power International hold leakage current to an ultralow 5 μA.

That isolation, a 9-mm creep distance between the input and output sections (which helps produce the isolation rating), and that leakage current mean that the supplies meet both the VDE class II requirements and the UL 478 standard for medical equipment.

Available for 5-, 12-, or 24-V operation, the PSPM series of modules operates at a switching frequency of 40 kHz, which allows its members to achieve a minimum efficiency of 80% and minimize audible noise. Their 2.2-by-3.5-by-1.25-in. package includes an internal LC EMI filter and a six-sided shield.

All units operate from 110 or 220 V ac, 47 to 440 Hz, as well as from 156 or 311 V dc. Load regulation is ±0.2% maximum, and line regulation is the same for variations of −15% to +10%; ripple and noise are each 75 mV pk-pk. The output voltage varies ±0.01%/°C maximum.

The PSPM 110-5S500 provides 5 V at 5 A, the PSPM 110-12S2100 is designed for 12 V at 2 A, and the PSPM 110-24S1050 is rated for 24 V at 1 A. All the units cost $156 each in lots of one to nine and are available from stock.

Total Power International, Inc., 418 Bridge St., Lowell, Mass. 01850; Carl Fryatt, (617) 453-7272.

Gary Elinoff

POWER

300-W servo amplifier is complete in 15 in.^{3}

A 300-W pulse-width-modulated servo amplifier in a very compact package, the Model 210 from Copley Controls contains all the circuitry needed to operate in a rate loop or as an inner loop in a position control system. It delivers 4 A continuously or 10 A for 1 second at 75 V, operating at a switching frequency of 22 kHz and therefore eliminating essentially all audible noise.

Only 5 by 4 by 0.75 in., the amplifier contains a 15-V dc-dc converter for the sensing and control circuitry, so that it can operate from a single dc power source of 20 to 80 V. It also includes a unity-gain differential amplifier and a current-sensing resistor.

The servo preamplifier's gain is determined by external resistors, and the power stage sports a small-signal bandwidth (−3 dB) of 1 kHz.

The unit provides full output over 0° to 40°C or up to 70°C when mounted on a machined baseplate. It is available with an internal heat sink (the Model 210H), thereby allowing for operation at up to 55°C ambient or 60°C with forced air of 400 cfm. Heat-sink temperature sensing and current limiting protect the amplifier from excessive temperature.

The Model 210 is priced at $310 each in quantities of one to nine pieces; the Model 210H costs $330 for similar lots. Delivery is in four to six weeks after the receipt of an order.

Copley Controls Corp., 375 Eliot St., Newton, Mass. 02164; Charles Sarkisian, (617) 965-2410.

CIRCLE 303

Gary Elinoff

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CIRCLE 193

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POWER

FETlington ousts bipolar Darlingtons

Replacing bipolar Darlington configurations with a single compact device is the FETlington—a MOSFET that successfully combines logic compatibility and low cost. The price of the FETlington ranges from $0.10 to $0.20 (in quantities of one million and ten thousand, respectively). Unlike its bipolar predecessors, the device does not require extra components when used in the same applications. In addition to cost savings, its small die size of 0.036 in. square saves pc board space.

The first member of the FETlington family, the 2N7000 delivers up to a 60-V, 100-mA signal with a total drop (V_{ds}) of 0.5 V. Currents of up to 200 mA are possible with a 10-V gate drive. The 2N7000 also offers turn-on and turn-off times of less than 10 ns and 40-V DURAMOS gate protection.

Siliconix Inc., 2201 Laurelwood Road, Santa Clara, Calif. 95054; (408) 988-8000. Stock.

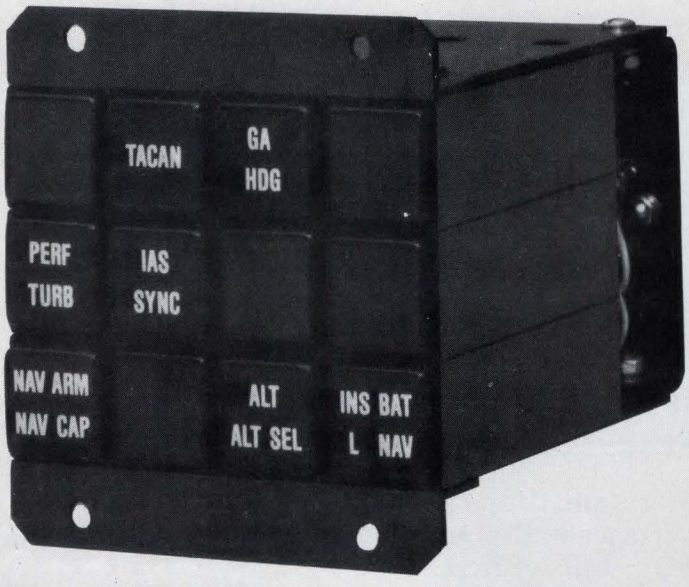
CIRCLE 351

200-W UPS protects personal computers

The Model 300PC+ uninterruptible power supply provides regulated power for a fully configured IBM PC XT, including a monochrome or color monitor. During total power outages, it delivers up to 200 W (or 300 VA) for 5 to 45 minutes, depending on the amount of power being consumed by the computer. The 300 PC + has a typical transfer time of 4 ms, 8 ms maximum. Its maintenance-free 12-V battery can be recharged in 8 to 12 hours. The unit has four ac power receptacles.

American Power Conversion Corp., 89 Cambridge St., Burlington, Mass. 01803; (617) 273-1570. $595.

CIRCLE 352



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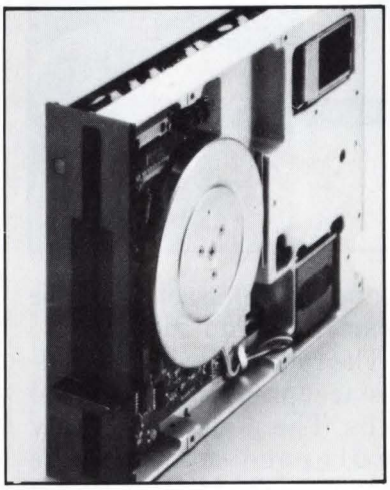
CIRCLE 194

COMPUTER PERIPHERALS

5¼-in. half-height floppy packs in 6.5 Mybtes

A 5¼-in. half-height floppy-disk drive has an unprecedented capacity of 6.5 Mbytes unformatted, four times more than the 1.6 Mbytes of conventional 5¼-in. floppies. In addition, the FDD541 drive, from Hitachi, transfers data at 3 Mbits/s, six times faster than conventional drives.

The formatted capacity is 4.15 Mbytes, stored on 208 tracks (at 125 tpi) at 29,560 bpi. The drive uses narrow-gap manganese-zinc read/write heads, which produce a stronger magnetic field than nickel-zinc ferrite heads and



therefore more precise, higher-resolution recording.

The minifloppy is 41.3 by 119 by 146 mm and weighs approximately 1.5 kg. It requires +5 and +12 V and uses a modified ST506 interface, making for easy installation with systems having 5¼-in. hard-disk drives. Priced at $540 for an evaluation sample, it will be available in the U.S. in March.

Hitachi America Ltd., 950 Elm Ave., Suite 100, San Bruno, Calif. 94066; (415) 872-1902.

Hitachi Ltd., Computer Department, 6 Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo 101, Japan (03) 258-1111.

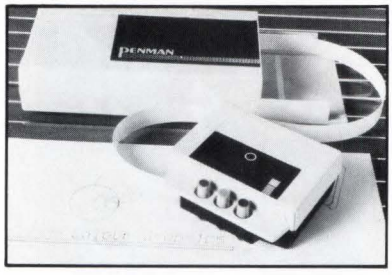
CIRCLE 306

COMPUTER PERIPHERALS

Plotter prints and acts as mouse as well

A three-color plotter costing only about $260 also functions as a high-resolution printer and mouse. The Penman plotter from Penman Products in England connects to almost any computer through an RS-232 interface and consists of a control box linked (when in use) by ribbon cable to a 5-in.-square "robot," a turtle-like device that moves across the paper at 50 mm/s.

The robot draws straight lines and circles without any "staircase" effect, resolving 10 dots/mm. It includes a full ASCII character set plus a



pound sign; characters can be as small as 1 mm high.

The robot's three pen holders accept standard Pentel pens. The pens can simply be dropped in and can be changed in mid-line. Paper size is limited only by the 1-m-long cable.

When the robot is placed on the paper, optical sensors guide it to the bottom-left corner, which it uses as a reference point. It will detect if it has wrapped the cable around itself and, if so, will rotate to unwind it. Slotted together for storage, the two parts are only 34 by 13 by 5.5 cm.

American Micro Products Inc., 705 North Bowser, Richardson, Texas 75081; (214) 238-1815.

Penman Products Ltd., 8 Hazelwood Close, Dominion Way, Worthing, West Sussex BN14 8NP, England: (0903) 209081; Telex: 946240.

CIRCLE 301

Streamer threads tape automatically

Designated the Model 9600, a ½-in. reel-to-reel tape transport automatically threads any size reel—from small demonstration tapes to full 2400-ft 10½-in. reels. The unit operates in either a true start-stop mode at 45 ips or in a streaming mode at 100 ips. In both streaming and start-stop modes, the transport achieves a data density of 800 or 1600 char/in. using NRZI or phase-encoding techniques, respectively.

At 45 ips, the 9600's start-stop time is 8.3 ms. The transport rewinds at 200 ips. In the streaming mode, microprocessor control and tension arms give less than a ±5% speed variation and 8 oz of tension to provide operating specifications that are 50% better than other streamers. The read and write access time of the 9600 is 100 ms, while reposition time from a full stop is 400 ns.

Kennedy Co., 1600 Shamrock Ave., Monrovia, Calif. 91016; (818) 357-8831. $3400 (500 units).

CIRCLE 353

Two-board set forms digital filter

Housed in a compact Euro enclosure, a 16-bit digital FIR filter card and a 12-bit analog I/O card combine to perform real-time digital signal processing. Up to 256 filter taps can be downloaded from a terminal or a personal computer via an RS-232-C interface. The unit, designated the FDU-16E, has a sampling frequency range of up to 200 kHz, with the sampling clock generated either internally or externally.

Simple filter design routines allow the user to specify the filter type—low-pass, high-pass, bandpass, or band-reject—and the pass-band edges. Filters can have more than 50 dB/octave of rolloff and 60 dB of stop-band attenuation. The FDU-16E also provides four output range selections in 6-dB steps.

Interactive Circuits and Systems Ltd., 3101 Hawthorne Road, Ottawa, Ont., Canada K1G 3V8; (613) 521-0590. $3295.

CIRCLE 354

COMPUTER PERIPHERALS

3½-in. Winchester accesses in 70 ms

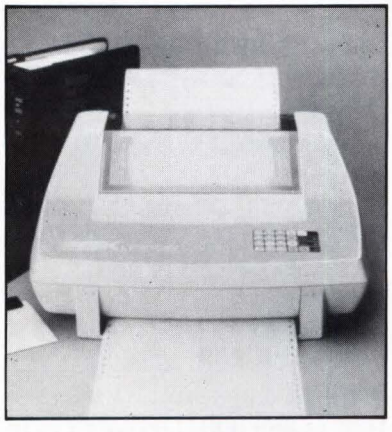
Rated at 70 ms, a 3½-in. half-height Winchester disk drive produces one of the industry's fastest average access times among sub-5¼-in. hard disk drives. Designated the HH-312, it offers a formatted storage capacity of 10 Mbytes and data transfer rates of 5 Mbytes/s.

The compact 2¼-lb Winchester drive serves microcomputer applications where space, weight, and power are prime considerations. It operates on 9 W, which simplifies interfacing requirements and makes it suitable for portable applications.

Microscience International Corp., 575 E. Middlefield Road, Mountain View, Calif. 94043; (415) 961-2212.

CIRCLE 355

Multimode printer produces 300 char/s



The SX dot-matrix printer offers multiple modes of operation to provide draft, near-letter-quality, and letter-quality printing at speeds of up to 300 char/s. Letter-quality print is achieved through the use of a 23-by-18-dot matrix head, which produces clean, crisp characters.

About 50% faster than many popular dot-matrix printers, the SX works at 300 char/s in the draft mode, 71 char/s in the near-letter-quality mode, and 52 char/s in the letter-quality mode. Repeat and sidewinder functions allow a document to be printed out in its entirety up to 99 times and wide-column spreadsheet programs to be printed lengthwise on the paper. The latter requires an optional 64-kbyte buffer in addition to the printer's standard 4-kbyte buffer.

Micro Peripherals Inc., 4426 S. Century Drive, Salt Lake City, Utah 84123; (801) 263-3081. $795; 60 days.

CIRCLE 356

Winchester drives transfer 6.25 kbytes/s

Aimed at the integrator and systems development markets, a family of 5¼-in. Winchester disk drives has a data transfer rate of 6.25 kbytes/s and an average access time of 85 ms, including settling time. The product line includes the RD-4000 series, which comprises four models offering unformatted storage capacities of 6.4, 12.7, 19.1, and 25.5 Mbytes. Additionally, two half-height units are available—part of the RD-2000 series—for 6.37 and 12.7 Mbytes of unformatted data storage. All of the drives use a standard ST506 interface. Units can be vertically or horizontally installed, and up to four drives can be daisy-chained to a single system.

Sumicon Inc., 17862 E. 17th St., Tustin, Calif. 92680; (714) 730-6061.

CIRCLE 357

3½-in. Winchester features rugged design

Intended for use with personal and portable computers, a 3½-in. Winchester disk drive is designed to tolerate a wide variety of adverse environmental conditions. The micro-Winchester, designated the HP 97501A, is able to withstand shocks of up to 50 G without requiring elaborate mounting techniques. It also withstands 95% relative humidity and rapid changes in temperature.

The HP 97501A is currently available with 10 Mbytes of formatted storage, but the mechanism is designed to incorporate larger capacities in future versions. Interface options include IEEE-488 and SCSI.

Hewlett-Packard Co., Inquiries Manager, 1020 NE Circle Blvd., Corvallis, Ore. 97330; call local sales office. Less than $400 (10,000 units).

CIRCLE 358

Series 97-500*
The original, ¾"
wide Sticky Fingers
with superior shielding
effectiveness.

Series 97-538*
For maximum
effectiveness at
10GHz plane wave; a
bit less than 1" wide.

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Telephone: (717) 424-8510

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*patented

CIRCLE 196

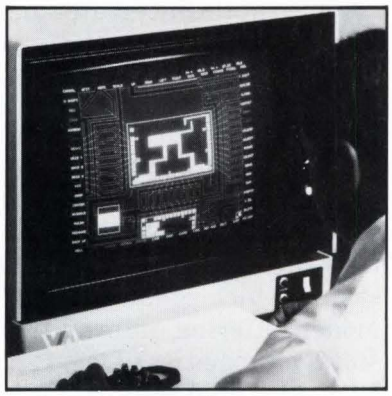
NEW PRODUCTS

COMPUTER SYSTEMS

CAE workstation takes on hybrid ICs

The SystemNode 120H from Via Systems is the first CAE workstation specifically built for the design and manufacture of hybrid circuits. It eliminates the distortions and inaccuracies long associated with the use of Mylar film techniques for hybrid layout and mask generation.

The system is based on a PDP-11/23 and a variety of software packages, dubbed "ToolKits." Among the standard packages are ones for layout, precision resistors, and substrate design-rule checking. The workstation accepts or issues data in design or production formats. Formats from other systems or mask houses are acceptable.



Fully capable of operating as a stand-alone unit, the unit can be linked to other design systems by means of an Ethernet option.

The hardware includes 256 kbytes of main memory, a 35-Mbyte Winchester disk drive with controller board, a ½-in. tape drive, and a color graphics display. A 70-Mbyte disk drive is optional, as is a pen plotter. The base price of the stand-alone system is $89,900. Delivery is in 30 days.

Via Systems Inc., 76 Treble Cove Road, North Billerica, Mass. 01862; Bob Consentino, (617) 667-8574.

CIRCLE 318

COMPUTER SYSTEMS

Unix-based workstation comes in at $9900

Taking advantage of an Ethernet local-area network, a workstation based on the Unix 4.2 BSD operating system and a 68010 CPU is specifically designed to operate as a diskless node. Dubbed the Sun-2/50 Desktop SunStation, the one-board unit is available at the exceptionally low price of $9900. A typical configuration will have several of these units sharing the hard-disk memory space of a single file server, with demand paging handled at high speed over the Ethernet network.

The unit comes with 1 Mbyte of main memory standard, expandable up to 4 Mbytes; a 19-in. tilt-and-swivel monochrome display refreshed at 66 Hz noninterlaced; and a 128-kbyte frame buffer. It handles bit-mapped graphics with a resolution of 1152 by 900 pixels.

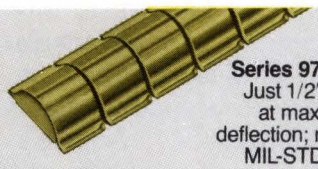
In addition to accessing Ethernet through a VLSI controller chip, the workstation provides two RS-423 serial ports. A memory management unit allows the 10-MHz 68010 processor to access any location in main memory with no wait states, and users can specify an IEEE-standard floating-point option.

The software includes the SunCore graphics program and the SunWindows window manager. Also standard are C, Fortran, and Pascal compilers. The unit is completely software-compatible with all other members of the Sun-2 workstation family.

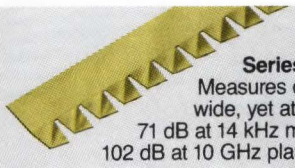
Discounts are given for volume purchases, and delivery takes 60 to 90 days after receipt of an order.

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, Calif. 94043; Jackie Rae, (415) 960-1300.

CIRCLE 304



Series 97-520*
Just 1/2" wide at maximum deflection; meets MIL-STD-285.



Series 97-555
Measures only 3/8" wide, yet attenuates 71 dB at 14 kHz magnetic, 102 dB at 10 GHz plane wave.

Series 97-540*
Newest in the line, this series is only 0.37" wide at maximum deflection.

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Series 97-541*
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*patented

CIRCLE 196

COMPUTER SYSTEMS

System meets large CAE/CAD/CAM demands

The 32-bit CDS 5000 is a large-scale system designed to meet the challenge of storing and managing graphic information and engineering data common in large CAE/CAD/CAM installations. The system can simultaneously support up to 64 interactive users and data bases of more than 40 Gbytes.

Driving the CDS 5000 is the CDS-R, a powerful system resource comprising an IBM 4300 processor, a bus-control unit, and the IBM VM/CMS operating system. Coupled with IBM's SQL/DS relational data-base manager, the Product Data Manager, a proprietary application program, manipulates, controls access to, and safeguards the integrity of large data bases.

Computervision Corp., 100 Crosby Drive, Bedford, Mass. 01730; (617) 275-1800. From $485,000 to $650,000.

CIRCLE 359

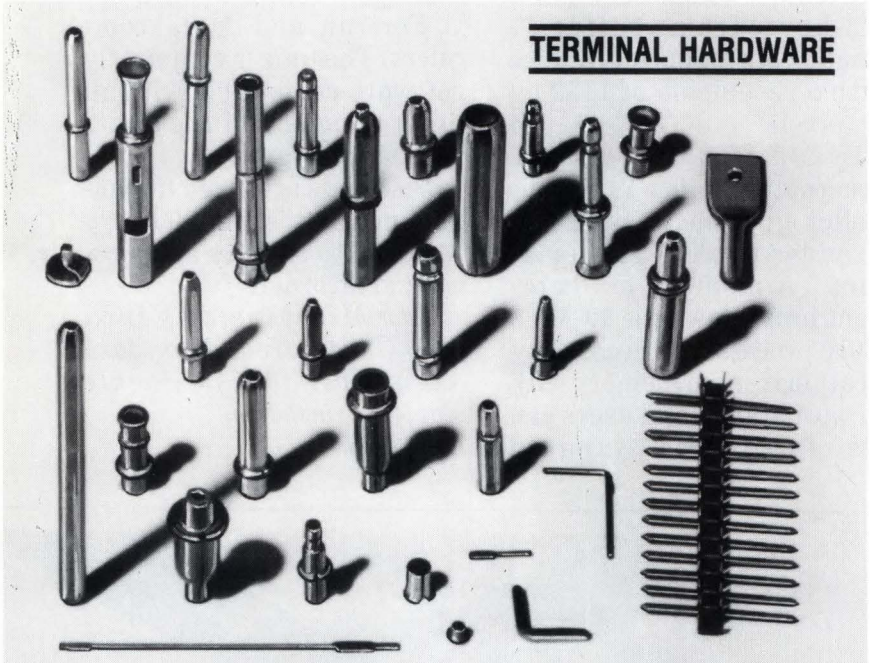
Multi-user micro runs existing mini software

The MAI 2000 management system, a multi-user microcomputer, runs an entire line of business application software developed in Business Basic for MAI/Basic's existing line of minicomputers. The system features Boss/IX, a powerful Unix-like operating system, and the ability to be linked with more than 60 other MAI 2000s in a local area network.

The main processing unit of the 68010-based microcomputer fits easily on a desktop or in a vertical position alongside it. Each system, which is configured with a minimum of 768 kbytes of memory, holds up to six 256-kbyte memory boards and up to five controller cards.

MAI/Basic Four Information Systems, 14101 Myford Road, Tustin, Calif. 92680; (714) 731-5100. From $14,250.

CIRCLE 360



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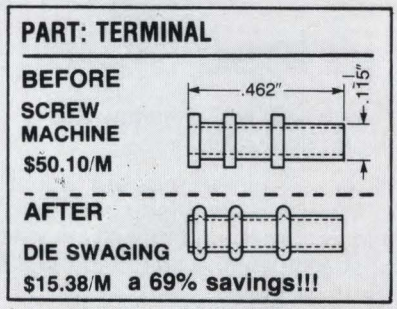

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CIRCLE 197

COMPUTER SYSTEMS

VMEbus computer handles 6 32-bit CPUs

The latest member in a family of 32-bit multiprocessor computers, the Expert 32 supports up to six processor cards. Based on the NS32032 CPU, each processor card includes a floating-point processor, a memory management unit, and 32 kbytes of cache memory.

The system features a 16-slot double-width VMEbus backplane and up to 16 Mbytes of main memory. It also comes with 10 Mbytes of removable storage and 10 Mbytes of fixed storage. The Expert's four RS-232-C serial channels are expandable to twenty.

Although the ECS PVS virtual-storage operating system is supplied with the computer, users may also opt for Unix, which will be available by the end of the first quarter of 1985.

Elite Computer Systems, 4129 May St., Wichita, Kans. 67209; (316) 942-6619. $17,700.

CIRCLE 361

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CIRCLE 198

FACTORY AUTOMATION

Floppy-disk drive mimics paper-tape reader

A plug-in floppy-disk control module emulates a paper-tape reader, bringing the advantages of magnetic program to numerical control application. Originally designed for the company's wire-wrapping systems, the FDR-1000 floppy-disk module, from OK Industries, can be retrofitted to most existing paper-tape-driven systems without modification.

Each IBM 3740-formatted 8-in. disk stores up to 256 kbytes of data—or approximately 5000 wiring sequences. Using floppy

disks, data from over 150 reels of tape can be stored in approximately the same space that a single reel of tape occupies. What's more, the disk drive has a selectable baud rate of up to 9600 bauds, 16 times faster than paper tape, and the disks of course can be rewritten and will not tear.

Wiring-program disks can be created on a host computer, or the program can be downloaded directly to the FDR-1000 via an RS-232-C interface and stored on disk.

The FDR-1000 costs $3250 for the rack-mounted version and $3500 in a stand-alone configuration (the FDR-1000). It is also available as part of the SW-1000 semiautomatic wire-wrapping system, which is priced starting at $8595.

OK Industries Inc., 3455 Conner St., Bronx, N.Y. 10475, Bob Cirr, (212) 994-6600.

CIRCLE 310

Cluster controller links robotic work cells

A cluster controller provides hierarchical control for up to 64 robots in a variety of flexible manufacturing work cells. Called Merlin, the controller serves as an interface between the robots and the host computer. Depending on the information received from the host, the controller can download programs to the appropriate robots, upload robot production information to the host, and perform monitoring functions through its extensive analog, digital, and serial communications channels.

The 68000-based Merlin controller incorporates a standard VERSAbus interface and comes with 640 kbytes of main memory, a 400-kbyte floppy-disk drive, a 65-Mbyte Winchester disk drive, and a removable streaming tape cartridge. Merlin runs under Magix, a Unix-based multi-user operating system.

American Robot Corp., 121 Industry Drive, Pittsburgh, Pa. 15275; (412) 787-3000. $50,000.

CIRCLE 362

Kelvin probes boost accuracy and speed

Designed for probing anything from a monolithic IC to a thick-film hybrid circuit, a family of Kelvin probes eliminates errors caused by variable probe-card trace resistance, as well as contact resistance. Multiple four-point Kelvin measurements are possible with the single-body dual-conductor probes through the use of fixed-pattern probe cards. This makes it possible to trim a complex hybrid circuit completely and accurately on one pass through a laser trimmer, thereby boosting both throughput and accuracy.

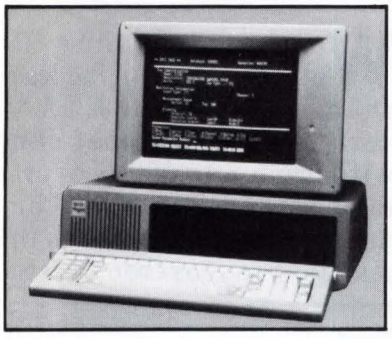
The probes are mounted on a Z-adjustable ceramic blade for planarization accuracy and electrical isolation. The Z adjustment is ±25 mils and planarization between the probe tips is better than 1 mil. The contact center spacing of the tip may be selected from 2 to 60 mils.

Accuprobe, 1 Harrison Ave., PO Box 1044, Salem, Mass. 01970; (617) 745-7878. $16.50 and $18.80 for short- and long-bodied assemblies, respectively.

CIRCLE 363

FACTORY AUTOMATION

Modified IBM 5531 extends industrial uses



A modified version of the IBM 5531 industrial computer, the Macsym 120 workstation adds an 8087 math coprocessor, Concurrent CP/M-86, and multitasking MacBasic to optimize operation. Additionally, Macsym I/O cards support more analog channels (as many as 30 on a single card) than any other IBM-compatible plug-in cards. For distributed applications, Macsym front ends provide analog and digital interfacing.

Analog Devices Inc., 3 Technology Way, Norwood, Mass. 02062; (617) 329-4700. $9495; four weeks.

CIRCLE 364

Batcher controls single ingredient

Offering users high-performance batching without having to invest in a complex, software-intensive system, the 1200 single-ingredient batch controller sports many of the features found on large custom batchers, yet is easier to install and operate. Up to nine different batch sizes can be stored in the controller's nonvolatile memory. Three programmable relay contacts provide control of main feed, slow feed, and tolerance alarms.

The 1200 leads the operator through all setup and calibration procedures with simple menu prompts. An optional feature allows the 1200 to continually monitor the sensors and associated wiring. If a fault is detected, the controller indicates the location. A 4-to-20-mA current loop transmitter and an RS-232-C serial interface may also be specified.

Kistler-Morse, 10201 Willows Road NE, PO Box 3009, Redmond, Wash. 98073; (800) 426-9010 or (206) 881-8000.

CIRCLE 365

Motion controller fits servo amplifier chassis

Designed to fit into a standard servo amplifier chassis, the Mini MC^2 motion control interface card can be used in nearly any closed-loop, servo-controlled application. The board may be daisy-chained to drive up to eight axes under the supervision of a host computer. ASCII commands are sent to the MC^2 via a serial RS-232-C, parallel, or IEEE-488 interface.

Delta Tau Data Systems Inc., 21115 Osborne St., Canoga Park, Calif. 91304; (213) 998-2095. Less than $700.

CIRCLE 366

Think FAST.

If you're looking for high speed and low power in drivers, receivers, multiplexers, ALUs, latches and registers, think FAST.™ Fairchild Advanced Schottky TTL. Come to think of it, call your nearest sales office and ask for the *new 1985 FAST Data Book.*

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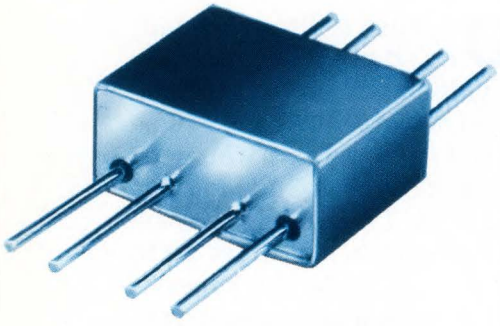
CIRCLE 199

tough flatpack
power
splitters



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- hi isolation, 25 dB
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*Units are not QPL listed

LPS-109 SPECIFICATIONS

FREQUENCY RANGE, (MHz)	10-500
INSERTION LOSS, dB (above 3 dB)	
10-250 MHz	0.6
250-500 MHz	0.8
ISOLATION, dB	25 dB
AMPLITUDE UNBAL.	0.3 dB
PHASE UNBAL.	2°
IMPEDANCE	50 ohms

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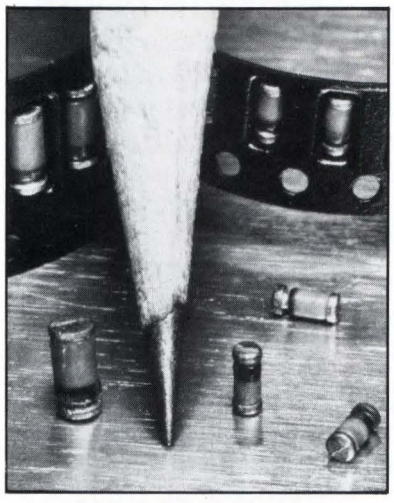
C96-3 REV. ORIG.

CIRCLE 200

COMPONENTS

Zener diodes can be surface-mounted



A full range of 1/2- and 1-W zener diodes are available in MLL34 and MLL41 leadless glass packages, respectively. The 49 devices that comprise the 1/2-W MLL5221 series cover a zener-voltage range of 2.4 to 91 V. Covering a range of 3.3 to 100 V are the 36 devices that make up the 1-W MLL4728 family.

The cases are hermetically sealed and contain the same nitride-passivated die as their leaded counterparts (the 1N5221 and 1N4728 series). Both series are available bulk packed or in tape-and-reel packages. T1 and T2 configurations are also available (cathode- and anode-facing sprocket holes, respectively).

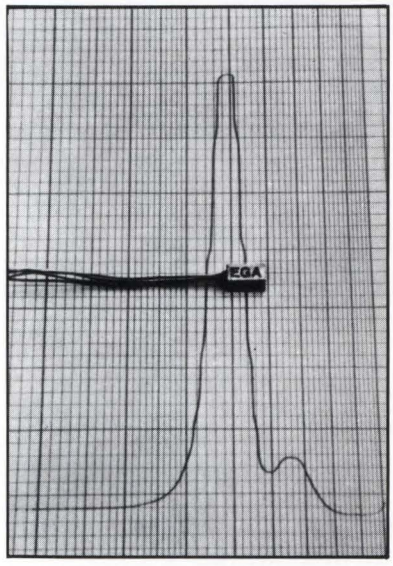
In quantities of 100, the price for the 1/2-W series ranges from $0.11 to $0.20; for the 1-W series, from $0.17 to $0.36. Tape-and-reel packaging adds $0.01 per device.

Motorola Semiconductor Products Inc., PO Box 20912, Phoenix, Ariz. 85036; (602) 244-4561.

CIRCLE 367

Tiny accelerometer withstands 10,000 G

Weighing less than 1/2 gram and occupying less than 0.006 in.^{3}, the EGAX series accelerometer can withstand a 10,000-G overload without damage. The monitoring device works in standard ranges from ±5 to



±2500 G. Its fully active semiconductor Wheatstone bridge gives a full-scale output of up to 250 mV.

Viscous damping and internal mechanical stops provide the 10,000-G overrange specification in the sensitive axis at all frequencies for the standard ranges. The accelerometer is also available with the same overrange protection in all three axes. Applications for the device range from ballistic missile control to automotive crash tests.

Entran Devices Inc., 10 Washington Ave., Fairfield, N.J. 07006; (201) 227-1002. From $495; stock to eight weeks.

CIRCLE 368

PRODUCT NEWS

LAN products link PCs and S-100 bus

Making its entry into the local area network market, **Intercontinental Micro Systems Corp. (Anaheim, Calif.)** has unveiled a line of products based on the ARCnet protocol. Hardware entries include a LAN controller card for the S-100 bus, a processor board that converts dumb terminals into 8-bit intelligent workstations with LAN communications capabilities, and a controller card that enables IBM PC and PC-compatible computers to be integrated into the network. Linking the various components together is the TurboDOS-based MicroNet software.

CIRCLE 369

Multipliers work faster, consume less

Optimized versions of two CMOS 8-by-8-bit multipliers, manufactured by **Logic Devices Inc. (Sunnyvale, Calif.)**, are not only faster, but consume less power than earlier models as well. The LMU080-1 parallel multiplier and the LMU8U-1 unsigned parallel multiplier operate with typical multiplication times of 40 ns at power dissipation levels of 75 mW—a 25-ns improvement over their predecessors, which consume 15 mW more power. The 16 outputs on each circuit can drive 100-pF loads with typical rise times of 4 ns. Housed in plastic packages, the multipliers are priced at $28.50 each in quantities of 1000; ceramic-packaged devices are priced at $45 each in like quantities.

CIRCLE 370

Power transistors' TO-220 case improved

A variety of power transistors in improved TO-220 packages is available from the **Electronic Components Division of Panasonic Industrial Co. (Secaucus, N.J.)**. By using a thin insulating coating on the transistor mounting fins, the company has eliminated the mounting and insulating hardware that is normally required for the TO-220 package. The insulating resin has a high thermal conductivity, improving free-air heat dissipation by approximately 17%. The dielectric strength of the resin is 1000 V. When used in conjunction with a heat sink, the new package reduces costs by eliminating the need for a metal spacer, a mica insulator, an insulating bushing, and a solder lug. It also reduces installed costs by simplifying assembly.

CIRCLE 371

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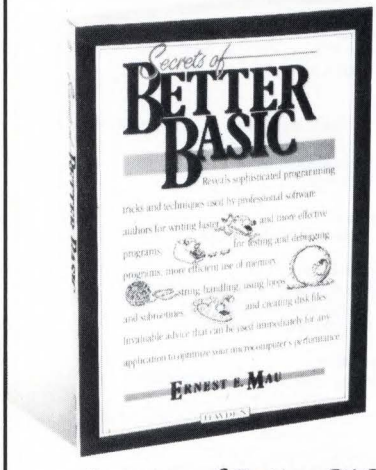

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PRODUCT NEWS

EPROM family is faster, costs less

The availability of a 256-kbit EPROM with a faster read access time of 200 ns was announced by **Intel Corp. Santa Clara, Calif.)**—introduced at $78 in quantities of 10,000. Additionally, the company announced that it is reducing the price of all its 256k EPROMs. The 450-ns version is $48 in quantities of 10,000, down from $76. The reduced price is part of a continuing program to make the 27256 family of memory devices available for $25 (in like quantities) by the end of the year. All versions of the 27256 EPROM offer 32 kbytes of storage and are compatible with such high-speed microprocessors and microcontrollers as the iAPX 186 and the 8031.

CIRCLE 372

Packages expand PROM programmer's range

Prepackaged hardware and software systems from **Wavetek-Digelec (Sunnyvale, Calif.)** enhance the company's Model 803 universal PROM and logic programmer. Called Digipacks, the six systems include two for PROM programming, two for logic programming, and two for both PROM and logic programming. The latter packages come with CUPL, the company's high-level programming language, at no extra charge. All of the Digipacks offer a choice of device adapters, specified by the customer from a guide that identifies over 800 devices that can be programmed with the Model 803. Additionally, each Digipack that performs PROM programming includes the DA-88 adapter, which programs more than 114 different device types. Prices for the Digipack systems range from $4995 to $6950.

CIRCLE 373

Enhanced spooler works with Run program

The print spooler portion of the OR-88C disk cache board, from **Origin Inc. (Los Angeles, Calif.)**, is now able to operate concurrently with the Intel Run program on Intel's Series III development system. What's more, the new spooler also works with CP/M. The 196-kbyte spooler requires no additional cables or hardware and uses the development system's parallel or serial port at a baud rate of up to 9600 bauds. The 480-kbyte cache RAM portion of the OR-88C speeds disk access by as much as threefold. Existing OR-88C disk cache boards can be retrofitted with the spooler enhancement at no extra charge.

CIRCLE 374

PRODUCT NEWS

Six-axis robot is more affordable

Making robotic automation more attractive to the electronics, automotive, and packaging industries, **Unimation Inc. (Danbury, Conn.)** has announced an approximate 30% price reduction for its computer-controlled six-axis robot, the Unimate Puma Series 260. In the VAL I configuration, the price has been reduced from $42,775 to $30,000, which includes the robot, a controller, a CRT, and a teaching pendant. The VAL II software option has also been significantly reduced—from $5000 to $3500. The robot has 2.2-lb payload capacity and a repeatability to within ±0.002 in.

CIRCLE 375

Options enhance Compaq Deskpro line

For its recently introduced Deskpro family of personal computers, **Compaq Computer Corp. (Houston, Texas)** is offering options that increase the machines' mass-storage capacities and operating speeds. A 30-Mbyte fixed-disk drive is available for each of the four models comprising the Deskpro line at a suggested retail price of $2995. For math-intensive engineering, scientific, and business applications, a high-speed 8087-2 coprocessor can be purchased for $375.

CIRCLE 376

12-bit d-a converter gets second source

The AD563, a laser-trimmed 12-bit d-a converter, is now being alternately sourced by **Motorola Semiconductor Products Inc. (Phoenix, Ariz.)**. The converter typically settles to within ±½ LSB in 200 ns and provides programmable output ranges of 0 to 5 V, 0 to 10 V, ±2.5 V, ±5 V, and ±10 V. Prices for the AD563 range from $22.95 to $71; delivery is from stock to six weeks.

CIRCLE 377

Logic tester works with 64-bit buses

Asynchronous logic tester (SLT) module, developed by **Marconi Instruments' ATE Division (Sunnyvale, Calif.)** for its System 80 in-circuit tester, speeds the testing of wide bus structures (up to 64 bits) by addressing all bus pins in parallel and adding a static functional test without decreasing productivity.

CIRCLE 378

ElectronicDesign

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- To aid progress in the electronics industry by promoting good design.
- To give the electronic design engineer concepts and ideas that make his job easier and more productive.
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NEW LITERATURE

Smartpower technology

Discussed in a four-color, 60-page compendium is the new Smartpower technology and its predicted impact on the electronics and electrical industries. The informative guide includes reprints of relevant articles selected from established technical publications and a glossary of terms. Smartpower ICs are the first to combine control logic and power devices on the same chip.

Siliconix Inc., 2201 Laurelwood Road, Santa Clara, Calif. 95054; (408) 988-8000.

CIRCLE 379

CMOS STD bus cards and cages

The MSI-C800 series of industrial-grade CMOS STD bus cards is featured in a four-page bulletin. Photographs and descriptions of each board are given, along with an overview of the entire series. Also included is the MSI-CR series of card cages.

Microcomputer Systems Inc., 1814 Ryder Drive, Baton Rouge, La. 70808; (504) 769-2154.

CIRCLE 380

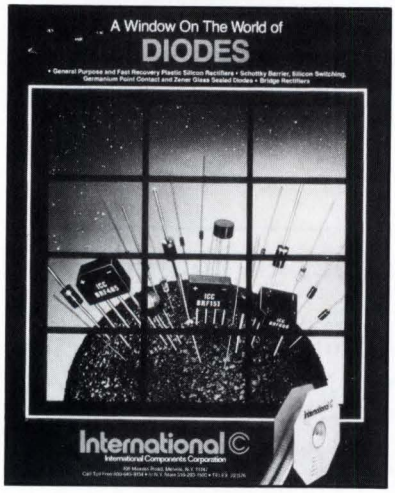
Magnetic circuit breakers

A 30-page brochure features magnetic circuit breakers for the international market. The devices, which protect circuits up to 50 A, are UL-recognized, CSA-certified, and meet IEC spacing requirements.

Airpax Corp., PO Box 868, Cheshire, Conn. 06410; (301) 228-4600.

CIRCLE 381

Rectifiers and zener diodes



A six-page pamphlet specifies general-purpose and fast-recovery silicon rectifiers, Schottky barrier and bridge rectifiers, germanium diodes, and zener diodes. The literature provides case and lead dimensions and applications information.

International Components Corp., 105 Maxess Road, Melville, N.Y. 11747; (516) 293-1500.

CIRCLE 382

IEEE computer publications

The 1985 Publications Catalog of the Computer Society of the Institute of Electrical and Electronics Engineers features 200 titles on a variety of subjects and applications in computer science and engineering. The 28-page document details over 45 best-selling tutorials and nearly 60 conference records and proceedings that have been published since the 1984 catalog.

IEEE Computer Society Press, 1109 Spring St., Suite 300PR, Silver Spring, Md. 20910; (301) 589-8142.

CIRCLE 383

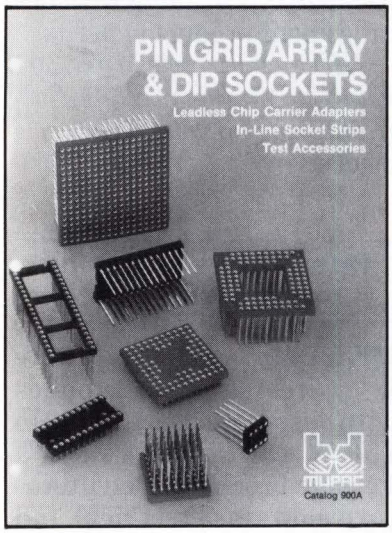
Fifth-generation switching supplies

A four-page pamphlet presents the LR series of fifth-generation switching power supplies, which provide high reliability with half the number of components in a smaller, more compact package. Complete specifications, as well as prices, are given for each of the 16 models that comprise the series. The units deliver 5 to 48 V dc at current ratings of up to 40 A for the lowest-voltage supply and up to 5.8 A for the highest-voltage supply.

Veeco Instruments Inc., Lambda Electronics Division, 515 Broad Hollow Road, Melville, N.Y. 11747; (516) 694-4200.

CIRCLE 384

Pin-grid array and DIP sockets



Outlining a full line of pin-grid array, DIP, and SIP sockets is a 16-page illustrated catalog (No. 900A). Also described in the catalog are leadless chip-carrier adapters and test accessories. The document contains device specifications, photos, features, line drawings, and ordering information.

Mupac Corp., 10 Mupac Drive, Brockton, Mass. 02401; (617) 588-6110.

CIRCLE 385

Single-, multilayer microwave capacitors

Two six-page brochures feature ceramic single-layer capacitors for microwave integrated circuits and multiple-layer capacitors for rf/microwave applications. Each brochure lists capacitance values, types, tolerances, working voltages, and ordering information. Dimensional drawings and typical temperature-coefficient curves are also included.

AVX Corp., PO Box 867, Myrtle Beach, S.C. 29577; (803) 448-9411.

CIRCLE 386

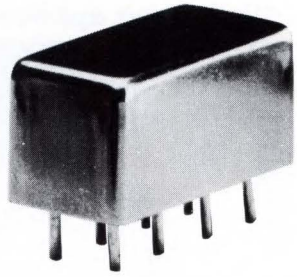
Products for Apple users

The Association of Independent Microdealers (AIM) is offering the first edition of the *Apple Buyer's Guide.* The 323-page catalog lists hardware and software from 162 manufacturers and publishers, covering approximately 2000 products. Items for the Apple IIe, IIc, Macintosh, and Lisa computers are available from participating AIM members or may be ordered directly from AIM headquarters.

Association of Independent Microdealers, 3010 N. Sterling Ave., Peoria, Ill. 61604; (309) 685-4843. $12.95.

CIRCLE 387

electronic attenuator/ switches



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CONTROL	DC-0.05	
INSERTION LOSS, dB	TYP.	MAX.
one octave from band edge	1.4	2.0
total range	1.6	2.5
ISOLATION, dB	TYP.	MIN.
1-10 MHz IN-OUT	65	50
IN-CON	35	25
10-100 MHz IN-OUT	45	35
IN-CON	25	15
100-200 MHz IN-OUT	35	25
IN-CON	20	10
IMPEDANCE	50 ohms	

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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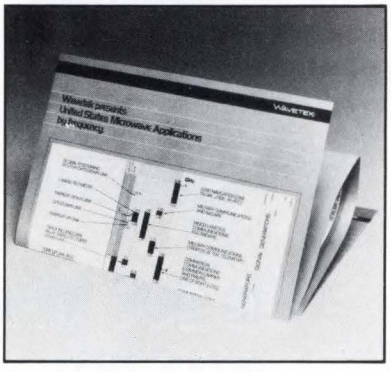
CIRCLE 203

NEW LITERATURE

Frequency chart shows microwave applications



Suitable for wall-mounting, a colorful chart depicts microwave applications by frequency. It identifies the satellite communications up/down links for the commercial C and Ku bands, the military C band, DBS, and MILSTAR. Others include common-carrier microwave links, telemetry L and S bands, and various radar bands. Letter designations are given for both the IEEE STD-521 radar bands and the military ECM bands. The back of the chart describes Wavetek's line of microwave products.

Wavetek, PO Box 85265, San Diego, Calif. 92138; (619) 279-2200.

CIRCLE 388

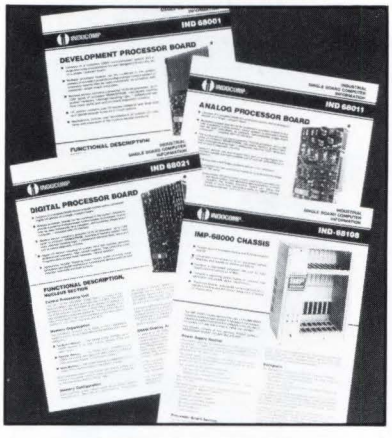
Robotics newsletter

Automation Update, a quarterly newsletter for industrial manufacturers in the plastics and electronics industries, is designed to keep readers abreast of new robotic technology and to create a forum for communicating ideas and issues. The publication presents news on service, accessories, end-of-arm tooling, and successful robot case histories.

Automated Assemblies Corp., 25 School St., Clinton, Mass. 01510; (617) 368-8914.

CIRCLE 389

68000-based industrial computer boards



Four technical publications describe three industrial single-board computers and a chassis that holds up to eight processor boards and eight I/O termination boards. Each of the boards contains a 68000 microcomputer section and either a wire-wrap area, an analog I/O section, or a digital I/O section.

Indocomp Inc., 5409 Perry Drive, PO Box 157, Drayton Plains, Mich. 48020; (313) 674-2294.

CIRCLE 390

CMOS, TTL, and ECL gate arrays

NEC's semicustom gate arrays—including ten CMOS, five TTL, and six ECL families—are described in a 12-page, four-color brochure. Charts show customer interface options, available densities (up to 11,000 gates), and package types, along with details about product benefits.

NEC Electronics Inc., 401 Ellis St., Mountain View, Calif. 94043; (415) 960-6000.

CIRCLE 391

Open-frame switching power supplies

Forty-nine open-frame switching power supplies with output ratings from 40 to 150 W are described in a 12-page brochure. The literature contains electrical and mechanical specifications, as well as pricing information.

Computer Products Inc., Compower Division, 2220 Lundy Ave., San Jose, Calif. 95131; (408) 942-1600.

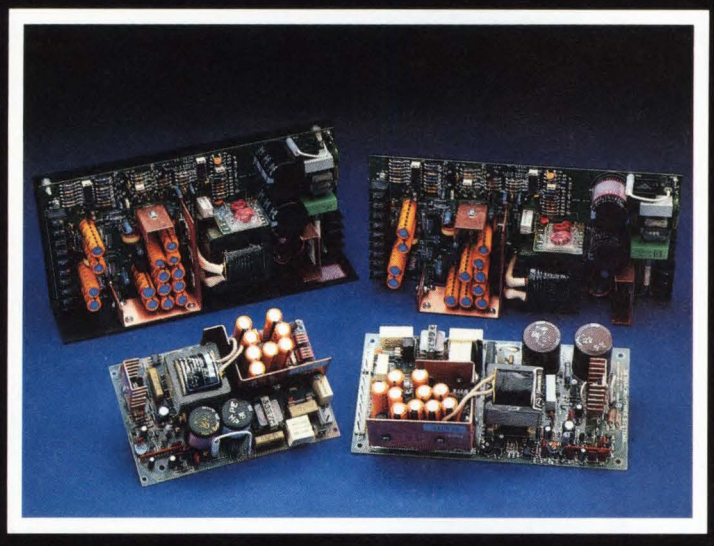
CIRCLE 392

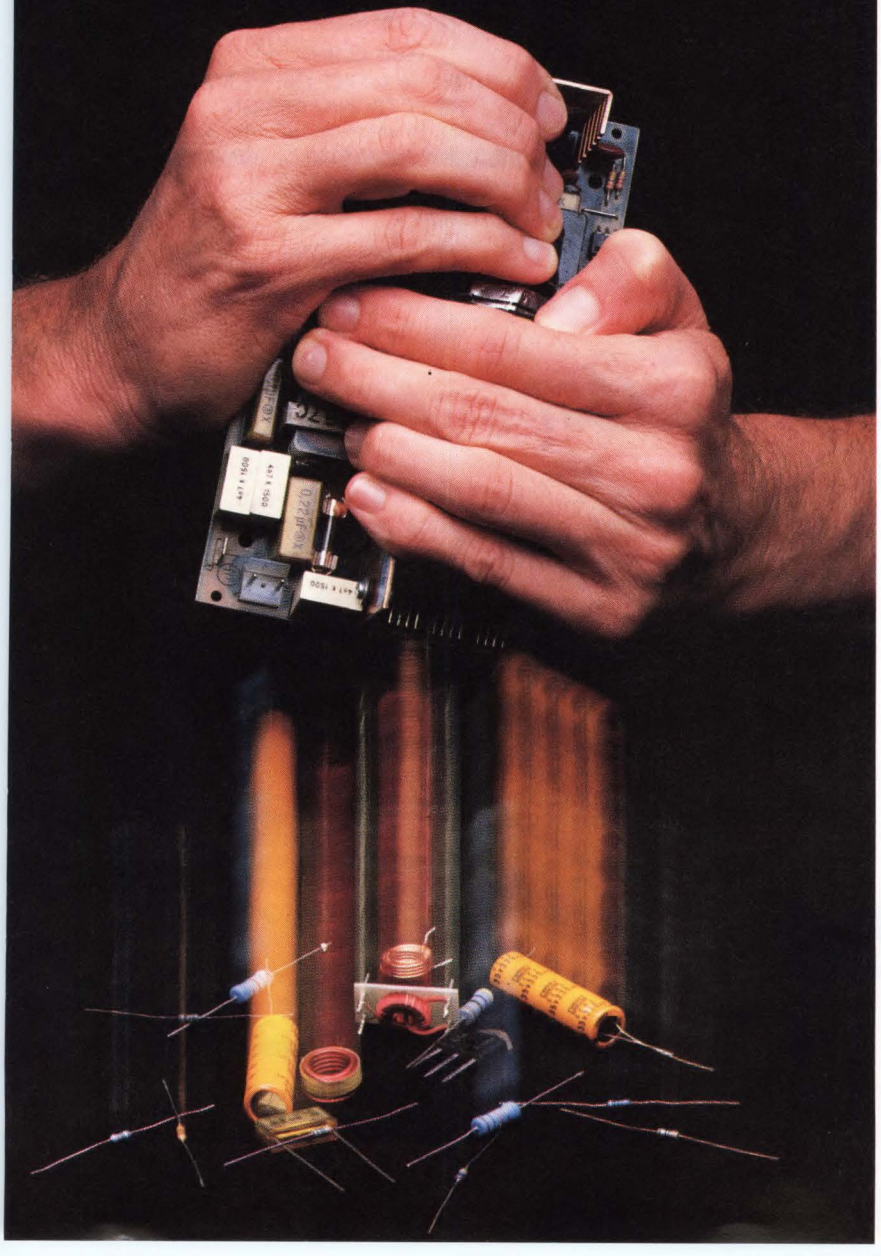
Potting and encapsulating systems

Conapoxy Conacure epoxy potting and encapsulating systems are presented in a bulletin that provides specifications on materials cured at room temperature and at elevated temperatures.

Conap Inc., 1405 Buffalo St., Olean, N.Y. 14760; (716) 372-9650.

CIRCLE 393





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CIRCLE 205

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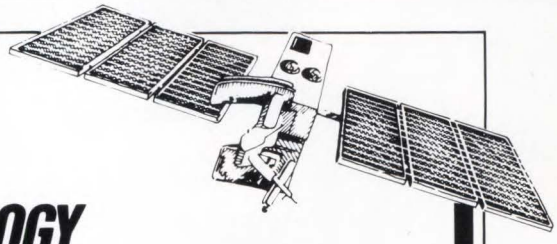

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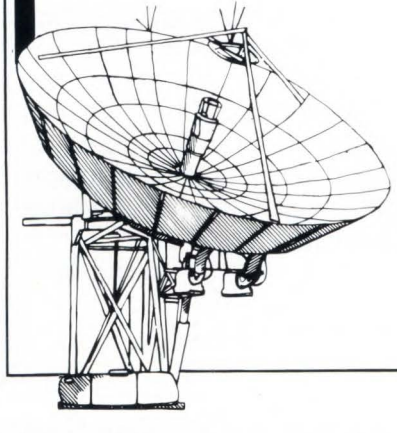

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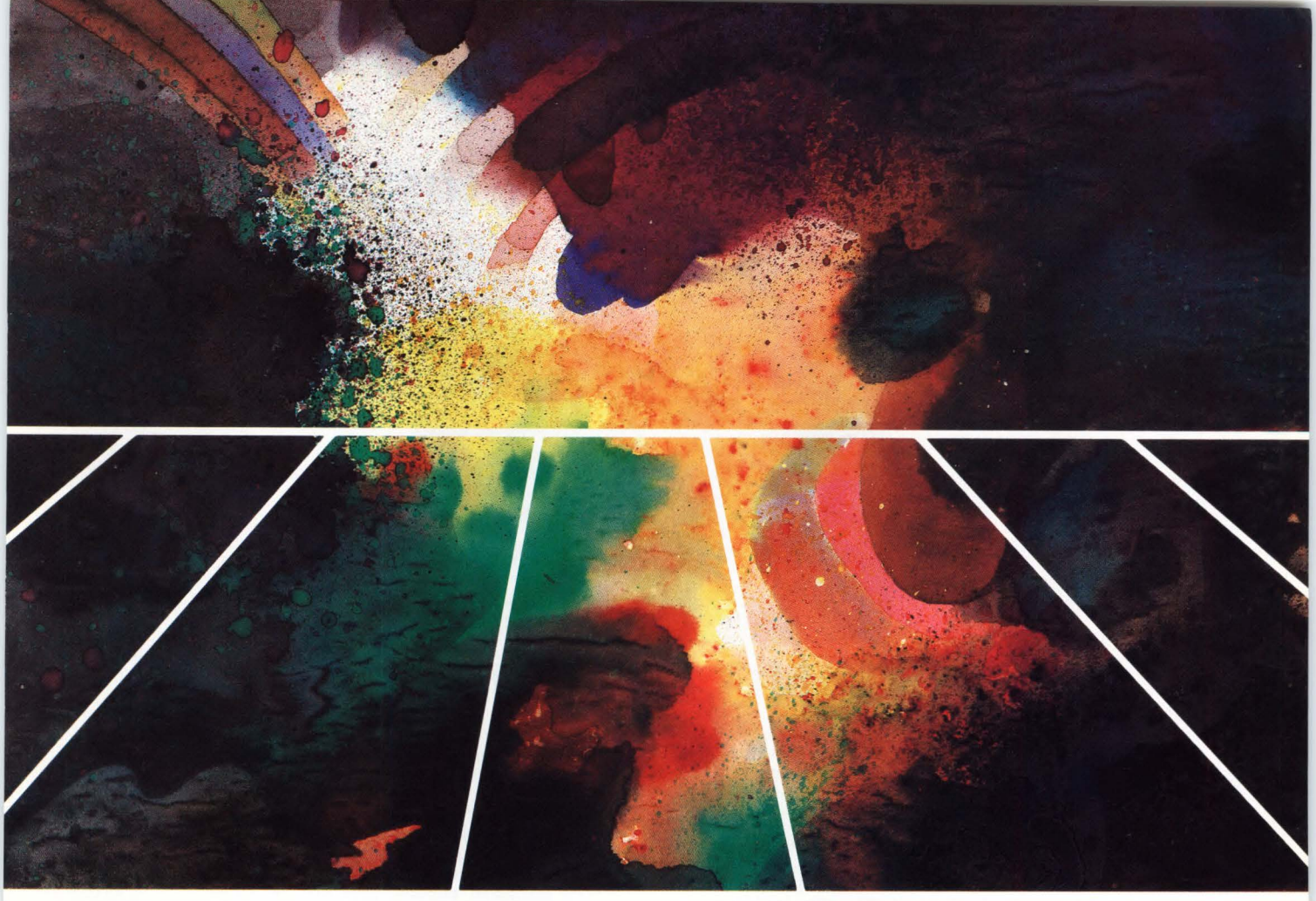

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VLSI TECHNOLOGY, INC.

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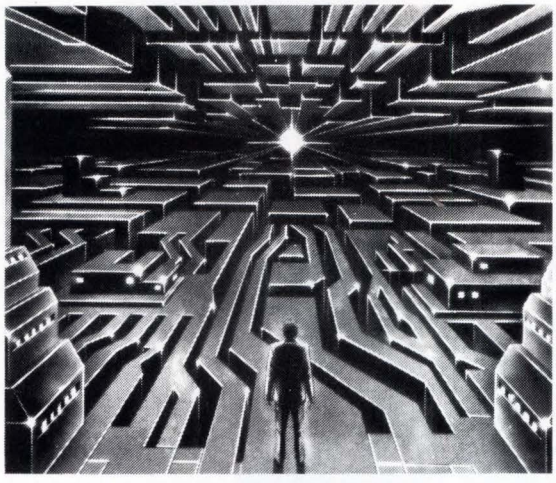

MAKING IT HAPPEN.

Our leadership is a result of our technology...that's how the VLSI revolution came about, here at Intel. Our standard setting microelectronics developments include the first RAM, EPROM, microprocessor, single-board computer, microcomputer development system, and million-bit bubble memory. We also originated CMOS and HMOS technologies, and we will continue to set the standard in the next generation of advanced microprocessors, memory devices and microcontrollers. Intel professionals have vision, desire, convictions and discipline to lead...do you?

PROCESS DEVELOPMENT SCIENTISTS

Carry out independent advanced development in the areas of thin films technology for next generation IC products. Areas of emphasis are:

- Low Pressure and plasma enhanced CVD development.
- Defects studies, impurity doping and various gettering techniques as they relate to controlling end-of-process defect levels, junction-leakage and high resistivity region.
- Development of plasma etching technology for future products.

All positions require a PhD in Chemistry, Chemical or Electrical Engineering or related fields, with at least 5 years experience in research and development.

ADVANCED MEMORY DESIGN ENGINEERS

Responsible for the design and characterization of advanced memory products, including DRAM, E/E^{2}PROM, Static RAM and Magnetic Bubble Memories. Responsibilities include all phases of logic design, circuit design, characterization and transfer. BS/MS/PhD in Engineering Sciences plus related experience.

FUNCTIONAL/PHYSICAL DESIGN CAD

We are seeking CAD professionals with logic and fault simulation, behavioral modeling and mixed level simulation for our Functional Design area. Our Physical Design area requires expertise with layout synthesis including sticks, place and route, cell compilers as well as post design tools including pattern generation and frame generation. CAD and workstation experience desired.

SYSTEMS CAD (Oregon)

This area encompasses functional and physical aspects of board and system-level products. This includes functional through gate-level simulation, testing and test generation, and automatic placement and routing for boards.

PRODUCT ENGINEERS-DEVELOPMENT

Will develop test programs, yield/cost analysis on Sentry, Teradyne, LTX or Megatest systems. Responsible for product characterization and new product introduction for memory component, microprocessor or peripheral products groups. BS/MSEE and related MOS/CMOS experience.

VLSI DESIGN ENGINEERS

Design new high-integration, high-performance CMOS/CHMOS microprocessors or peripherals. Responsible for architecture/microarchitecture simulation, chip and circuit design, chip planning, and layout supervision on CMOS/CHMOS products within our peripheral or microprocessor groups. BS/MS/PhD in Engineering Sciences plus related experience.

Dedicated professionals are now extending our technology into a growing family of components for the future. If you have vision, we'll help you make it happen. For consideration, send your resume to the locations that interest you c/o Intel Employment, Dept. 155742, **Phoenix, AZ,** 5000 W. Williams Field Road, Chandler, AZ 85224; **Santa Clara, CA,** P.O. Box 2546, Santa Clara, CA 95051; **Folsom, CA,** 151 Blue Ravine Road, Folsom, CA 95630; **Albuquerque, NM,** 4100 Sara Road, Rio Rancho, NM 87124; **Portland, OR,** 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124-6497. An Equal Opportunity Employer M/F/H.

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Delivering innovative systems in an exciting and competitive marketplace is a formidable challenge—one that we accept.

At work within the Micro Products Division and Sperry Network Systems groups, we'll surprise you with uncommon opportunities for career growth in state-of-the-art microprocessor and network communications technology.

We are seeking individuals with expertise in the following areas: UNIX Software programming, Systems design engineering, systems programming, SNA, DCA, OSI communications architectures, LAN technology communication software engineering, and many others.

At Sperry, you'll work in a business environment which encourages your participation as you share responsibility with other team members, for developing new generations of micro-based products and data communications systems.

This is the Sperry challenge and we invite your participation.

And, nowhere in America will you find better skiing than in Utah—powder snow, blue skies and sunshine less than 40 minutes away from work.

If you are interested in the Sperry challenge, please send your resume to:
SPERRY, Employment Dept., Attn: Dept. 1D
322 N. Sperry Way, Salt Lake City, Utah 84116

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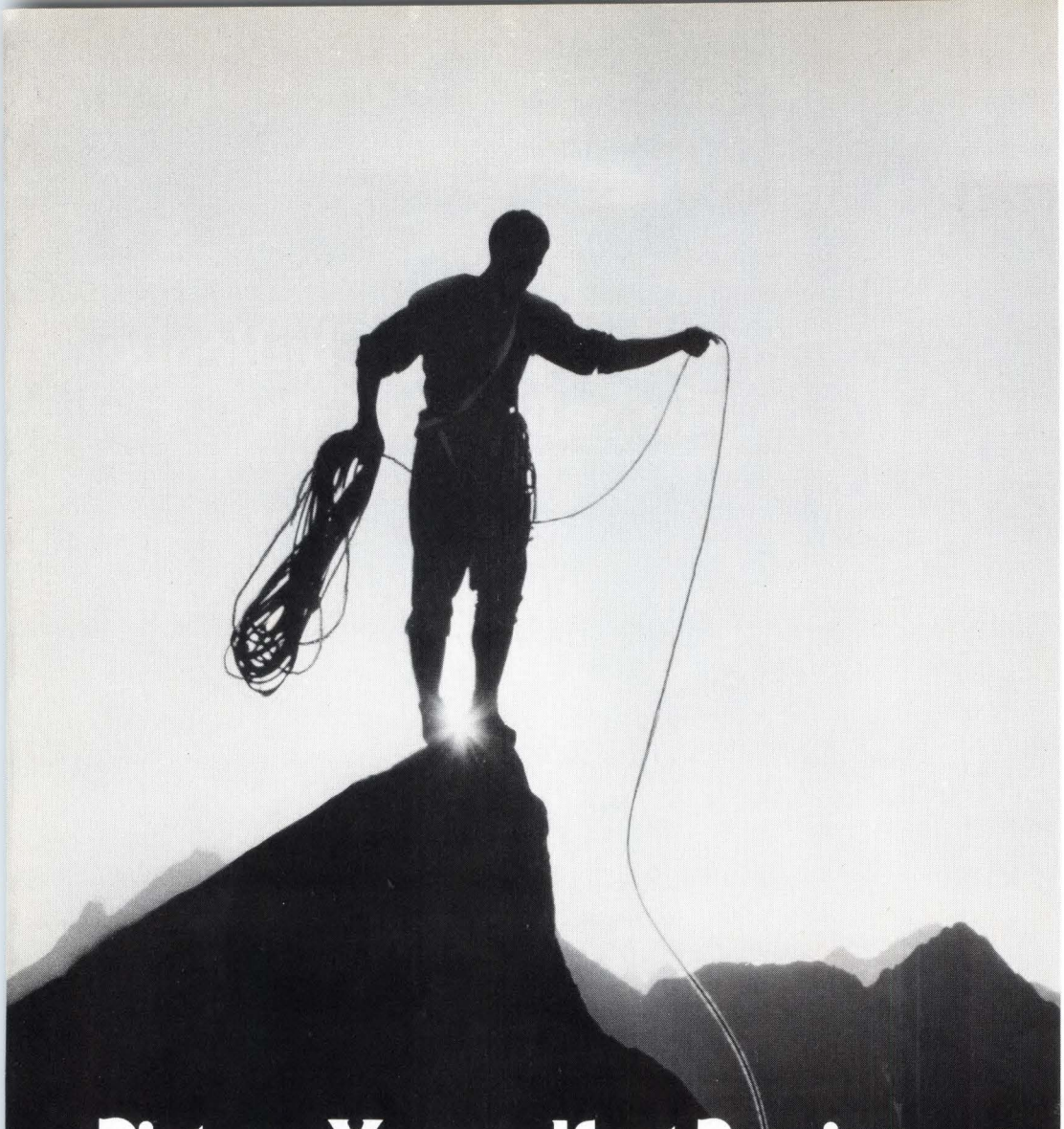

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SOFTWARE ENGINEERS

There are key openings right now for talented people on B1-B Avionics, AI, Image Generation, Radar, Flight Simulation and Commercial Avionics programs.

These positions offer challenging opportunities for the development of advanced technology for the next generation of software engineering.

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SOFTWARE OPERATIONS SUPPORT

OPERATIONAL SOFTWARE DEVELOPMENT

SOFTWARE AND COMPUTER TESTING AND EVALUATION

SUPPORT SOFTWARE DEVELOPMENT

REAL TIME SYSTEMS/ SIMULATION SOFTWARE ENGINEERING

AUTOMATED SYSTEMS TESTING

Some positions require U.S. citizenship.

If you're the right person for the assignment, send your résumé, with present and expected salary, to The Boeing Company, P.O. Box 3707-THX, Seattle, WA 98124.

Data Communications Research Specialists —

Join Racal-Milgo... where the approach to research allows individual options.

Dr. Ming-Luh Kao had the option of taking his advanced technology idea (video compression) through the product development phase...or only through prototype. Dr. Kao elected to start on the next area of technology, yet remained available to those in Development who were preparing the product for market.

"Join the 'right-size' Racal-Milgo research group where you can provide input into the Company's strategic plan, pursue individual specialties, and gain recognition ...while enjoying project diversity, excellent research 'tools' and a large commitment to data communications industry leadership."

— Dr. C. R. Baugh
Senior Director, Applied Research

Racal-Milgo, a world leader in the design, development, manufacture and marketing of data communications systems, has a record of continuous growth, scientific breakthroughs, technical excellence and quality products. Right now we seek research professionals with advanced degrees and/or extensive experience in multiple areas of...

- **Communications Software Technology**
- **Speech/Image Signal Processing**
- **Technology Forecasting**
- **Communications Protocols**
- **Packet/Circuit Switching**
- **Local Area Networks**
- **Broadband Networks**

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Employer (optional): _____

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Phone day (____) _____ night (____) _____

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from _____

Years of experience _____

Please enclose a resume if you have one.

Electrical Engineer Vacuum Technician Mechanical Engineer
Computer Science Physicist

GROWTH CAREERS IN OPTICAL STORAGE

3M has a major commitment to the development and manufacture of optical recording media. We have immediate openings for innovative technical professionals who will contribute to the growth of our high technology erasable and read only optical discs. The location of each position (either St. Paul, Minnesota and/or Menomonie, Wisconsin) is shown within the description.

#1 RESEARCH SPECIALIST

We require an advanced degree in Physics or Optics with 3+ years applied research experience in thin films, optics, microstructures, and/or semiconductors. Will also consider new PhD's with appropriate related graduate level research. Responsibilities include R&D in the areas of mastering and replication of our optical disc recording, and/or development of optical test and recording systems. Location: St. Paul, MN.

#2 RESEARCH SPECIALIST

A BS or advanced degree in Electrical Engineering, Computer Science, or Physics with 3+ years experience in real-time programming, computer interfacing and familiarity with electronic subsystems is required. Responsibilities include developing the software necessary for process control of our thin film deposition systems, and interfacing to process control hardware. Location: St. Paul, MN.

#3 ELECTRICAL ENGINEER

BSEE with educational emphasis in analog and digital design and implementation. We require 3+ years R&D that has involved analog and digital circuitry for electro-optic servo controls and signal processing. Will be responsible for the design and building of optical disc test systems. Location: St. Paul, MN and Menomonie, WI.

#4 ROBOTICS ENGINEER

We prefer an MS in Mechanical, Electrical Engineering or Computer Science. 3+ years experience in the application and implementation of robotic systems, their mechanical modification and software design. Must understand the mechanical limitations of robots. Responsibilities include the specification and customization of robotic systems for clean-room parts handling. Location: St. Paul, MN and Menomonie, WI.

#5 THIN FILM ENGINEER

We will consider a BS or MS in Mechanical, Chemical or other engineering discipline with appropriate experience. Must have working knowledge of and process engineering experience with sputtering and/or other thin film deposition processes and equipment. Responsibilities include specifying and optimizing several thin film processes. Location: Menomonie, WI.

#6 VACUUM TECHNICIAN

Responsibilities include the maintenance, troubleshooting and repair of thin film vacuum coating equipment. Candidates should have 3+ years experience in metal deposition using sputtering and E-Beam methods. Location: Menomonie, WI.

Salary will be based upon candidates level of experience. 3M offers a highly competitive employee benefits program. Relocation expenses paid.

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Interested candidates should mail **(no phone calls or agencies please)** their resumes referencing the appropriate position number and title to Jerry K. Buegler.

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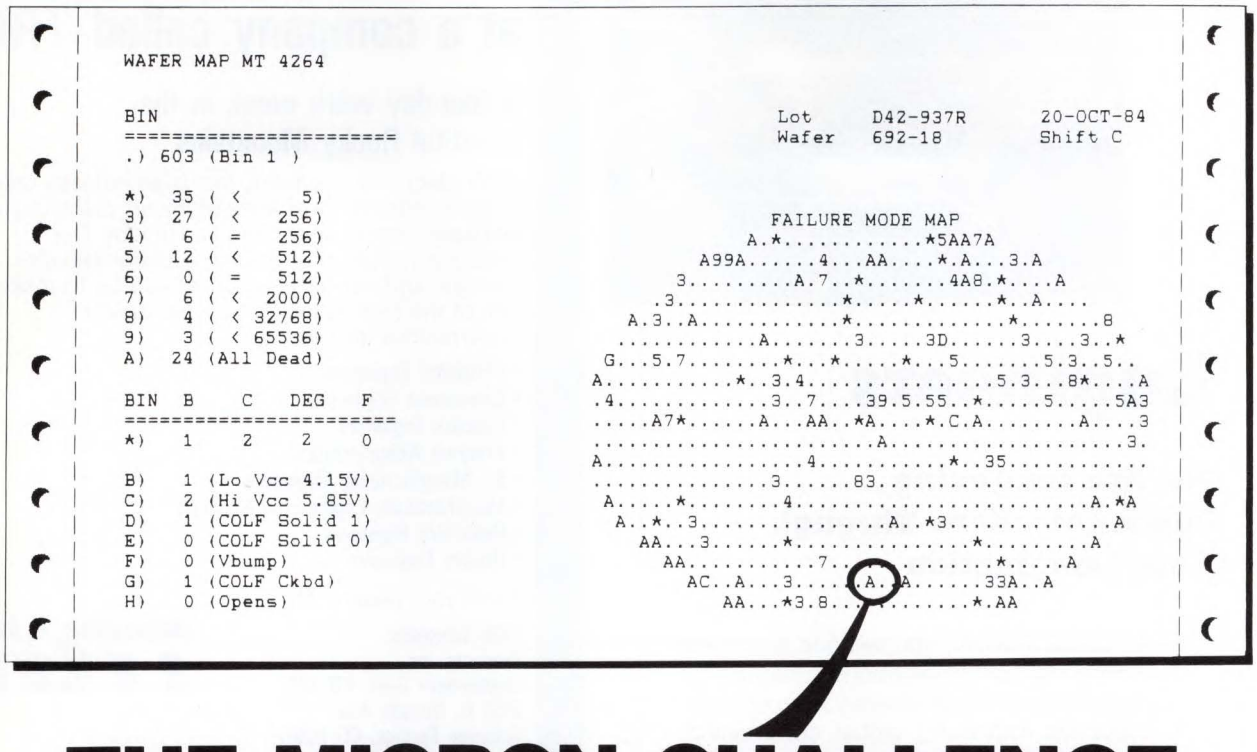

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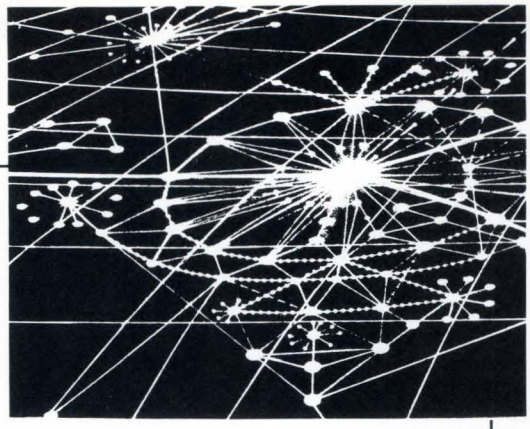

Engineers

We Are Improving Communications Through Your Imagination

At CASE RIXON, you will find a system of internal communications designed for the professional. It allows you to concentrate on improving global communications instead of fighting red tape. The spirit of our company is one of dedication, enthusiasm and adventure. CASE RIXON believes in its product and believes in its people. We recognize and reward innovative thinking and we appreciate the impact your ideas can have on the data communications industry.

For those individuals who are interested in accepting responsibility and who grow with each challenge, CASE RIXON offers the ideal climate for making real contributions. We currently have opportunities in the following areas:

- Network Management Architecture
- LANS Research Engineering (Broadband)
- Hardware Design Engineering
- Software Design Engineering
- LSI Design Engineering
- Applications Engineering (pre and post sales support)

For complete information about these outstanding positions, call John Jaeger at (301) 622-2121, or send your resume in confidence to: CASE RIXON COMMUNICATIONS, Inc., 2120 Industrial Parkway, Silver Spring, MD 20904. An equal opportunity employer.

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- **Process Engineers**
- **Program Administrators**
- **Sr. Manufacturing Engineers**
- **Manufacturing Engineering Manager**
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Employment Dept. KB 198
3650 N. Nevada Ave.
Colorado Springs, CO 80907

TRW

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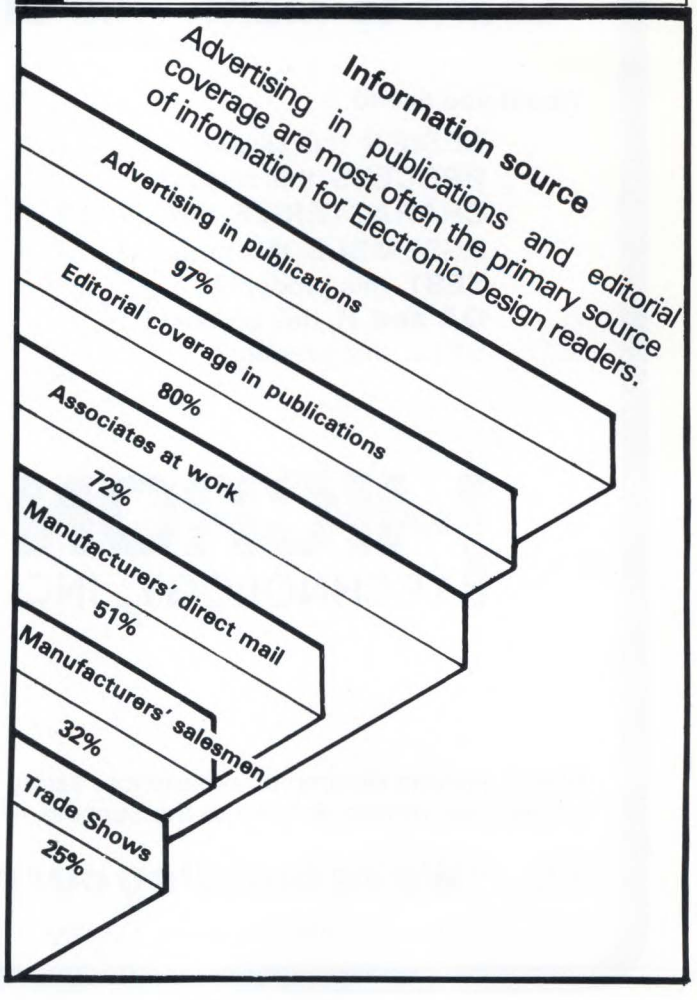

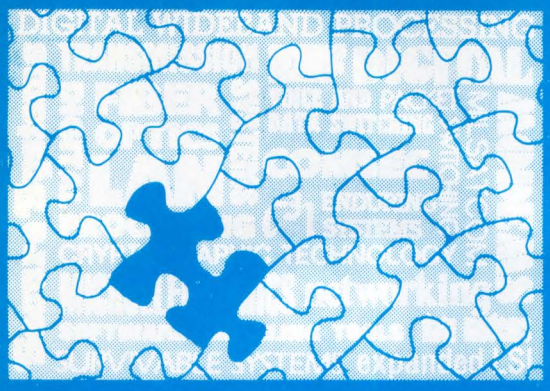

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From extreme environments on earth to remote areas of space—wherever the greatest challenges of modern communications are found, you'll find CSD. Our extensive resources, unmatched experience and total involvement in every area of communications technology makes CSD the pacesetter of the industry. If you can solve difficult communications problems by incorporating divergent technologies and innovations into a complete system design, join CSD on the threshold of new discoveries. Because of our depth, leadership and emphasis on individual achievement, we can create a position specially suited to your interests and abilities. Wherever your career goals lie, you'll find the room to accomplish them at CSD—because we have the future for you.

SYSTEMS ENGINEERS, SOFTWARE ENGINEERS

We are seeking qualified engineers with a BS, MS or PhD in Electrical Engineering or Computer Science, 5+ years experience with military communications systems. Project needs will utilize technical expertise in the areas of:

• Digital Signal Processing • Computer Controlled Data Communications Systems • Computer Communications Networks • Secure Systems • Troposcatter Modems

If you possess specialized knowledge in one or more of these fields, and flourish in an environment whose teamwork brims with visibility and excitement, we invite you to contact us for further, more specific project information. Skills such as yours deserve the attention and rewards our company excels at providing.

Send your resume to: Harriet D. Solomon, GTE's Communication Systems Division, 77 "A" Street, Needham MA 02194. Or call us at 1-800-225-3956.

SYSTEM DESIGN / ACQUISITION ENGINEER

Packet Communications

We require a system design engineer to lead front-end studies of packet networks. Responsibilities include system trade studies and transforming system requirements into hardware and software design specifications. You should have experience with current technology and systems, in either packet radio or packet switching, including analytical determination of correct packet size, network access schemes, coding techniques and other system parameters. BSEE or CS required, MS preferred. 5+ years experience. Familiarity with DoD requirements, specifications and systems is a plus.

Send your resume to: Sherry D. Huffer, Dept. ED 1213, GTE's Communication Systems Division, 400 Park Plaza, P.O. Box 13279 Research Triangle Park NC 27709. Or call us at 919-549-1111.

SYSTEMS ENGINEERING MANAGER

This is an excellent opportunity for a professional with broad experience in communications including specific knowledge of data communications and telephony. We also require a background in hardware programs for real time aspects of stored program control. Your range of experience should include individual contributor level positions through to senior level management of hardware and software groups. You must have at least 15 years experience with a BSEE and MS in EE or CS.

TELEPHONE SYSTEM O&M DESIGN

In this position you will design modern telephone operation and maintenance methods involving SPC switching equipment and centralized O&M facilities. You will provide support to our U.S. operations, with the potential for advancement into European support activities. We require 5-10 years in the above areas along with a BSEE or equivalent experience.

Send your resume to: Brian D. Harris, GTE's Communication Systems Division, Suite 441, 1777 North Kent St., Arlington VA 22209.

We can give you a strong system of support and rewards. Advancement in managerial or technical directions. Recognition within GTE and across the communications industry. Colleagues at the top of their disciplines. And benefits including tuition reimbursement as well as life, medical and dental insurance covering your dependents. For the important opportunities in communications, we can be the last place you'll ever have to look. U.S. Citizenship is required.

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Boston	January 28-29
*Anaheim — AFCEA	January 29-30
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Dallas/Fort Worth	February 25-26
Los Angeles	March 4-5
Minneapolis	March 11-12
Phoenix	March 18-19
Washington, D.C./Baltimore	March 25-26
Orlando	April 1-2
Long Island	April 15-16
Boston	April 22-23
San Jose	April 29-30
Chicago	May 6-7
Denver	May 13-14
Seattle	May 20-21
*Washington, D.C./ Baltimore — AFCEA	June 5-6
Los Angeles/Irvine	June 10-11
Raleigh/Durham	July 15-16
Boston	July 29-30
Dallas/Fort Worth	August 5-6
Long Island	August 12-13
Phoenix	August 19-20
San Jose	August 26-27
Denver	September 9-10
Orlando	September 23-24
Minneapolis	Sept. 30-Oct. 1
Chicago	October 7-8
Los Angeles	October 21-22
Washington, D.C./Baltimore	October 28-29
San Jose	November 11-12
Boston	November 18-19

* Feature Fairs Schedule subject to change

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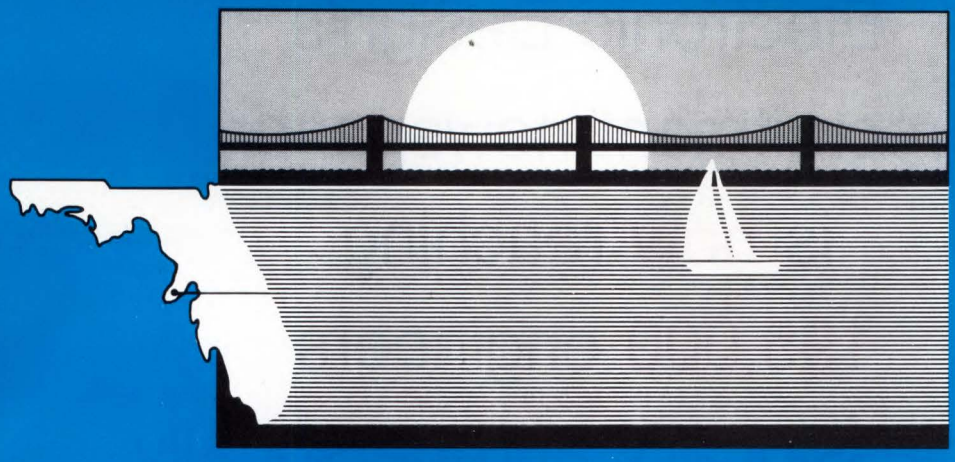

E-SYSTEMS

E-SYSTEMS, INC., ECI DIVISION, ST. PETERSBURG, FLORIDA

And also by the technology we produce. At the ECI Division in St. Petersburg, we're involved in building military communications systems, including everything from satellite communications systems and space communications equipment to shipboard terminals, transmitters, receivers and amplifiers. Electronic data handling systems, including transmission systems, teleprinters and digital plotters. Microwave phased array antennas, conformal arrays and adaptive null steering antennas.

That's why we're known by the people we keep. Because it takes engineers and technical support personnel of the highest quality to live up to the unique challenges we have. If you're qualified, come see what our package of career-long challenges, Flexible Employee Benefits, Human Resource Program, Employee Stock Ownership Plan and Relocation Assistance have to offer.

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- Antenna/Microwave Engineers
- EMI-TEMPEST Engineers
- Quality Engineers
- Systems Engineers
- Member Technical Staff — Data Communications/ Real-Time Systems
- Software Designers — ADA — Packet Switching

If you're the person we're looking for, get to know our company. Send resume to: **Mr. T.B. Harris, Director of Employee Relations, E-Systems, Inc., ECI Division, Dept. 26, P.O. Box 12248, St. Petersburg, Florida 33733.**

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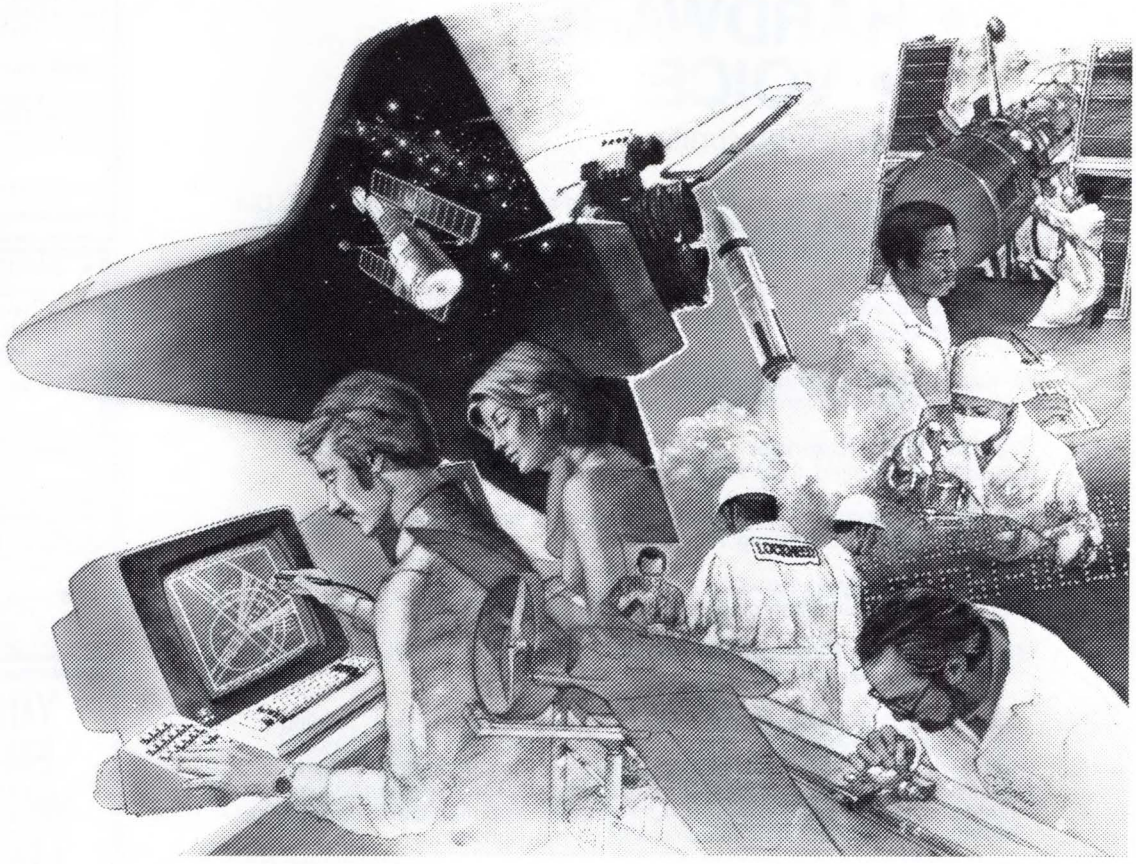

We have initiated an exciting new program in modern electronics design and packaging. A dedicated team of highly skilled engineers is performing advanced electronics systems analysis, design, development and production using the latest computer aided engineering tools and VLSIC technology. We are hiring innovative goal oriented engineers who are interested in expanding their technical and management horizons.

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- Computer aided engineering system design and support using UNIX.
- Sophisticated signal processing algorithm development, simulation and test.
- Firmware design, integration and test.
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- VLSI circuit research, design and packaging.
- Modern electronics packaging and design.
- Microprocessor applications and custom microprocessor design.

Special CAE and semicustom VLSIC design courses are provided for qualified candidates. Positions are available at entry level and above for individuals with BSEE, BSCS, or BSME.

For immediate consideration, send your resume to Professional Staffing, Dept. 518BX07, Lockheed Missiles & Space Company, P.O. Box 3504, Sunnyvale, CA 94088-3504. We are an equal opportunity, affirmative action employer. U.S. citizenship is required.

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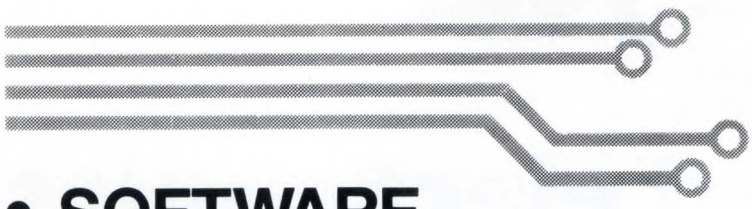
Leadership in Technology



• SOFTWARE • HARDWARE • VOICE

South Florida Opportunities

Racal-Milgo is a world leader in the expanding field of data communications. Our products are high tech and we are growing rapidly! Bring your knowledge and expertise to Racal-Milgo and help us continue to grow in:

- Multiplexing
- Digitized Voice
- Switching
- Networking
- Protocols
- Encryption

We have multiple openings for professionals with experience and skills in one or more of the following high technology areas.

Digitized Voice Engineer — CVSD, ADPCM; E&M interface; loop-start, ground-start signaling; trunk and subscriber line interface.

Real-Time Software — high level languages, assembly language, operating system internals, multitasking, multiuser.

Software Quality Assurance — standards, reliability and maintainability; quality monitoring and improvement in the design environment.

Microprocessor Hardware/Firmware — software and hardware for smaller microprocessor-based projects.

Your professional career at Racal-Milgo offers *many advantages:* a "leading edge," highly sophisticated, professional environment; modern facilities and equipment; an excellent total compensation plan with comprehensive benefits; and an outdoor Florida lifestyle featuring a comfortable climate and diverse recreational opportunities related to sunny days. For confidential consideration, send your resume and salary requirements, in confidence to:

Patrick Ahern, Technical Recruiter

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RACAL
The Electronics Group

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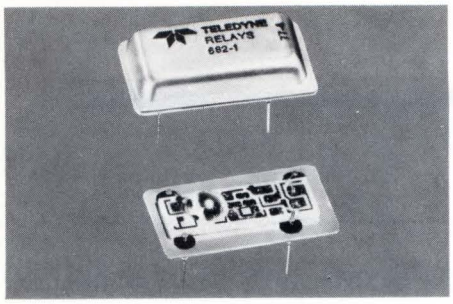

MIL SOLID STATE RELAYS Teledyne 682 AC relay features load rating of 1 amp at 250VRMS, over a frequency of 45 to 440Hz. Zero voltage turn-on assures low EMI. Optical isolation is 1500VRMS. Control range is 3.8 to 32VDC @13mA. Operating temp is −55°C to 100°C. Qualified to MIL-R-28750. $36 each for 500 pcs. Assembly to MIL-883B & 38510A available at additional cost. Model 683 is the DC version. Teledyne Solid State Products 12525 Daphne Ave., Hawthorne, Ca. 90250. (213) 777-0077.

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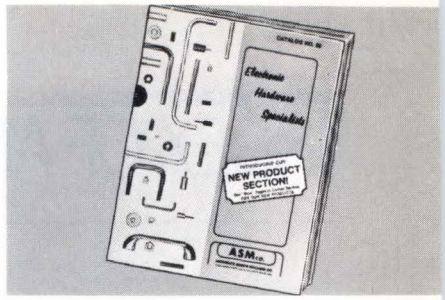
Electronic Circuit Analysis

ECA-2 is a high performance analog circuit simulator, featuring AC, DC and transient analysis. Advanced features include full nonlinear, large circuits, temperature effects, and a modeling facility. The nonlinear capabilities include both polynomials and break-points for all components, including inductors and capacitors. A proper semiconductor diode model is also included. The 8087 is recommended, but not required. For computers running MS-DOS, 192k minimum. Price: $395. A logic simulator is also available. Tatum Labs, P.O. Box 698, Sandy Hook, CT 06482, 203-426-2184.

ANALOG CIRCUIT SIMULATOR **252**



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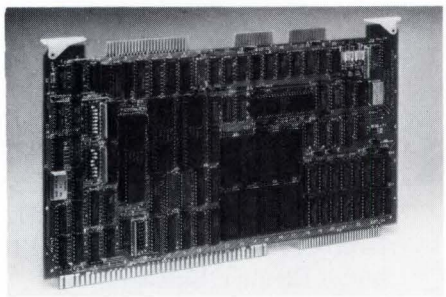

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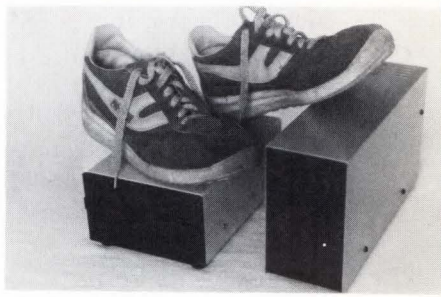

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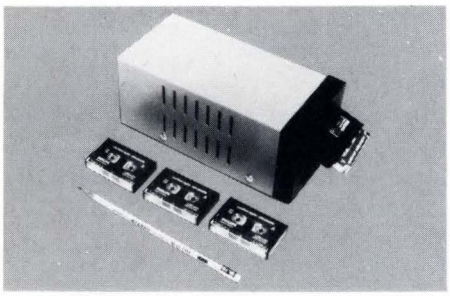

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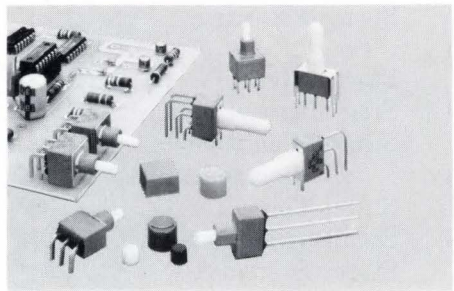

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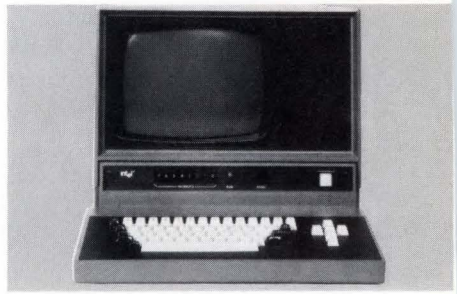

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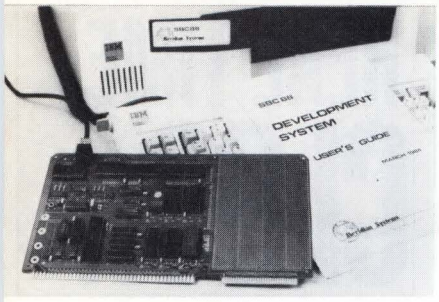

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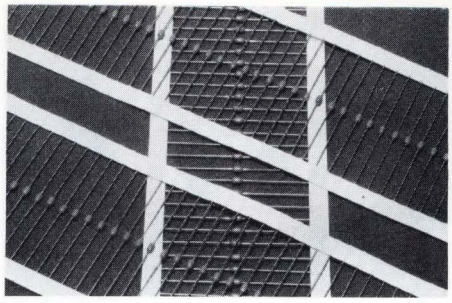

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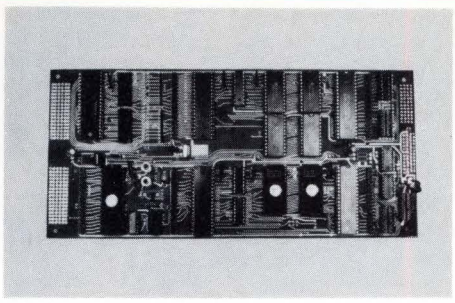

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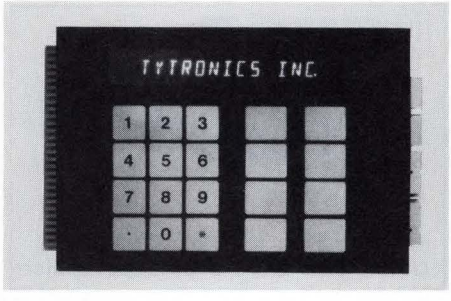

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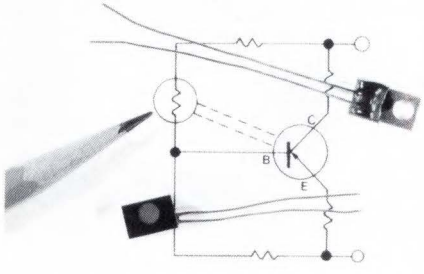

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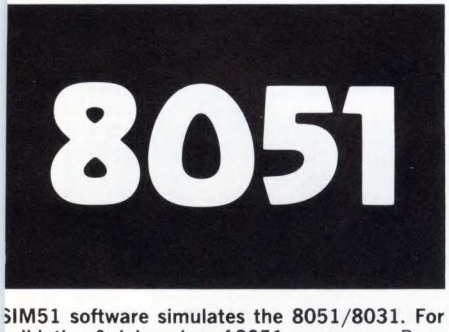
GTE TP-1 PROTECTORS **265**



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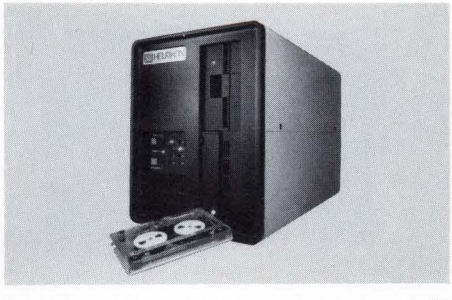
LOGICAL SYSTEMS **266**



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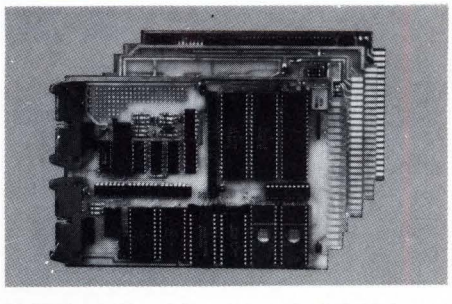

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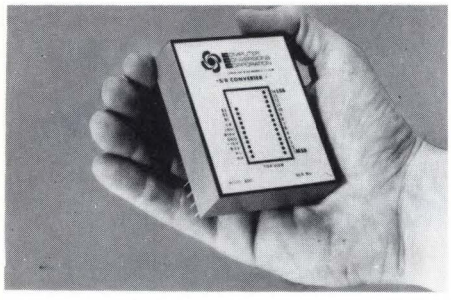

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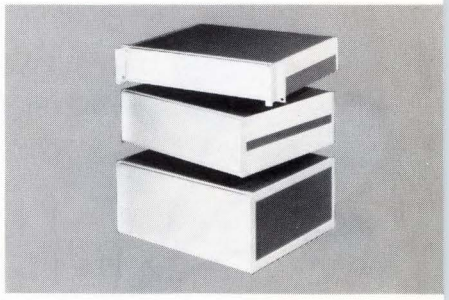

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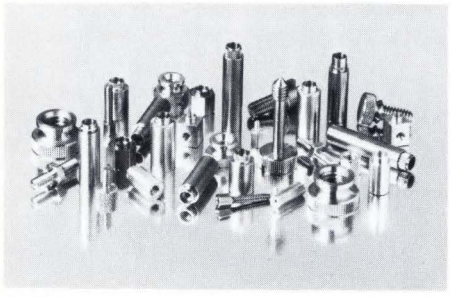

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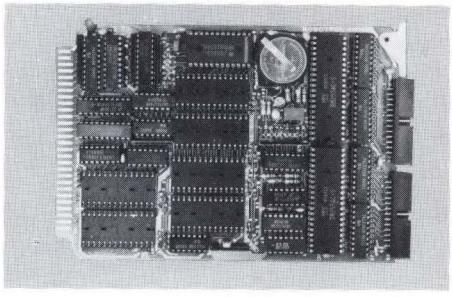

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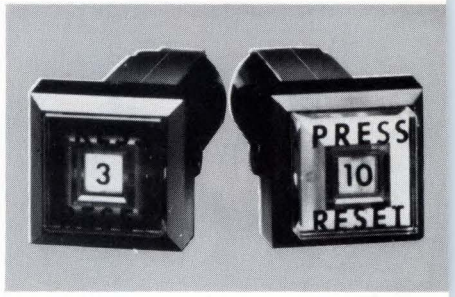
STD CLOCK, MEMORY, I/O **276**



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The new Stag ZL30 is the most cost-effective **programmable logic development system** available. Capable of programming and vector-testing all current 20, 24 and 28-pin PAL* and IFLs, without the need for plug-in modules, the ZL30 can also be used as an aid in the development of fuse patterns. New devices will be catered for by simple firmware changes.

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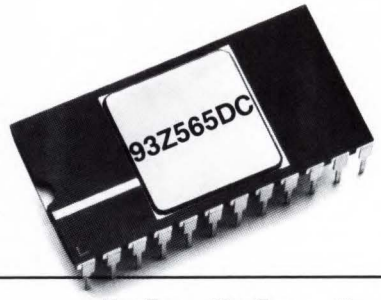

	Max. T_{AA} Commercial	Max. T_{AA} Military	Max. ICC
64K (8Kx8)			
93Z565	55 ns	65 ns	180 mA
93Z565A	45 ns	55 ns	180 mA
16K (2Kx8)			
93Z511	45 ns	55 ns	175 mA
8K (1Kx8)			
93Z451	40 ns	55 ns	135 mA
93Z451A	35 ns	45 ns	135 mA

Available in 24-pin dual-in-line and 28-pin leadless chip carrier. 8K and 16K also available in 24-pin flatpak and 300 mil DIP.

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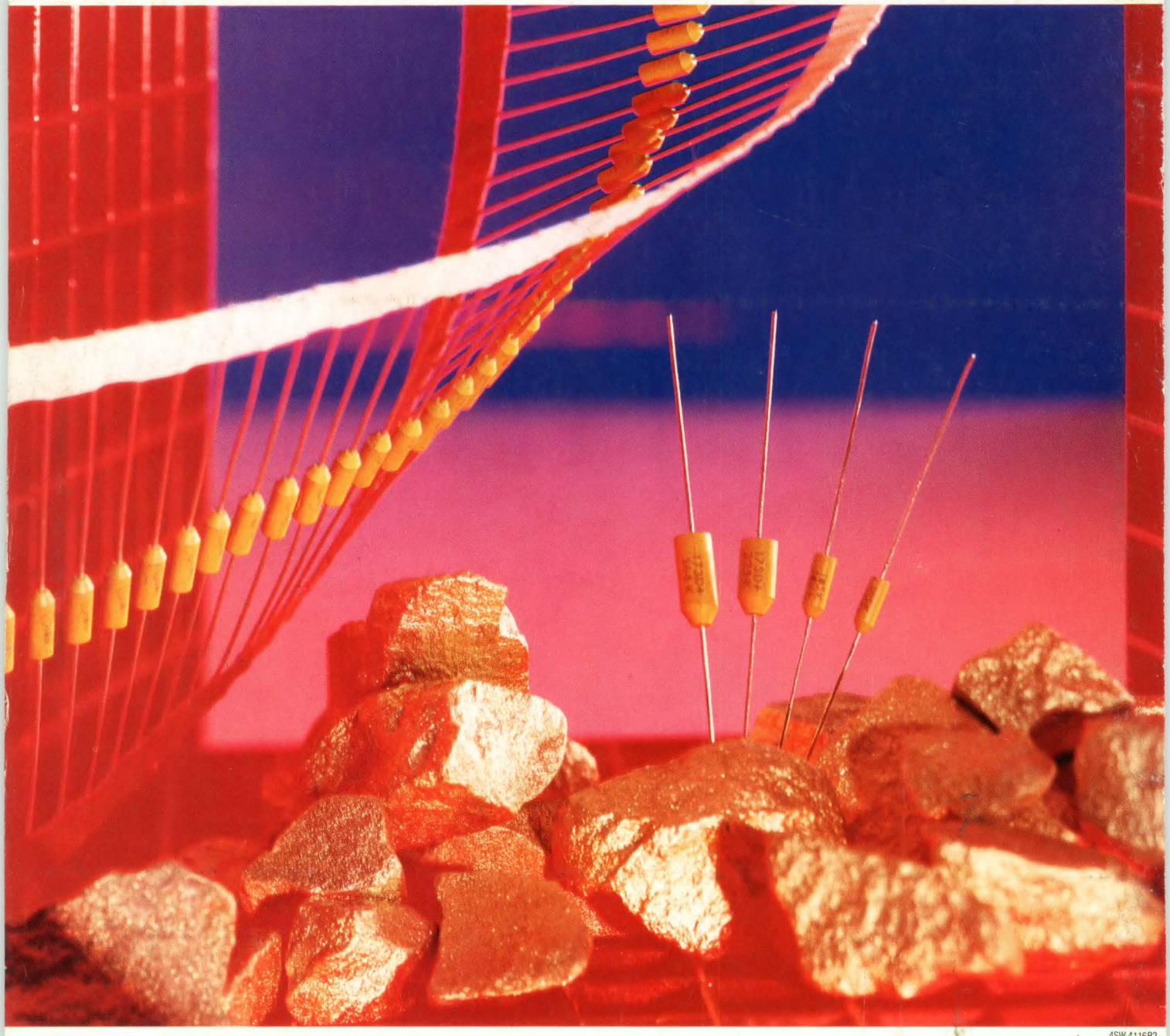

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